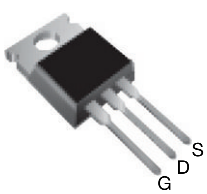
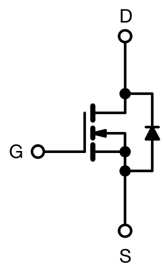
D Series Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V) at T_J max.	550	
$R_{DS(on)}$ max. (Ω) at 25 °C	V_{GS} = 10 V	1.5
Q_g max. (nC)	20	
Q_{gs} (nC)	3	
Q_{gd} (nC)	5	
Configuration	Single	

TO-220AB





N-Channel MOSFET

FEATURES

- Optimal design
  - Low area specific on-resistance
  - Low input capacitance (C_{iss})
  - Reduced capacitive switching losses
  - High body diode ruggedness
  - Avalanche energy rated (UIS)
- Optimal efficiency and operation
  - Low cost
  - Simple gate drive circuitry
  - Low figure-of-merit (FOM): R_{on} x Q_g
  - Fast switching
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- Consumer electronics
  - Displays (LCD or plasma TV)
- Server and telecom power supplies
  - SMPS
- Industrial
  - Welding
  - Induction heating
  - Motor drives
- Battery chargers

ORDERING INFORMATION	
Package	TO-220AB
Lead (Pb)-free	SiHP5N50D-E3
Lead (Pb)-free and Halogen-free	SiHP5N50D-GE3

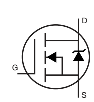
ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	500	V
Gate-Source Voltage			V_{GS}	± 30	
Gate-Source Voltage AC (f > 1 Hz)				30	
Continuous Drain Current (T_J = 150 °C)	V_{GS} at 10 V	T_C = 25 °C	I_D	5.3	A
		T_C = 100 °C		3.4	
Pulsed Drain Current [a]			I_{DM}	10	
Linear Derating Factor				0.83	W/°C
Single Pulse Avalanche Energy [b]			E_{AS}	28.8	mJ
Maximum Power Dissipation			P_D	104	W
Operating Junction and Storage Temperature Range			T_J, T_{stg}	-55 to +150	°C
Drain-Source Voltage Slope	T_J = 125 °C		dV/dt	24	V/ns
Reverse Diode dV/dt [d]				0.28	
Soldering Recommendations (Peak temperature) [c]	for 10 s			300	°C

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.
b. V_{DD} = 50 V, starting T_J = 25 °C, L = 2.3 mH, R_g = 25 Ω, I_{AS} = 5 A.
c. 1.6 mm from case.
d. $I_{SD} \leq I_D$, starting T_J = 25 °C.

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.2	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	500	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 250 μA	-	0.58	-	V/°C
Gate-Source Threshold Voltage (N)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	3	-	5	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30 V	-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 500 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 400 V, V_{GS} = 0 V, T_J = 125 °C	-	-	10	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V; I_D = 2.5 A	-	1.2	1.5	Ω
Forward Transconductance [a]	g_{fs}	V_{DS} = 20 V, I_D = 2.5 A	-	1.8	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 100 V, f = 1 MHz	-	325	-	pF
Output Capacitance	C_{oss}		-	34	-	
Reverse Transfer Capacitance	C_{rss}		-	6	-	
Effective Output Capacitance, Energy Related [b]	$C_{o(er)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V	-	31	-	
Effective Output Capacitance, Time Related [c]	$C_{o(tr)}$		-	41	-	
Total Gate Charge	Q_g	V_{GS} = 10 V; I_D = 2.5 A, V_{DS} = 400 V	-	10	20	nC
Gate-Source Charge	Q_{gs}		-	3	-	
Gate-Drain Charge	Q_{gd}		-	5	-	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 400 V, I_D = 2.5 A, R_g = 9.1 Ω, V_{GS} = 10 V	-	12	24	ns
Rise Time	t_r		-	11	22	
Turn-Off Delay Time	$t_{d(off)}$		-	14	28	
Fall Time	t_f		-	11	22	
Gate Input Resistance	R_g	f = 1 MHz, open drain	-	1.7	-	Ω
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse P - N junction diode 	-	-	5	A
Pulsed Diode Forward Current	I_{SM}		-	-	20	
Diode Forward Voltage	V_{SD}	T_J = 25 °C, I_S = 4 A, V_{GS} = 0 V	-	-	1.2	V
Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = I_S = 2.5 A, dI/dt = 100 A/μs, V_R = 20 V	-	320	-	ns
Reverse Recovery Charge	Q_{rr}		-	1.2	-	μC
Reverse Recovery Current	I_{RRM}		-	8	-	A

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature.

b. $C_{oss(er)}$ is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

c. $C_{oss(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DSS}.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

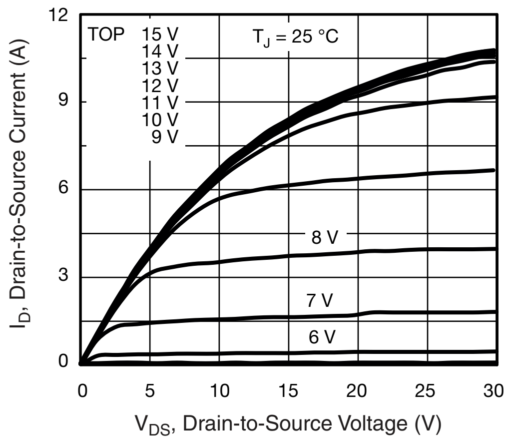


Fig. 1 - Typical Output Characteristics

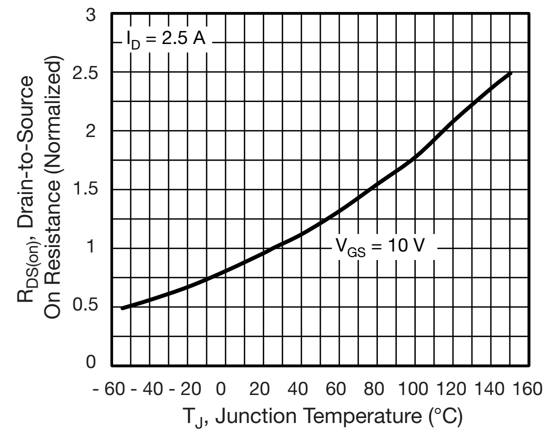


Fig. 4 - Normalized On-Resistance vs. Temperature

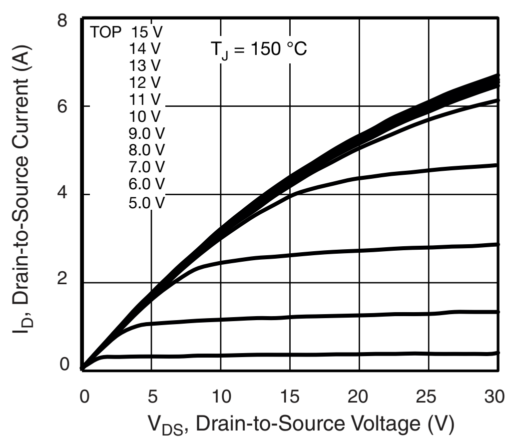


Fig. 2 - Typical Output Characteristics

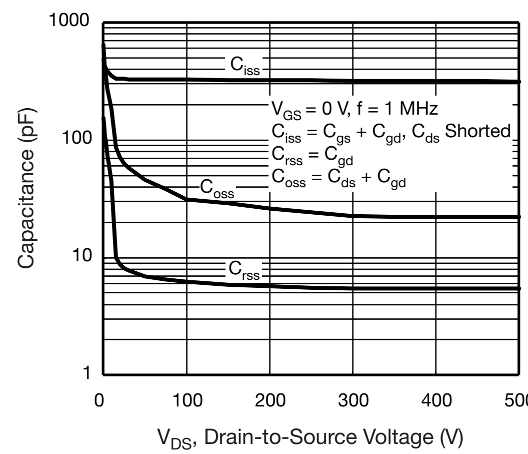


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

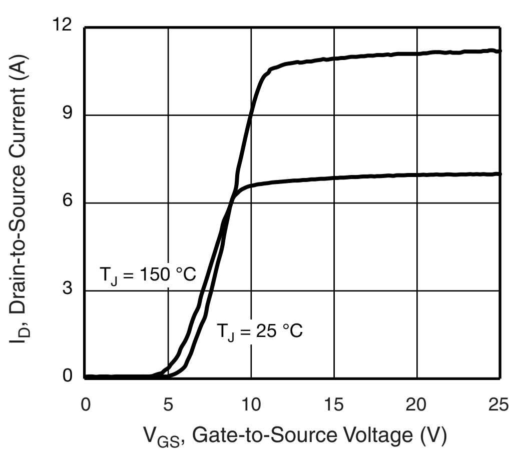


Fig. 3 - Typical Transfer Characteristics

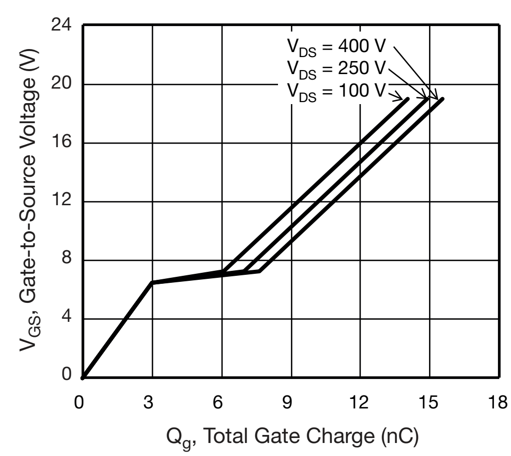


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

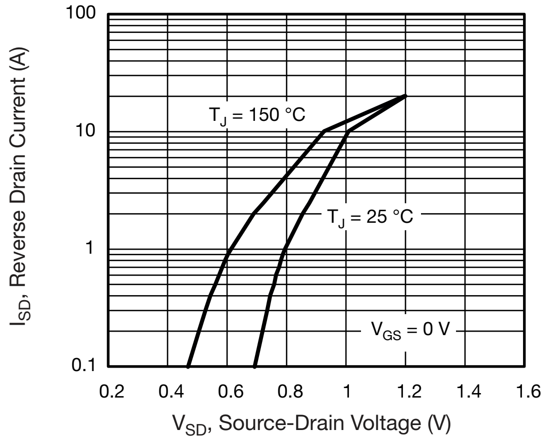


Fig. 7 - Typical Source-Drain Diode Forward Voltage

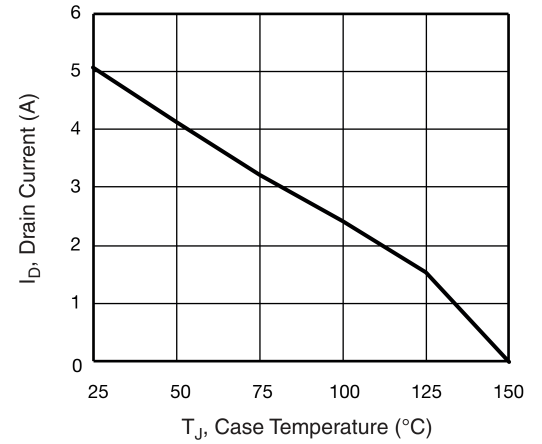
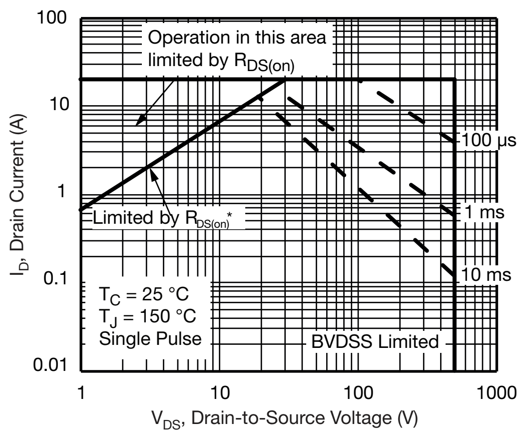


Fig. 9 - Maximum Drain Current vs. Case Temperature



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Fig. 8 - Maximum Safe Operating Area

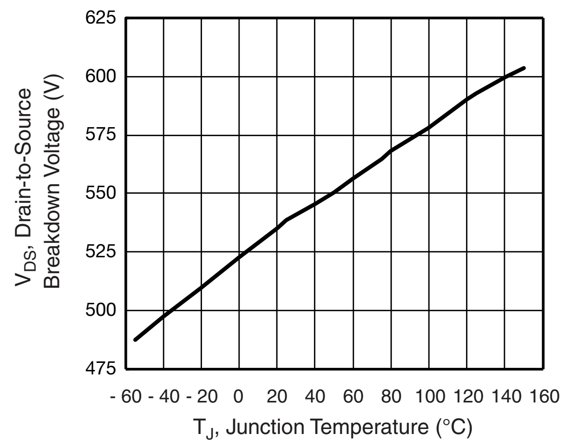


Fig. 10 - Typical Drain-to-Source Voltage vs. Temperature

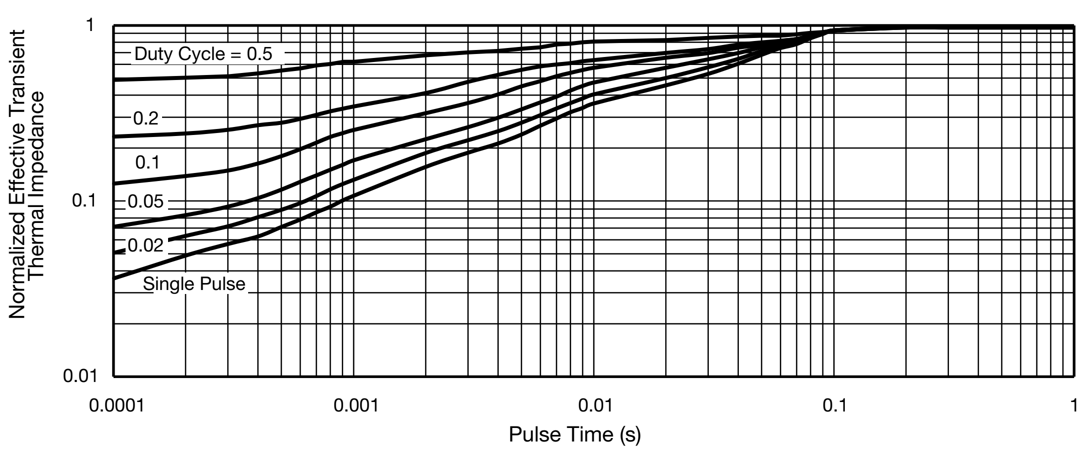


Fig. 11 - Normalized Thermal Transient Impedance, Junction-to-Case

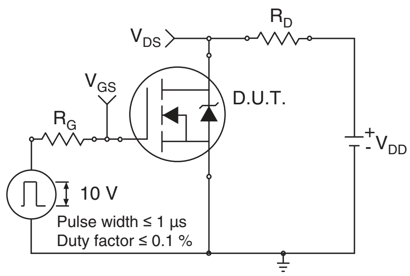


Fig. 12 - Switching Time Test Circuit

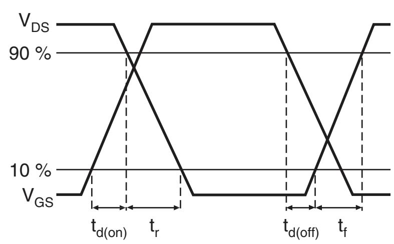


Fig. 13 - Switching Time Waveforms

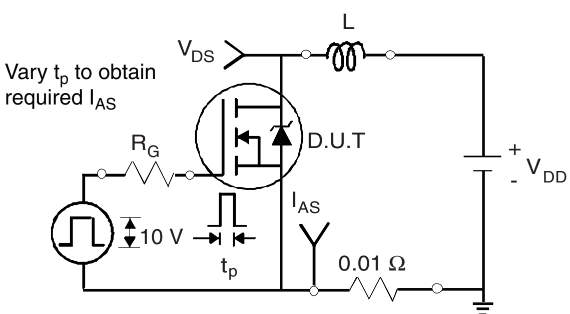


Fig. 14 - Unclamped Inductive Test Circuit

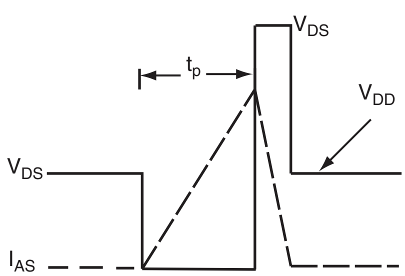


Fig. 15 - Unclamped Inductive Waveforms

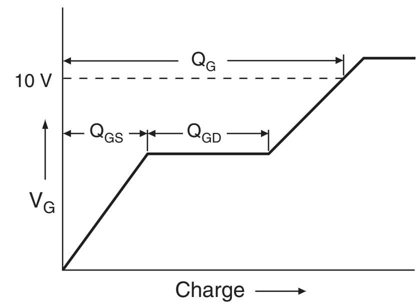


Fig. 16 - Basic Gate Charge Waveform

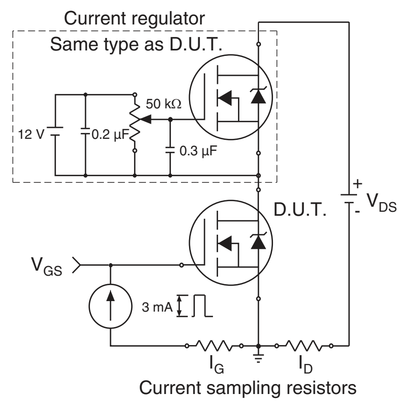
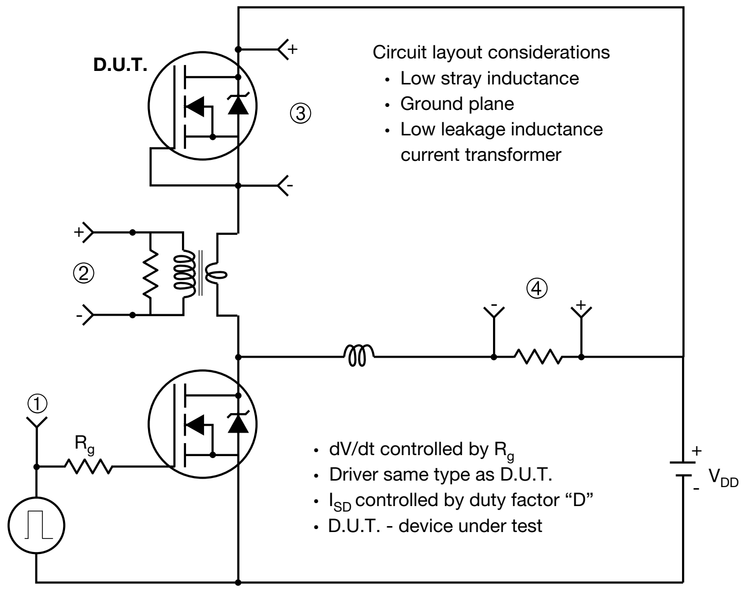
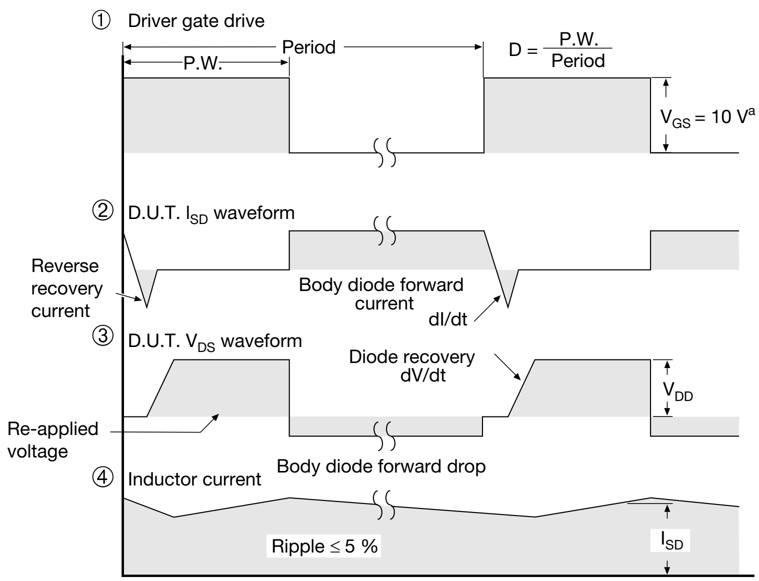


Fig. 17 - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 18 - For N-Channel

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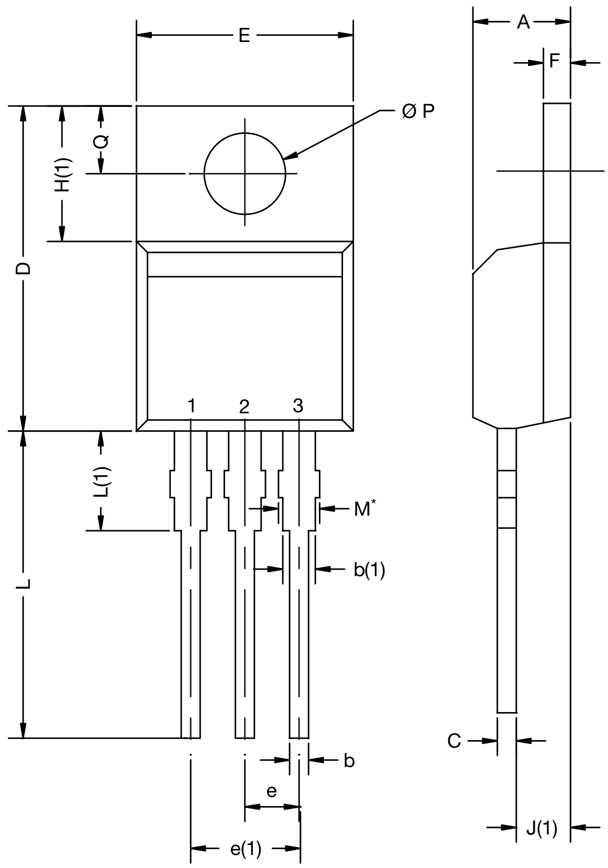
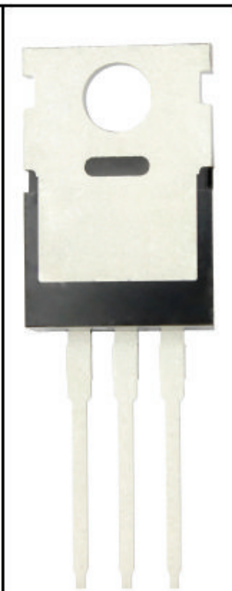
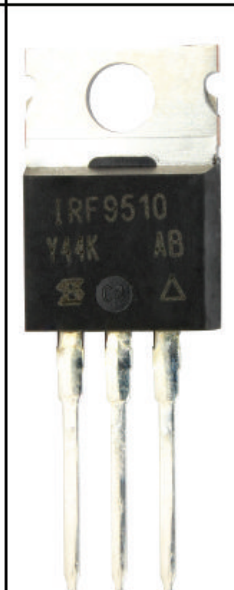
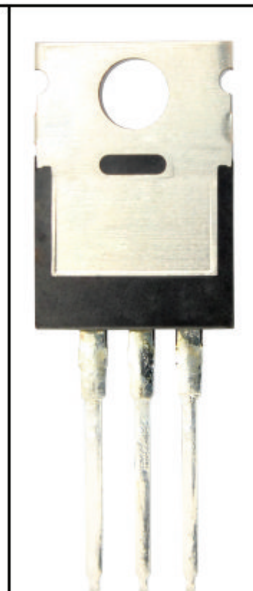
TO-220-1



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	4.24	4.65	0.167	0.183
b	0.69	1.02	0.027	0.040
b(1)	1.14	1.78	0.045	0.070
c	0.36	0.61	0.014	0.024
D	14.33	15.85	0.564	0.624
E	9.96	10.52	0.392	0.414
e	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.10	6.71	0.240	0.264
J(1)	2.41	2.92	0.095	0.115
L	13.36	14.40	0.526	0.567
L(1)	3.33	4.04	0.131	0.159
Ø P	3.53	3.94	0.139	0.155
Q	2.54	3.00	0.100	0.118
ECN: X15-0364-Rev. C, 14-Dec-15 DWG: 6031				

Note

- M* = 0.052 inches to 0.064 inches (dimension including protrusion), heatsink hole for HVM

Package Picture			
ASE		Xi'an	
			

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