SiJ4108DP

RoHS

COMPLIANT HALOGEN

FREE

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Vishay Siliconix



PRODUCT SUMMARY				
V _{DS} (V)	100			
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.009			
$R_{DS(on)}$ max. (Ω) at V_{GS} = 7.5 V	0.0106			
Q _g typ. (nC)	26.5			
I _D (A) ^a	56.7			
Configuration	Single			

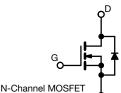
FEATURES

N-Channel 100 V (D-S) MOSFET

- TrenchFET[®] Gen IV power MOSFET
- Very low Q_g and Q_{oss} reduce power loss and improve efficiency
- Flexible leads provide resilience to mechanical stress
- 100 % R_q and UIS tested
- Q_{gd}/Q_{gs} ratio < 1 optimizes switching characteristics
- Material categorization: for definitions of compliance please see <u>www.vishav.com/doc?99912</u>

APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- DC/AC inverters
- Boost converter
- LED backlighting



ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and halogen-free	SiJ4108DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS	$(1_A = 25 \text{ C}, \text{ unles})$	s otherwise noted		
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V _{DS}	100	V
Gate-source voltage		V _{GS}	± 20	v
	T _C = 25 °C		56.7	
Continuous durin comment (T. 150 °C)	T _C = 70 °C		45.3	
Continuous drain current ($T_J = 150 \text{ °C}$)	T _A = 25 °C	I _D	15.2 ^{b, c}	
	T _A = 70 °C		12.1 ^{b, c}	A
Pulsed drain current (t = 100 µs)	I _{DM}	150	A	
	T _C = 25 °C	1	63.1	
Continuous source-drain diode current	T _A = 25 °C	I _S	4.5 ^{b, c}	
Single pulse avalanche current		I _{AS}	25	
Single pulse avalanche energy	L = 0.1 mH	E _{AS}	31.25	mJ
	T _C = 25 °C		69.4	
Maximum power dissipation	T _C = 70 °C	D	44	14/
	T _A = 25 °C	PD	5 ^{b, c}	W
	T _A = 70 °C		3.2 ^{b, c}	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +150	
Soldering recommendations (peak temperature) d, e			260	

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^{b, f}	t ≤ 10 s	R _{thJA}	20	25	°C/W	
Maximum junction-to-case (drain)	Steady state	R _{thJC}	1.3	1.8	0/10	

Notes

a. $T_C = 25 \degree C$

b. Surface mounted on 1" x 1" FR4 board

c. t = 10 s

d. See solder profile (<u>www.vishay.com/doc?73257</u>). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection

e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

f. Maximum under steady state conditions is 65 °C/W

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static	L						
Drain-source breakdown voltage	V _{DS}	$V_{GS} = 0 V, I_{D} = 1 mA$	100	-	-	V	
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	$I_D = 1 \text{ mA}$	-	63	-		
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-7.3	-	mV/°C	
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2	-	4	V	
Gate-source leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$	-	-	± 100	nA	
Zene ante coltana dueire coment		$V_{DS} = 100 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	-	1		
Zero gate voltage drain current	I _{DSS}	V_{DS} = 100 V, V_{GS} = 0 V, T_{J} = 75 °C	-	-	15	μA	
		V _{GS} = 10 V, I _D = 15 A	-	0.0075	0.009	Ω	
Drain-source on-state resistance ^a	R _{DS(on)}	$V_{GS} = 7.5 \text{ V}, \text{ I}_{D} = 10 \text{ A}$	-	0.0085	0.0106		
Forward transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 15 A	-	70	-	S	
Dynamic ^b	· · · · ·					·	
Input capacitance	C _{iss}		-	2440	-	pF	
Output capacitance	C _{oss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz	-	255	-		
Reverse transfer capacitance	C _{rss}		-	16.2	-		
	-	V _{DS} = 50 V, V _{GS} = 10 V, I _D = 15 A	-	34.5	52		
Total gate charge	Qg		-	26.5	40		
Gate-source charge	Q _{qs}	V_{DS} = 50 V, V_{GS} = 7.5 V, I_{D} = 15 A	-	12	-	nC	
Gate-drain charge	Q _{qd}		-	5.3	-		
Output charge	Q _{oss}	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$	-	46	-		
Gate resistance	R _q	f = 1 MHz	0.3	0.8	1.4	Ω	
Turn-on delay time	t _{d(on)}		-	15	30	-	
Rise time	t _r	$V_{DD} = 50 \text{ V}, \text{ R}_{\text{L}} = 3.33 \Omega$	-	7	14		
Turn-off delay time	t _{d(off)}	$I_D \cong 15 \text{ A}, V_{\text{GEN}} = 10 \text{ V}, \text{ R}_{\text{g}} = 1 \Omega$	-	25	50		
Fall time	t _f		-	6	12		
Turn-on delay time	t _{d(on)}		-	18	36	ns	
Rise time	t _r	$\begin{array}{l} V_{DD} = 50 \; V, R_L = 3.33 \; \Omega \\ I_D \cong 15 \; A, V_{GEN} = 7.5 \; V, R_g = 1 \; \Omega \end{array}$	-	8	16	-	
Turn-off delay time	t _{d(off)}		-	22	44		
Fall time	t _f		-	7	14		
Drain-Source Body Diode Characteristic	· · ·			1			
Continuous source-drain diode current	Is	T _C = 25 °C	-	-	63.1		
Pulse diode forward current ($t_p = 100 \ \mu s$)	I _{SM}	-	-	-	150	A	
Body diode voltage	V _{SD}	I _S = 5 A	-	0.75	1.1	V	
Body diode reverse recovery time	t _{rr}	-	-	42	84	ns	
Body diode reverse recovery charge	Q _{rr}	I _F = 10 A, di/dt = 100 A/μs,	-	55	110	nC	
Reverse recovery fall time	t _a	$T_J = 25 \text{ °C}$	-	26	-		
Reverse recovery rise time	t _b		-	16	_	ns	

Notes

a. Pulse test; pulse width $\leq 300~\mu\text{s},$ duty cycle $\leq 2~\%$

b. Guaranteed by design, not subject to production testing

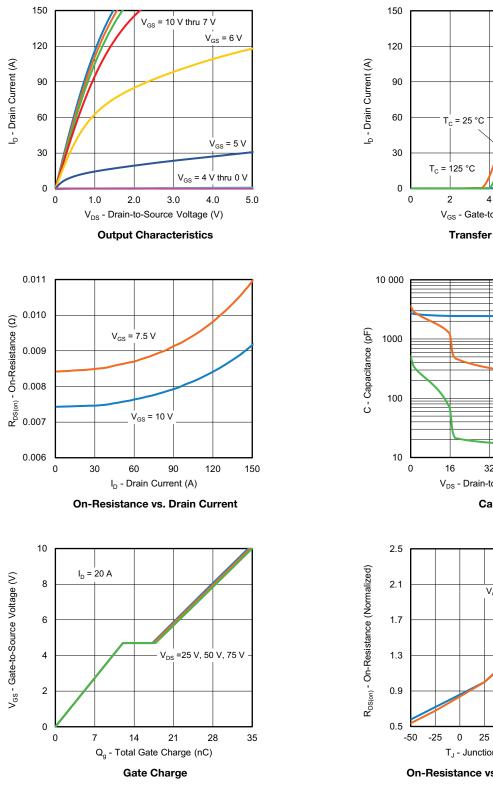
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

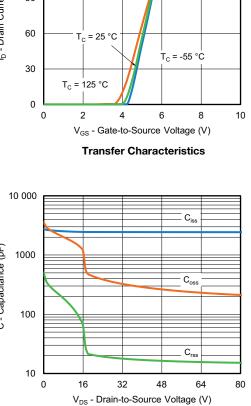
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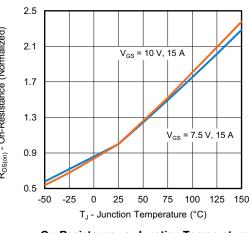
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





Capacitance



On-Resistance vs. Junction Temperature

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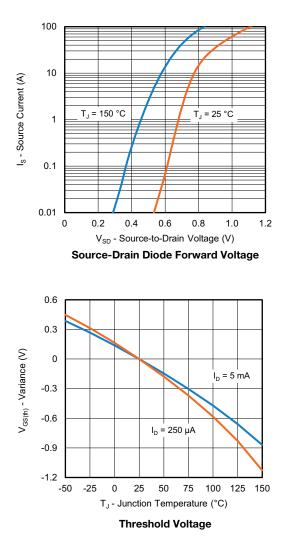
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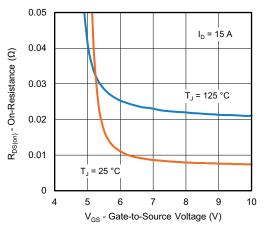
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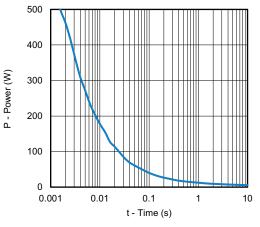
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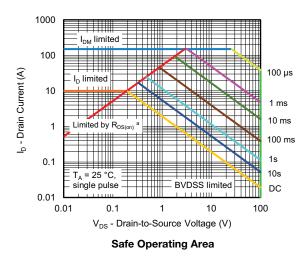




On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



Note

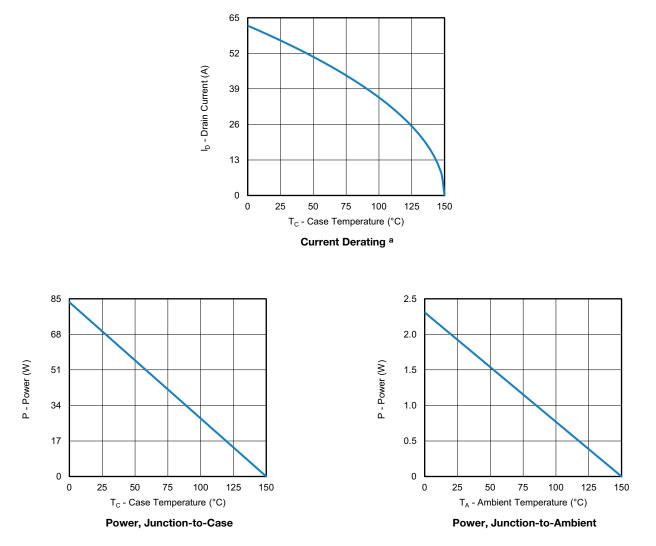
a. V_{GS} > minimum V_{GS} at which R_{DS(on)} is specified

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Note

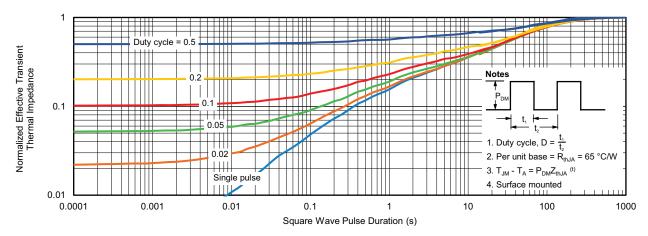
a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



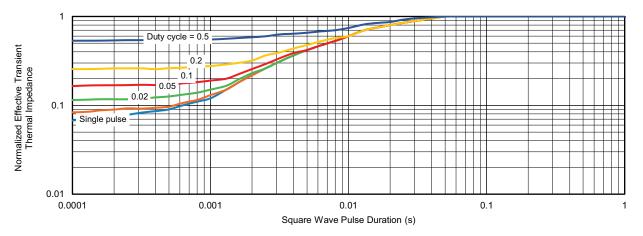
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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