

COMPLIANT

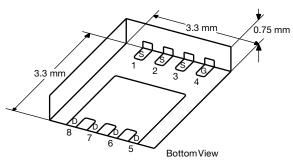
HALOGEN FREE

Vishay Siliconix

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	R _{DS(on)} (Ω) Max.	I _D (A)	Q _g (Typ.)		
	0.0045 at V _{GS} = - 4.5 V	- 50 ^e			
- 20	0.0063 at V_{GS} = - 2.5 V	- 50 ^e	93 nC		
	0.0115 at V _{GS} = - 1.8 V	- 50 ^e			

PowerPAK 1212-8S



SiSS23DN-T1-GE3 (Lead (Pb)-free and Halogen-free)

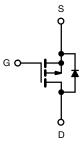
Ordering Information:

FEATURES

- TrenchFET[®] Power MOSFET
- Low Thermal Resistance PowerPAK[®] Package with Small Size and Low 0.75 mm Profile
- 100 % Rg and UIS Tested
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Smart Phones, Tablet PCs, Mobile Computing
 - Battery Switch
 - Load Switch
 - Power Management
 - Battery Management



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 2$	25 °C, unless oth	erwise noted)		
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	- 20	V
Gate-Source Voltage		V _{GS}	± 8	V
	T _C = 25 °C		- 50 ^e	
Continuous Drain Current ($T_J = 150 \ ^{\circ}C$)	T _C = 70 °C		- 50 ^e	
Continuous Drain Current $(1) = 150^{\circ}$ C)	T _A = 25 °C	I I _D	- 27 ^{a, b}	
	T _A = 70 °C		- 21 ^{a, b}	A
Pulsed Drain Current (t = 100 μs)	I _{DM}	- 200	A	
Continuous Source-Drain Diode Current	T _C = 25 °C	la la	- 47.5	
Continuous Source-Drain Diode Current	T _A = 25 °C	ا	- 4 ^{a, b}	
Avalanche Current	L = 0.1 mH	I _{AS}	- 23	
Single-Pulse Avalanche Energy	L = 0.1 mm	E _{AS}	26	mJ
	T _C = 25 °C		57	
Maximum Bower Dissinction	T _C = 70 °C	P _D	36	w
Maximum Power Dissipation	T _A = 25 °C		4.8 ^{a, b}	vv
	T _A = 70 °C	1 [3 ^{a, b}	
Operating Junction and Storage Temperature Range	-	T _J , T _{stg}	- 50 to 150	°C
Soldering Recommendations (Peak Temperature) ^{c, d}			260	

Notes:

a. Surface mounted on 1" x 1" FR4 board.

b. t = 10 s.

c. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

e. Package limited.

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THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{a, b}	t ≤ 10 s	R _{thJA}	21	26	°C/W
Maximum Junction-to-Case (Drain)	Steady State	R _{thJC}	1.7	2.2	C/W

Notes:

a.Surface mounted on 1" x 1" FR4 board. b.Maximum under steady state conditions is 63 °C/W.

Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static				•		
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = - 250 μA	- 20			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	1 050		- 12		mV/
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		3.4		°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	- 0.4		- 0.9	V
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 8 V$			± 100	nA
	I	$V_{DS} = -20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$			- 1	
Zero Gate Voltage Drain Current	IDSS	V _{DS} = - 20 V, V _{GS} = 0 V, T _J = 55 °C			- 10	mV/ °C V
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le -5 V$, $V_{GS} = -4.5 V$	- 20			Α
		V _{GS} = - 4.5 V, I _D = - 20 A		0.0035	0.0045	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 10 A		0.0051	0.0063	Ω
		V _{GS} = - 1.8 V, I _D = - 10 A		0.0081	0.0115	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 20 A		44		S
Dynamic ^b				•		
Input Capacitance	C _{iss}			8840		
Output Capacitance	C _{oss}	V _{DS} = - 15 V, V _{GS} = 0 V, f = 1 MHz		835		pF
Reverse Transfer Capacitance	C _{rss}			900		
Total Cata Charge		$V_{DS} = -15 \text{ V}, \text{ V}_{GS} = -10 \text{ V}, \text{ I}_{D} = -20 \text{ A}$		195	300	
Total Gate Charge	Q_g			93	140	~0
Gate-Source Charge	Q _{gs}	$V_{DS} = -15 \text{ V}, V_{GS} = -4.5 \text{ V}, I_{D} = -20 \text{ A}$		12		nC
Gate-Drain Charge	Q _{qd}			21		
Gate Resistance	R _a	f = 1 MHz	0.5	2.6	5.2	Ω
Turn-On Delay Time	t _{d(on)}			45	90	
Rise Time	t _r	V _{DD} = - 10 V, R _I = 1 Ω		50	100	1
Turn-Off DelayTime	t _{d(off)}	$I_D \cong$ - 10 Å, V_{GEN} = - 4.5 V, R_g = 1 Ω		140	280	
Fall Time	t _f			50	100	ns
Turn-On Delay Time	t _{d(on)}			15	30	
Rise Time	t _r	V_{DD} = - 10 V, R_{L} = 1 Ω		5	10	
Turn-Off DelayTime	t _{d(off)}	$I_D \cong -10$ Å, $V_{GEN} = -10$ V, $R_q = 1$ Ω		150	300	
Fall Time	t _f	Ŭ		40	80	
Drain-Source Body Diode Characterist	ics					
Continuous Source-Drain Diode Current	ا _s	T _C = 25 °C			- 50 ^c	^
Pulse Diode Forward Current ^d	I _{SM}				- 200	А
Body Diode Voltage	V _{SD}	I _F = - 10 A		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}			30	60	ns
Body Diode Reverse Recovery Charge	Q _{rr}			15	30	nC
Reverse Recovery Fall Time	t _a	I _F = - 10 A, dl/dt = 100 A/μs, T _J = 25 °C		16		
Reverse Recovery Rise Time	t _b	1		14		ns

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %. b. Guaranteed by design, not subject to production testing. c. Package limited.

d. $t = 100 \ \mu s$.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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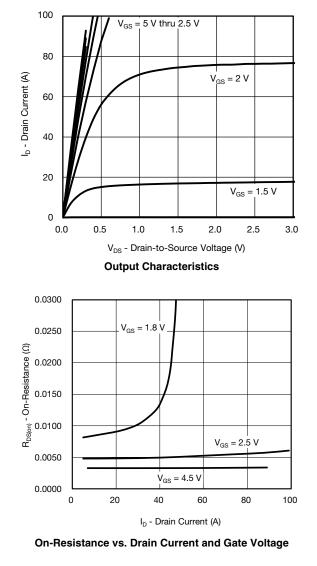
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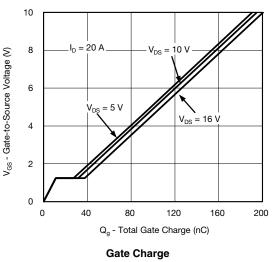


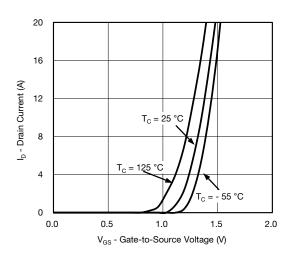
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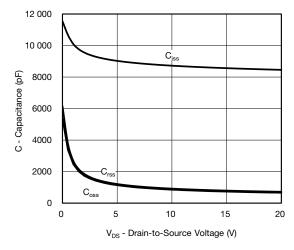
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



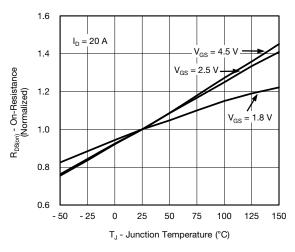




Transfer Characteristics



Capacitance



On-Resistance vs. Junction Temperature

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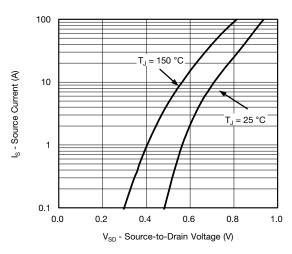
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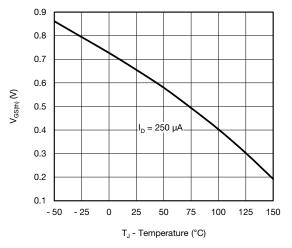
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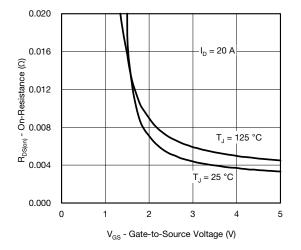
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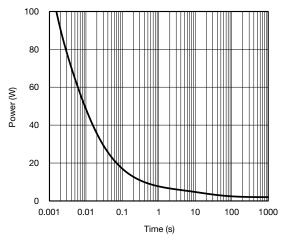
Source-Drain Diode Forward Voltage



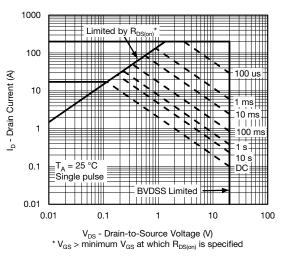




On-Resistance vs. Gate-to-Source Voltage



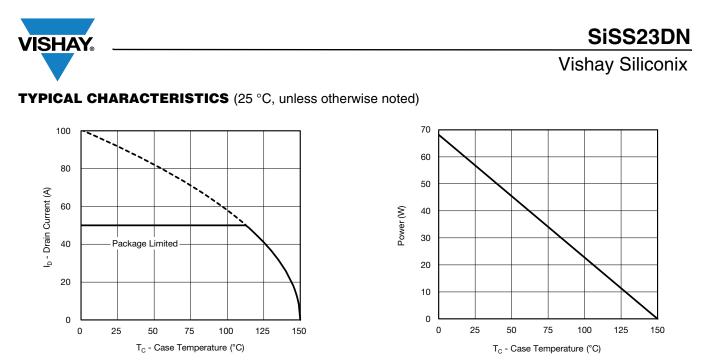
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

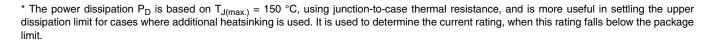
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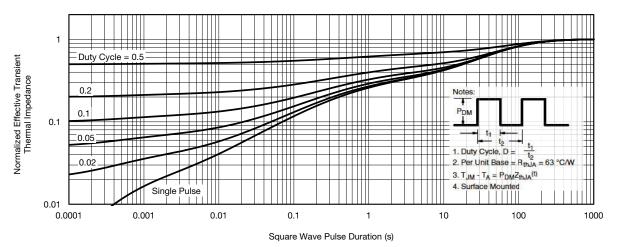
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Current Derating*

Power, Junction-to-Case





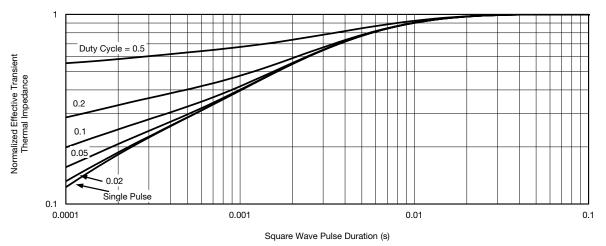
Normalized Thermal Transient Impedance, Junction-to-Ambient

SiSS23DN

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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

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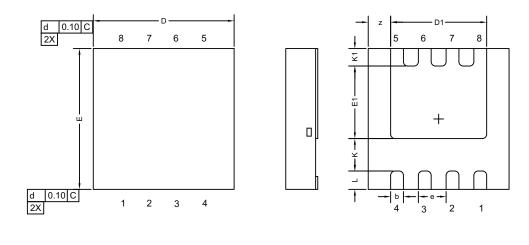
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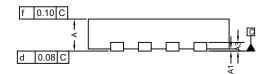
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Case Outline for PowerPAK[®] 1212-8S





DIM.		MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
А	0.67	0.75	0.83	0.027	0.030	0.033		
A1	0	-	0.05	0	-	0.002		
A3		0.20 REF			0.008 REF			
b	0.30 BSC				0.012 BSC			
D	3.30 BSC			0.130 BSC				
D1	2.15	2.25	2.35	0.084	0.088	0.092		
E		3.30 BSC			0.130 BSC			
E1	1.60	1.70	1.80	0.063	0.067	0.071		
е	0.65 BSC			0.026 BSC				
К		0.76 TYP			0.030 TYP			
K1	0.41 TYP			0.016 TYP				
L	0.43 BSC			0.017 BSC				
Z	0.525 TYP			0.021 TYP				

Note

• Millimeters will govern.



RECOMMENDED MINIMUM PADS FOR PowerPAK[®] 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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