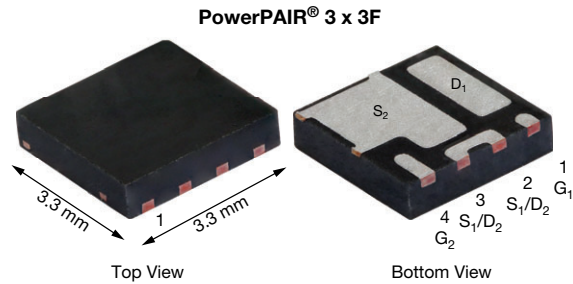


Dual N-Channel 30 V (D-S) MOSFET with Schottky Diode



FEATURES

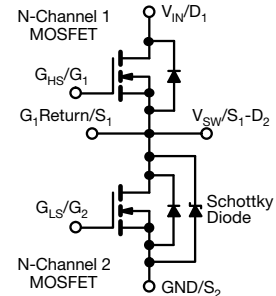
- TrenchFET® Gen IV power MOSFET
- SkyFET® low side MOSFET with integrated Schottky
- 100 % R_g and UIS tested
- Internally connected half-bridge configuration in 3.3 mm-by-3.3 mm footprint
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- CPU core power
- Computer / server peripherals
- POL
- Synchronous buck converter
- Telecom DC/DC



PRODUCT SUMMARY		
	CHANNEL-1	CHANNEL-2
V _{DS} (V)	30	30
R _{DS(on)} max. (Ω) at V _{GS} = 10 V	0.00450	0.00184
R _{DS(on)} max. (Ω) at V _{GS} = 4.5 V	0.00700	0.00257
Q _g typ. (nC)	6.9	19.4
I _D (A) ^a	75	141
Configuration	Dual	

ORDERING INFORMATION	
Package	PowerPAIR 3 x 3F
Lead (Pb)-free and halogen-free	SiZF300DT-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	CHANNEL-1	CHANNEL-2	UNIT	
Drain-source voltage	V _{DS}	30	30	V	
Gate-source voltage	V _{GS}	+20, -16	+16, -12		
Continuous drain current (T _J = 150 °C)	I _D	T _C = 25 °C	75	141	A
		T _C = 70 °C	60	113	
		T _A = 25 °C	23 ^{b, c}	34 ^{b, c}	
		T _A = 70 °C	18 ^{b, c}	27 ^{b, c}	
Pulsed drain current (t = 100 μs)	I _{DM}	150	200	mJ	
Continuous source-drain diode current	I _S	T _C = 25 °C	44		105
		T _A = 25 °C	3.4 ^{b, c}		6.2 ^{b, c}
Single pulse avalanche current	I _{AS}	14	16	mJ	
Single pulse avalanche energy	E _{AS}	9.8	12.8		
Maximum power dissipation	P _D	T _C = 25 °C	48	74	W
		T _C = 70 °C	31	47	
		T _A = 25 °C	3.8 ^{b, c}	4.3 ^{b, c}	
		T _A = 70 °C	2.4 ^{b, c}	2.8 ^{b, c}	
Operating junction and storage temperature range	T _J , T _{stg}	-55 to +150		°C	
Soldering recommendations (peak temperature) ^{d, e}		260			

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	CHANNEL-1		CHANNEL-2		UNIT	
		TYP.	MAX.	TYP.	MAX.		
Maximum junction-to-ambient ^{b, f}	t ≤ 10 s	R _{thJA}	26	33	23	29	°C/W
Maximum junction-to-case (source)	Steady state	R _{thJC}	2	2.6	1.3	1.7	

Notes

- T_C = 25 °C
- Surface mounted on 1" x 1" FR4 board
- t = 10 s
- See solder profile (www.vishay.com/doc?73257). The PowerPAIR 3 x 3F is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 66 °C/W for channel-1 and 67 °C/W for channel-2



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	Ch-1	30	-	-	V
			Ch-2	30	-	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	Ch-1	1.1	-	2.2	
			Ch-2	1.0	-	2.2	
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = +20\text{ V}, -16\text{ V}$	Ch-1	-	-	± 100	nA
		$V_{DS} = 0\text{ V}, V_{GS} = +16\text{ V}, -12\text{ V}$	Ch-2	-	-	± 100	
Zero Gate voltage drain current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	-	1	μA
			Ch-2	-	30	350	
		$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}, T_J = 55\text{ }^\circ\text{C}$	Ch-1	-	-	5	
			Ch-2	-	150	3000	
On-state drain current ^b	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	Ch-1	10	-	-	A
			Ch-2	10	-	-	
Drain-source on-state resistance ^b	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-1	-	0.00330	0.00450	Ω
		$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-2	-	0.00160	0.00184	
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$	Ch-1	-	0.00490	0.00700	
		$V_{GS} = 4.5\text{ V}, I_D = 7\text{ A}$	Ch-2	-	0.00210	0.00257	
Forward transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-1	-	60	-	S
		$V_{DS} = 10\text{ V}, I_D = 20\text{ A}$	Ch-2	-	90	-	
Dynamic ^a							
Input capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Ch-1	-	1100	-	pF
Output capacitance	C_{oss}		Ch-2	-	3150	-	
			Ch-1	-	530	-	
Reverse transfer capacitance	C_{rss}		Ch-2	-	1550	-	
			Ch-1	-	40	-	
C_{rss}/C_{iss} ratio			Ch-2	-	170	-	
			Ch-1	-	0.036	0.072	
Total gate charge	Q_g		$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	Ch-1	-	14.4	22
		Ch-2		-	41	62	
Gate-source charge	Q_{gs}	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	-	6.9	10.5	
			Ch-2	-	19.4	29	
Gate-drain charge	Q_{gd}	$V_{DS} = 15\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$	Ch-1	-	3.1	-	
			Ch-2	-	7.1	-	
Output charge	Q_{oss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$	Ch-1	-	1.5	-	
			Ch-2	-	3.8	-	
Gate resistance	R_g	$f = 1\text{ MHz}$	Ch-1	-	13	-	
			Ch-2	-	40	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	0.14	0.7	1.4	Ω
			Ch-2	0.12	0.62	1.2	
Rise time	t_r	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	-	17	35	ns
			Ch-2	-	25	50	
Turn-off delay time	$t_{d(off)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	-	40	80	
			Ch-2	-	53	110	
Fall time	t_f	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	-	23	45	
			Ch-2	-	30	60	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	-	7	15	
			Ch-2	-	12	25	
Rise time	t_r	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	-	11	20	
			Ch-2	-	13	25	
Turn-off delay time	$t_{d(off)}$	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	-	5	10	
			Ch-2	-	20	40	
Fall time	t_f	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	-	23	45	
			Ch-2	-	32	65	
Fall time	t_f	$V_{DD} = 15\text{ V}, R_L = 3\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$	Ch-1	-	5	10	
			Ch-2	-	6	15	



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
Drain-Source Body Diode Characteristics							
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	Ch-1	-	-	44	A
			Ch-2	-	-	105	
Pulse diode forward current ^a	I_{SM}		Ch-1	-	-	150	
			Ch-2	-	-	200	
Body diode voltage	V_{SD}	$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$	Ch-1	-	0.75	1.1	V
		$I_S = 5\text{ A}, V_{GS} = 0\text{ V}$	Ch-2	-	0.44	0.7	
Body diode reverse recovery time	t_{rr}	$I_F = 10\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$	Ch-1	-	36	75	ns
Body diode reverse recovery charge	Q_{rr}		Channel-1	Ch-1	-	26	
			Channel-2	Ch-2	-	40	80
Reverse recovery fall time	t_a		Channel-2	Ch-1	-	16	-
Reverse recovery rise time	t_b	Ch-2	Ch-2	-	18	-	
		Ch-1	Ch-1	-	20	-	
			Ch-2	-	28	-	

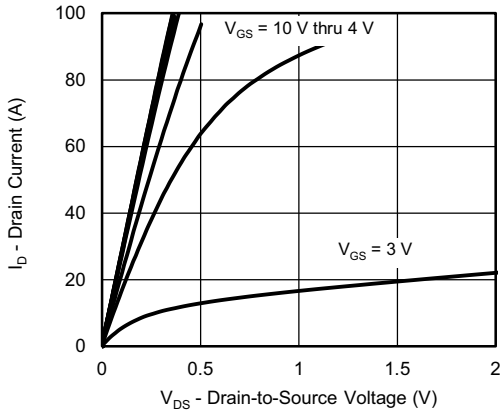
Notes

- a. Guaranteed by design, not subject to production testing
b. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

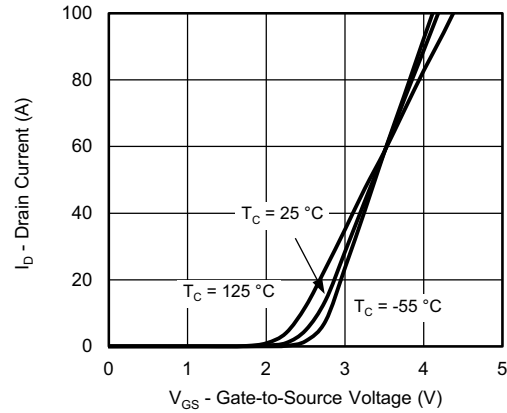
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



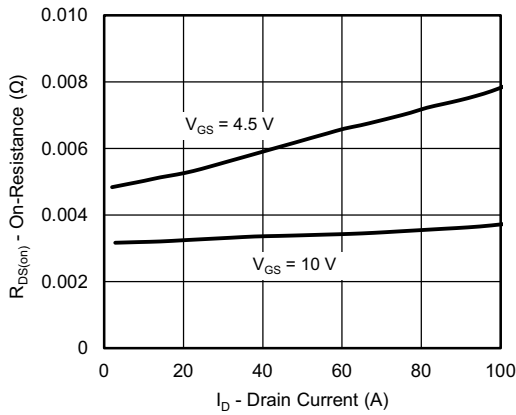
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



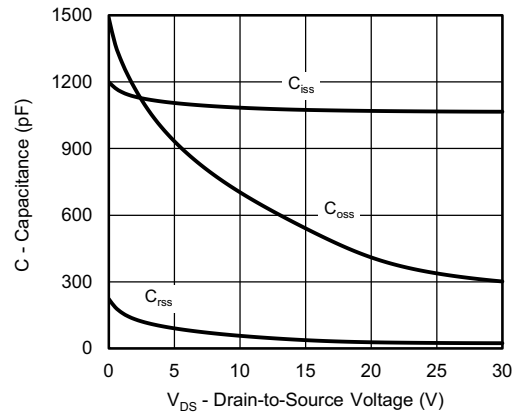
Output Characteristics



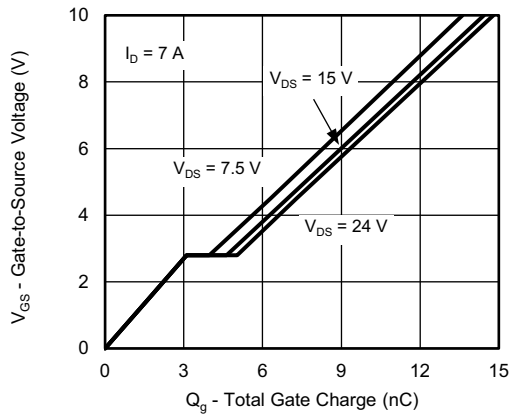
Transfer Characteristics



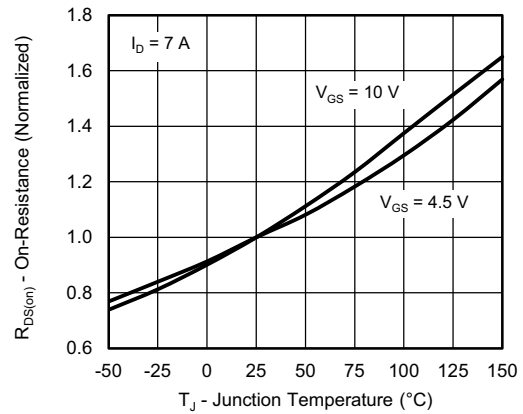
On-Resistance vs. Drain Current



Capacitance



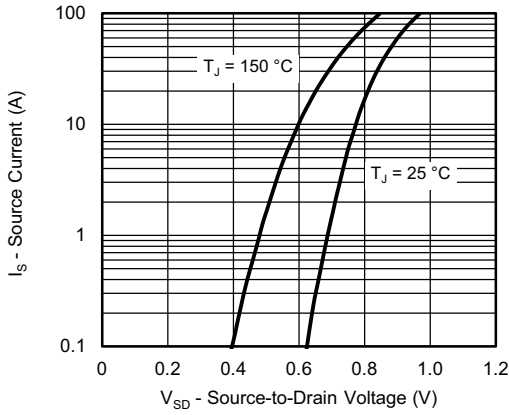
Gate Charge



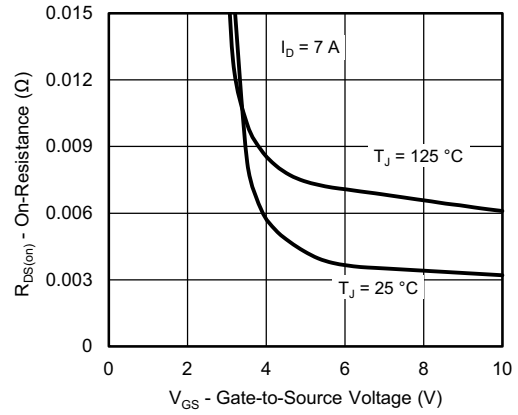
On-Resistance vs. Junction Temperature



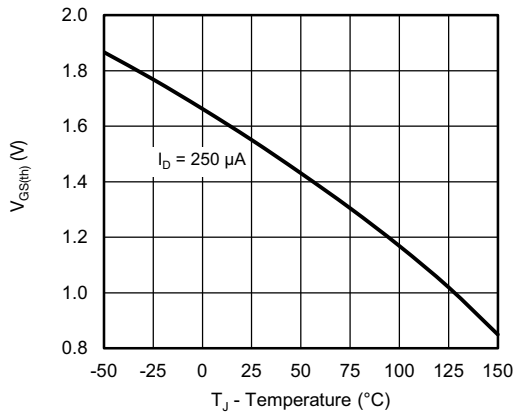
CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



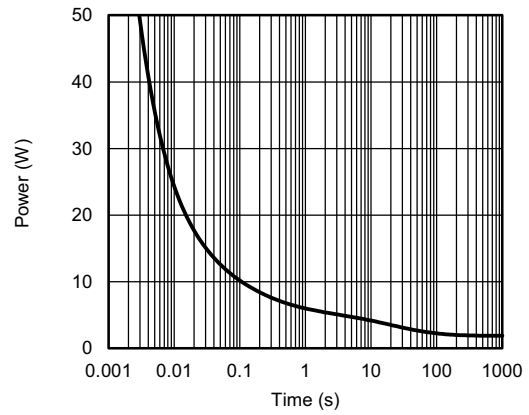
Source-Drain Diode Forward Voltage



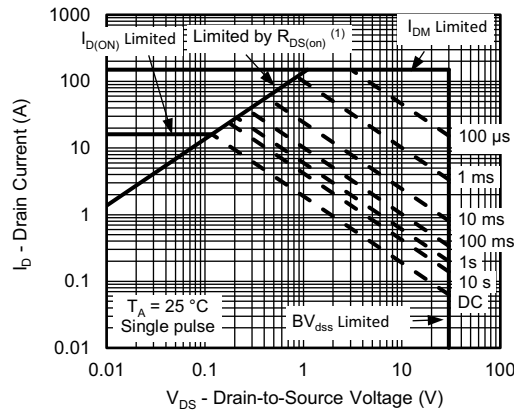
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage



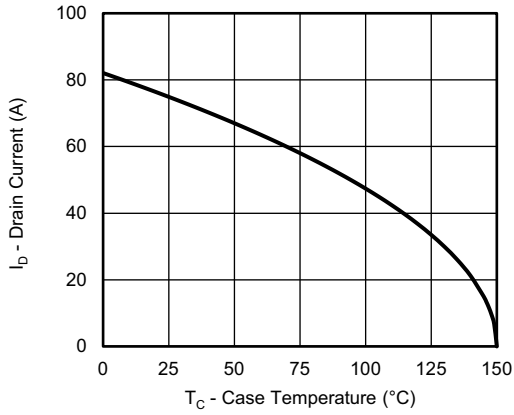
Single Pulse Power, Junction-to-Ambient



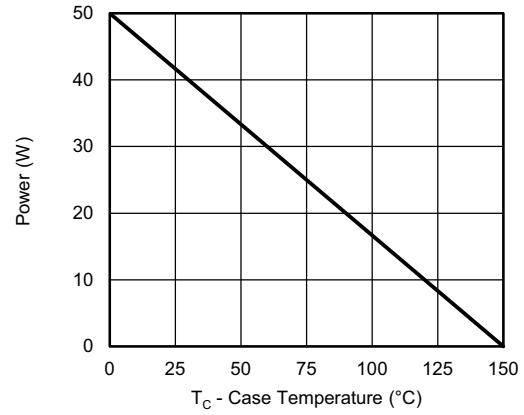
Safe Operating Area, Junction-to-Ambient



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



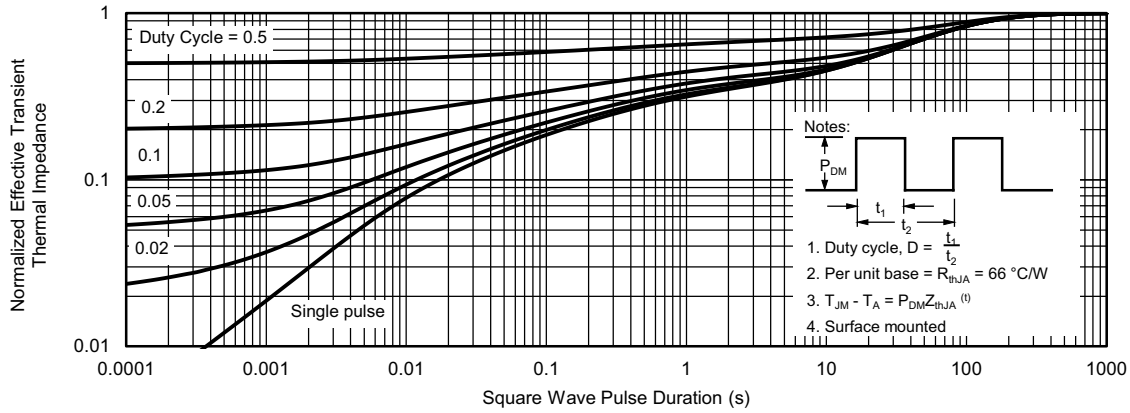
Power, Junction-to-Case

Note

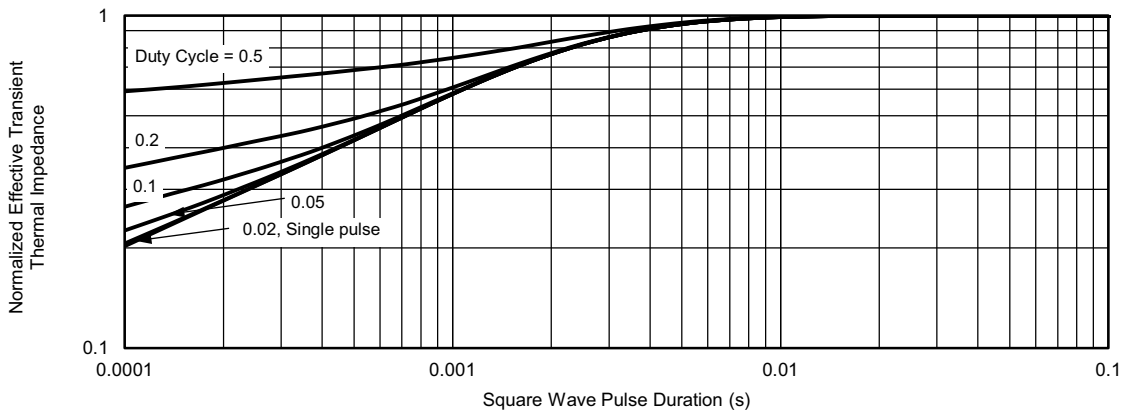
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-1 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

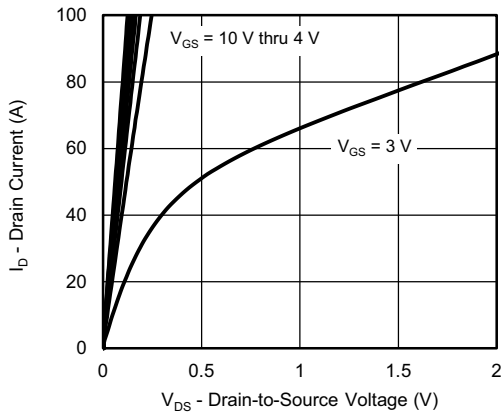


Normalized Thermal Transient Impedance, Junction-to-Ambient

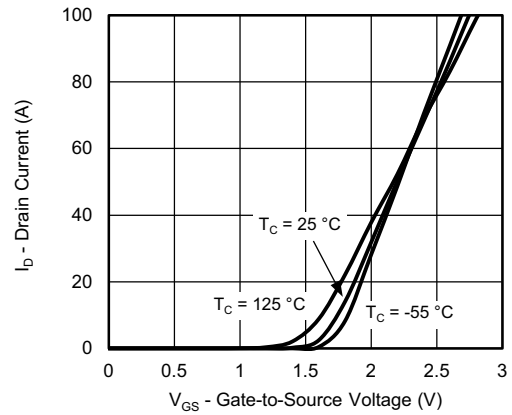


Normalized Thermal Transient Impedance, Junction-to-Case

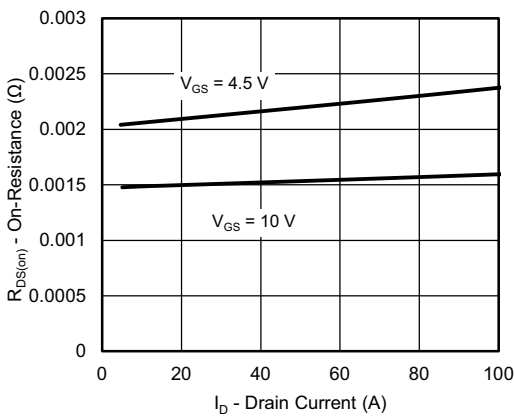
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



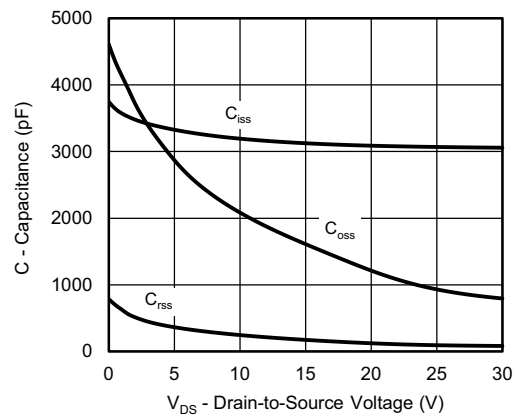
Output Characteristics



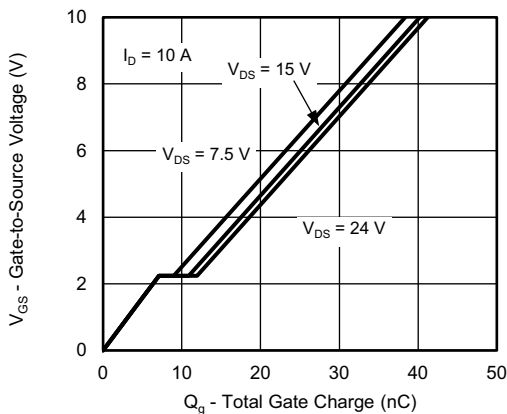
Transfer Characteristics



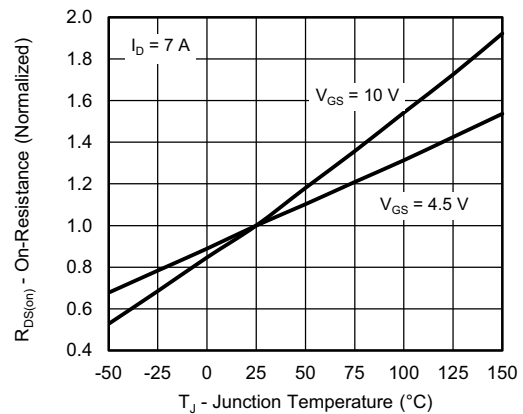
On-Resistance vs. Drain Current



Capacitance



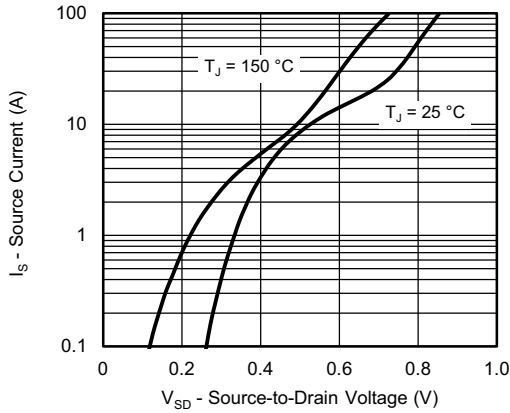
Gate Charge



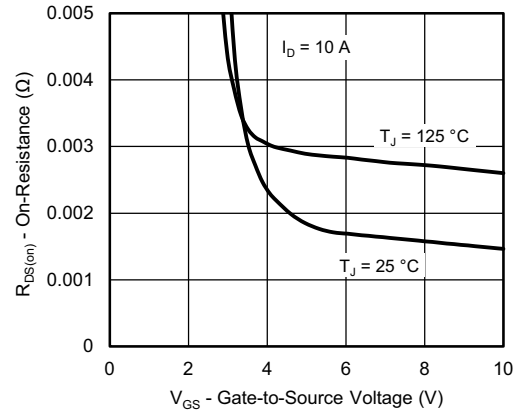
On-Resistance vs. Junction Temperature



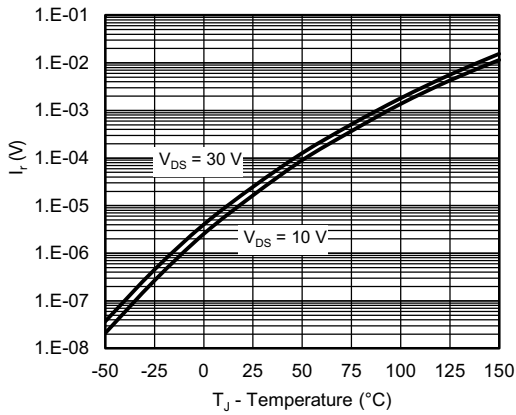
CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



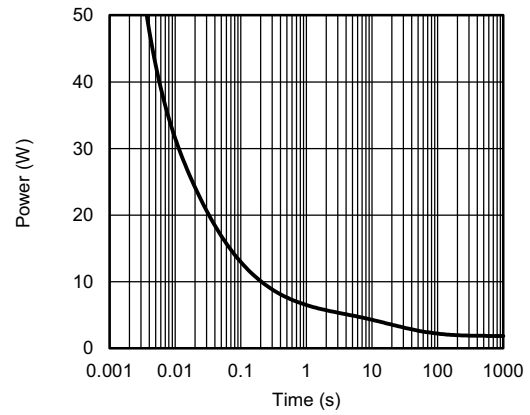
Source-Drain Diode Forward Voltage



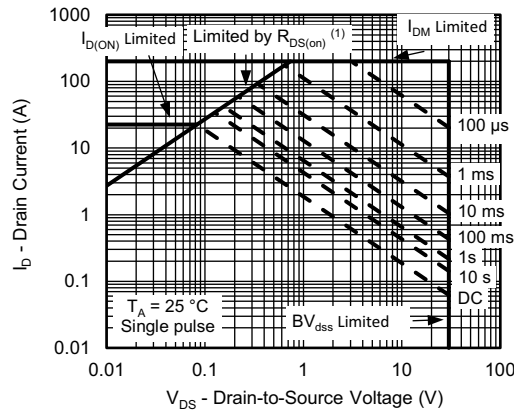
On-Resistance vs. Gate-to-Source Voltage



Reverse Current (Schottky)



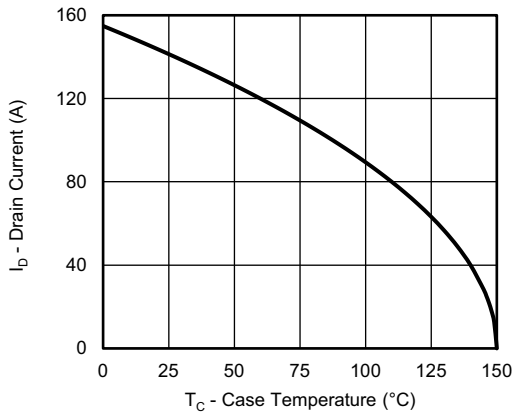
Single Pulse Power, Junction-to-Ambient



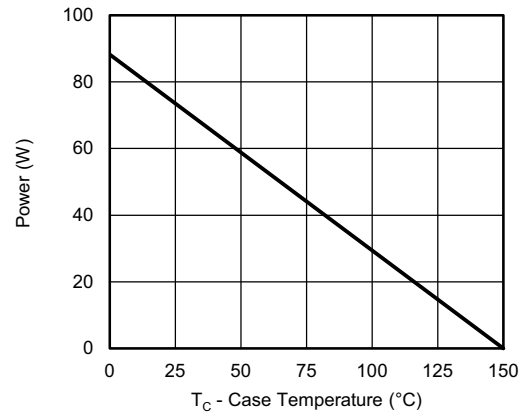
Safe Operating Area, Junction-to-Ambient



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating ^a



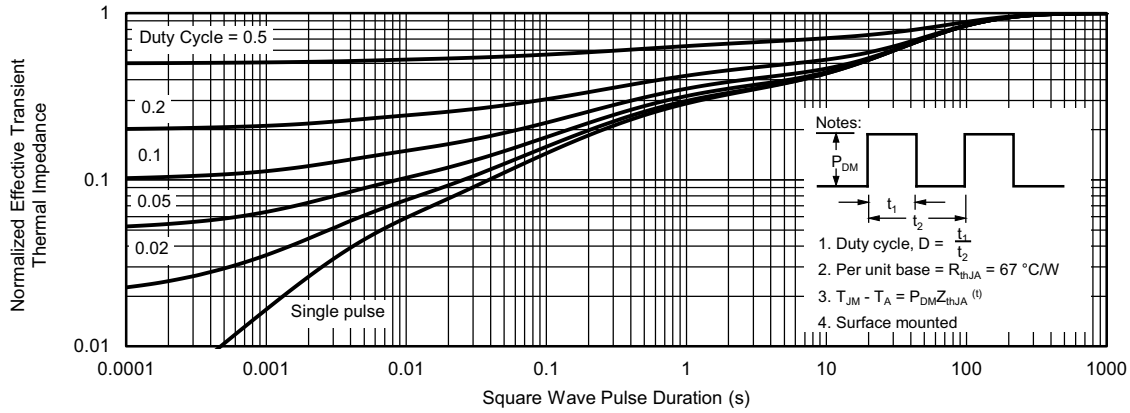
Power, Junction-to-Case

Note

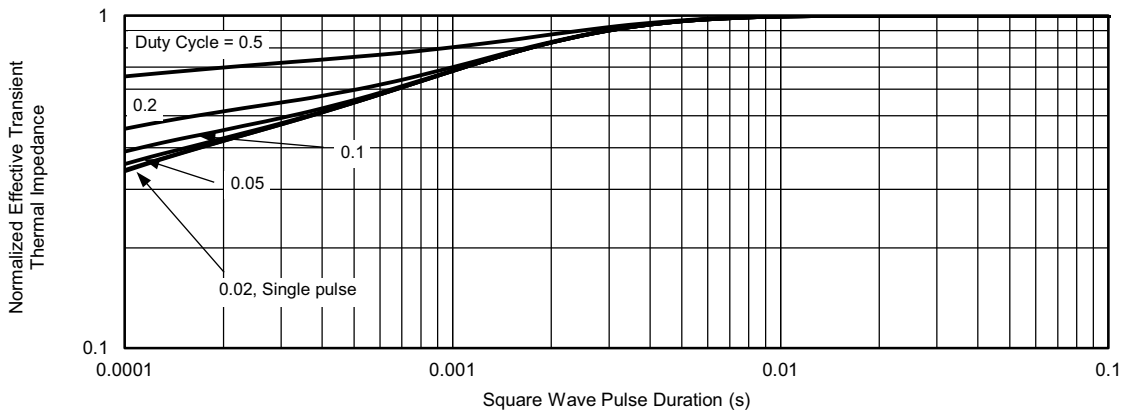
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit



CHANNEL-2 TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



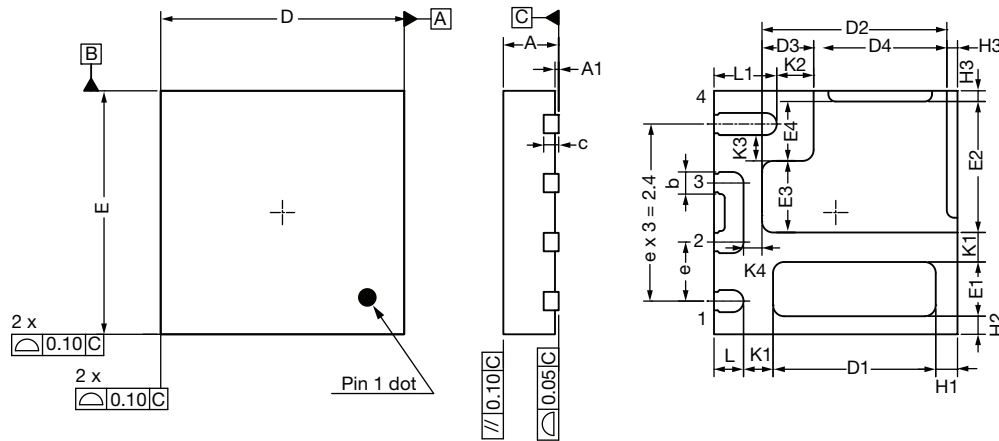
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?76288.

PowerPAIR® 3 x 3F Case Outline



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.028	0.030	0.032
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.20 ref.			0.008 ref.		
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.20	2.25	0.085	0.087	0.089
D2	2.45	2.50	2.55	0.096	0.098	0.100
D3	0.65	0.70	0.75	0.026	0.028	0.030
D4	1.75	1.80	1.85	0.069	0.071	0.073
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	0.69	0.74	0.79	0.027	0.029	0.031
E2	1.73	1.78	1.93	0.068	0.070	0.072
E3	0.92	0.97	1.02	0.036	0.038	0.040
E4	0.76	0.81	0.86	0.030	0.032	0.034
e	0.80 BSC			0.031 BSC		
K1	0.40 ref.			0.016 ref.		
K2	0.50 ref.			0.020 ref.		
K3	0.35 ref.			0.014 ref.		
K4	0.25 ref.			0.010 ref.		
H1	0.30 ref.			0.012 ref.		
H2	0.25 ref.			0.010 ref.		
H3	0.15 ref.			0.006 ref.		
L	0.35	0.40	0.45	0.014	0.016	0.018
L1	0.80	0.85	0.90	0.031	0.033	0.035

T18-0135-Rev. A, 02-Apr-18
DWG: 6065

Notes

- (1) Use millimeters as the primary measurement
- (2) Dimensioning and tolerances conform to ASME Y14.5M - 1994
- (3) N is the number of terminals; Nd is the number of terminals in X-direction; Ne is the number of terminals in Y-direction
- (4) Dimension b applies to plated terminal and is measured between 0.20 mm and 0.25 mm from terminal tip
- (5) The pin # 1 identifier must be existed on the top surface of the package by using indentation mark or other feature of package body
- (6) Exact shape and size of this features is optional
- (7) Package warpage max. 0.08 mm
- (8) Applied only for terminals



Disclaimer

ALL PRODUCT, PRODUCT SPECIFICATIONS AND DATA ARE SUBJECT TO CHANGE WITHOUT NOTICE TO IMPROVE RELIABILITY, FUNCTION OR DESIGN OR OTHERWISE.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained in any datasheet or in any other disclosure relating to any product.

Vishay makes no warranty, representation or guarantee regarding the suitability of the products for any particular purpose or the continuing production of any product. To the maximum extent permitted by applicable law, Vishay disclaims (i) any and all liability arising out of the application or use of any product, (ii) any and all liability, including without limitation special, consequential or incidental damages, and (iii) any and all implied warranties, including warranties of fitness for particular purpose, non-infringement and merchantability.

Statements regarding the suitability of products for certain types of applications are based on Vishay's knowledge of typical requirements that are often placed on Vishay products in generic applications. Such statements are not binding statements about the suitability of products for a particular application. It is the customer's responsibility to validate that a particular product with the properties described in the product specification is suitable for use in a particular application. Parameters provided in datasheets and / or specifications may vary in different applications and performance may vary over time. All operating parameters, including typical parameters, must be validated for each customer application by the customer's technical experts. Product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein.

Except as expressly indicated in writing, Vishay products are not designed for use in medical, life-saving, or life-sustaining applications or for any other application in which the failure of the Vishay product could result in personal injury or death. Customers using or selling Vishay products not expressly indicated for use in such applications do so at their own risk. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay. Product names and markings noted herein may be trademarks of their respective owners.

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [MOSFET](#) category:

Click to view products by [Vishay](#) manufacturer:

Other Similar products are found below :

[614233C](#) [648584F](#) [IRFD120](#) [JANTX2N5237](#) [2N7000](#) [FCA20N60_F109](#) [FDZ595PZ](#) [2SK2545\(Q,T\)](#) [405094E](#) [423220D](#)
[TPCC8103,L1Q\(CM](#) [MIC4420CM-TR](#) [VN1206L](#) [614234A](#) [715780A](#) [NTNS3166NZT5G](#) [SSM6J414TU,LF\(T](#) [751625C](#)
[IPS70R2K0CEAKMA1](#) [BUK954R8-60E](#) [DMN3404LQ-7](#) [NTE6400](#) [SQJ402EP-T1-GE3](#) [2SK2614\(TE16L1,Q\)](#) [2N7002KW-FAI](#)
[DMN1017UCP3-7](#) [EFC2J004NUZTDG](#) [ECH8691-TL-W](#) [FCAB21350L1](#) [P85W28HP2F-7071](#) [DMN1053UCP4-7](#) [NTE221](#) [NTE2384](#)
[NTE2903](#) [NTE2941](#) [NTE2945](#) [NTE2946](#) [NTE2960](#) [NTE2967](#) [NTE2969](#) [NTE2976](#) [NTE455](#) [NTE6400A](#) [NTE2910](#) [NTE2916](#) [NTE2956](#)
[NTE2911](#) [TK10A80W,S4X\(S](#) [SSM6P69NU,LF](#) [DMP22D4UFO-7B](#)