Automotive N-Channel 30 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	30
$R_{DS(on)}$ (Ω) at V_{GS} = 4.5 V	0.065
$R_{DS(on)}$ (Ω) at V_{GS} = 2.5 V	0.095
I_D (A)	1.7
Configuration	Single

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

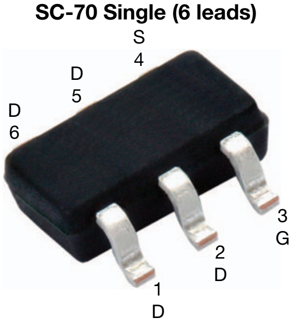
AUTOMOTIVE GRADE

Pb-free

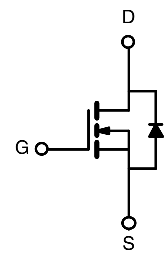
RoHS COMPLIANT

HALOGEN FREE

SOT-363
SC-70 Single (6 leads)



Top View



N-Channel MOSFET

Marking Code: 9O

ORDERING INFORMATION	
Package	SC-70
Lead (Pb)-free and Halogen-free	SQ1470AEH-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current [a]	T_C = 25 °C	I_D	1.7	A
	T_C = 125 °C		1.7	
Continuous Source Current (Diode Conduction) [a]		I_S	1.7	
Pulsed Drain Current [b]		I_{DM}	6.7	
Single Pulse Avalanche Current	L = 0.1 mH	I_{AS}	10	
Single Pulse Avalanche Energy		E_{AS}	5	mJ
Maximum Power Dissipation [b]	T_C = 25 °C	P_D	3.3	W
	T_C = 125 °C		1.1	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +175	°C

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount [c]	R_{thJA}	125	°C/W
Junction-to-Foot (Drain)		R_{thJF}	45	

Notes

a. Package limited.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
c. When mounted on 1" square PCB (FR4 material).

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SPECIFICATIONS (T_C = 25 °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA		30	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA		0.6	1	1.6	
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 12 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V	V_{DS} = 30 V	-	-	1	μA
		V_{GS} = 0 V	V_{DS} = 30 V, T_J = 125 °C	-	-	50	
		V_{GS} = 0 V	V_{DS} = 30 V, T_J = 175 °C	-	-	150	
On-State Drain Current [a]	$I_{D(on)}$	V_{GS} = 4.5 V	V_{DS} ≥ 5 V	5	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = 4.5 V	I_D = 4.2 A	-	0.045	0.065	Ω
		V_{GS} = 4.5 V	I_D = 3.8 A, T_J = 125 °C	-	-	0.097	
		V_{GS} = 4.5 V	I_D = 3.8 A, T_J = 175 °C	-	-	0.115	
		V_{GS} = 2.5 V	I_D = 4.2 A	-	0.060	0.095	
Forward Transconductance [b]	g_{fs}	V_{DS} = 15 V, I_D = 1.7 A		-	14	-	S
Dynamic [b]							
Input Capacitance	C_{iss}	V_{GS} = 0 V	V_{DS} = 15 V, f = 1 MHz	-	350	450	pF
Output Capacitance	C_{oss}			-	65	80	
Reverse Transfer Capacitance	C_{rss}			-	30	40	
Total Gate Charge [c]	Q_g	V_{GS} = 4.5 V	V_{DS} = 15 V, I_D = 4.2 A	-	4.2	5.2	nC
Gate-Source Charge	Q_{gs}			-	1.1	-	
Gate-Drain Charge [c]	Q_{gd}			-	0.7	-	
Gate Resistance	R_g	f = 1 MHz		1.9	3.8	5.7	Ω
Turn-On Delay Time [c]	$t_{d(on)}$	V_{DD} = 15 V, R_L = 3.9 Ω I_D ≅ 4.2 A, V_{GEN} = 4.5 V, R_g = 1 Ω		-	10	-	ns
Rise Time [c]	t_r			-	13	-	
Turn-Off Delay Time [c]	$t_{d(off)}$			-	14	-	
Fall Time [c]	t_f			-	8	-	
Source-Drain Diode Ratings and Characteristics [b]							
Pulsed Current [a]	I_{SM}			-	-	11	A
Forward Voltage	V_{SD}	I_F = 1.7 A, V_{GS} = 0 V		-	0.7	1.1	V

Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.
c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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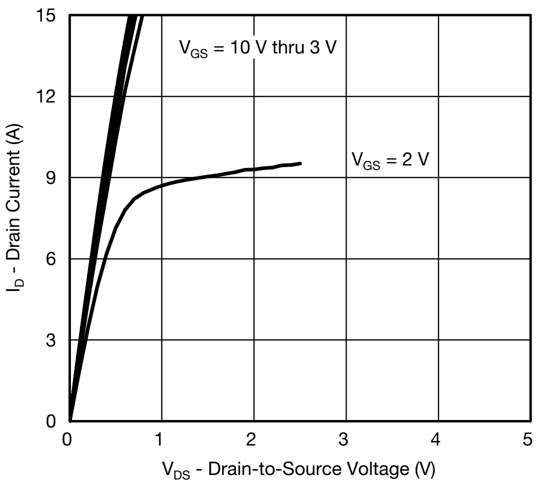
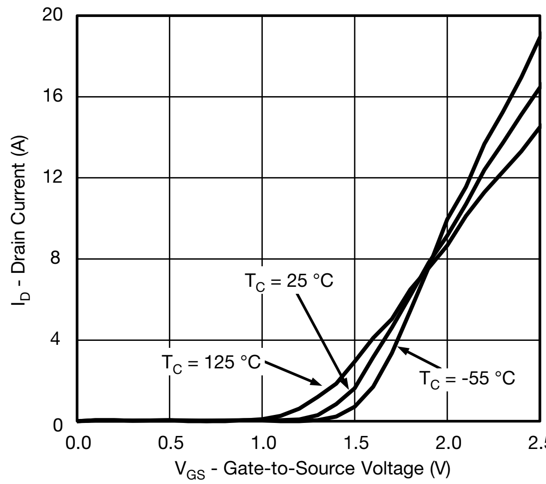
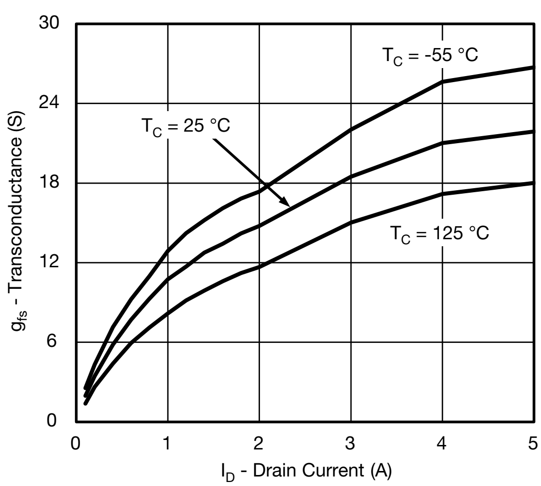
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



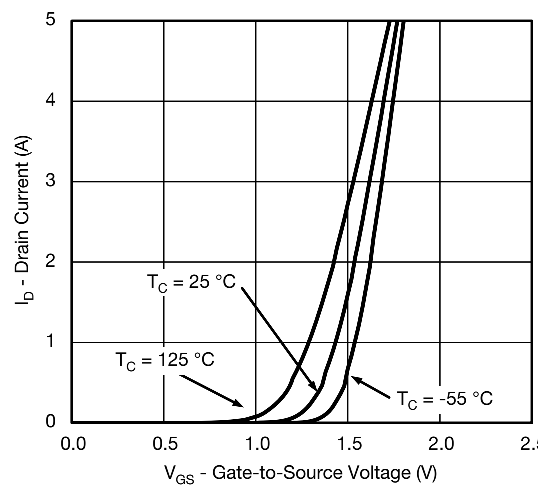
Output Characteristics



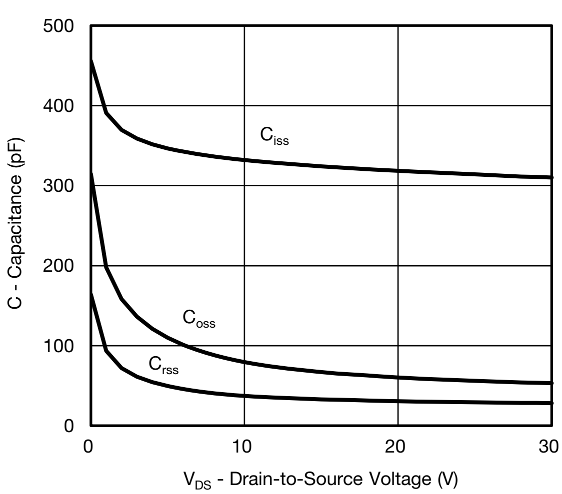
Transfer Characteristics



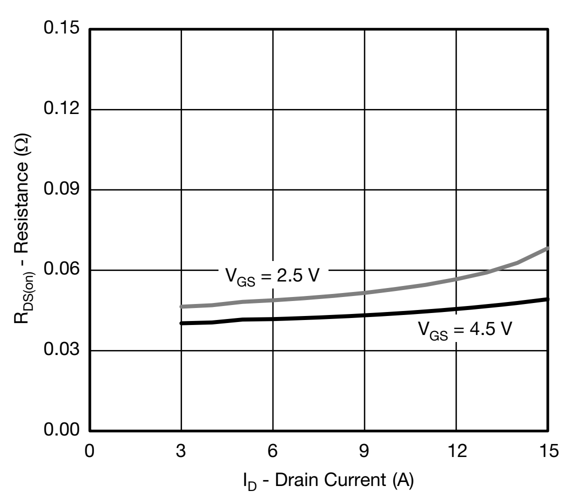
Transconductance



Transfer Characteristics



Capacitance



On-Resistance vs. Drain Current

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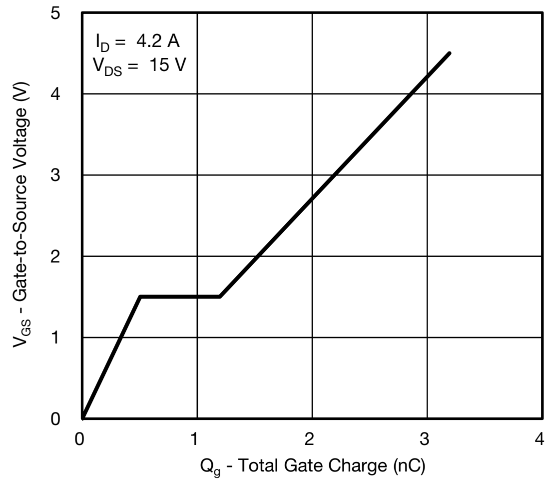
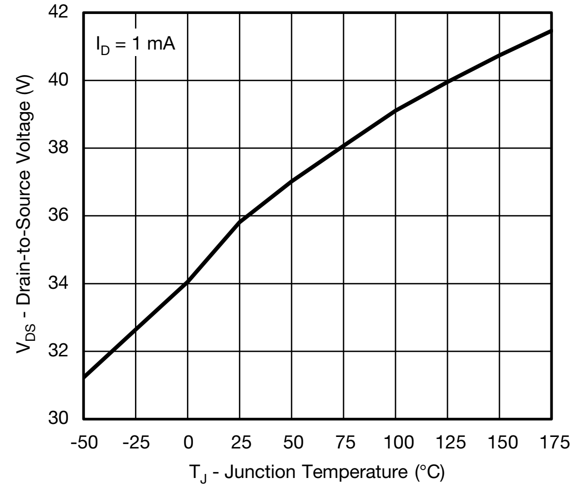
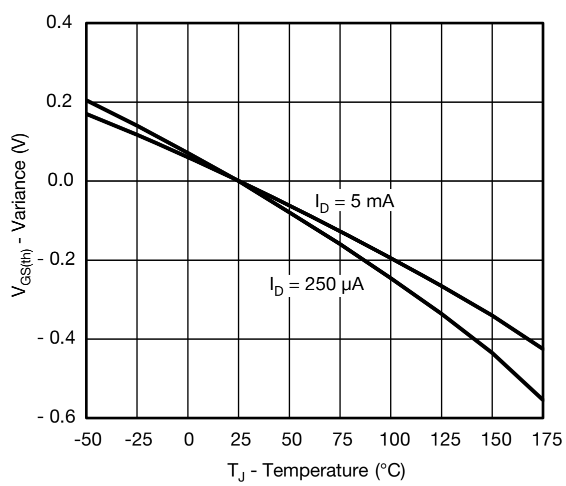
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



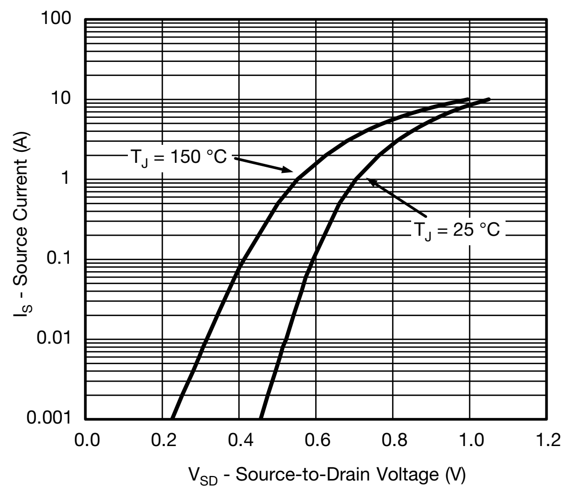
Gate Charge



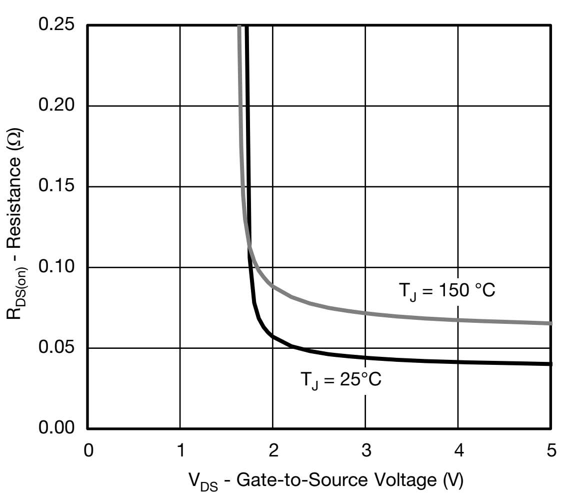
Drain Source Breakdown vs. Junction Temperature



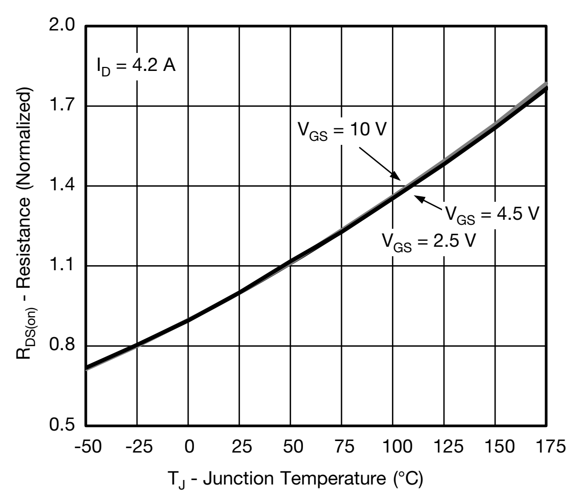
Threshold Voltage



Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



On-Resistance vs. Junction Temperature

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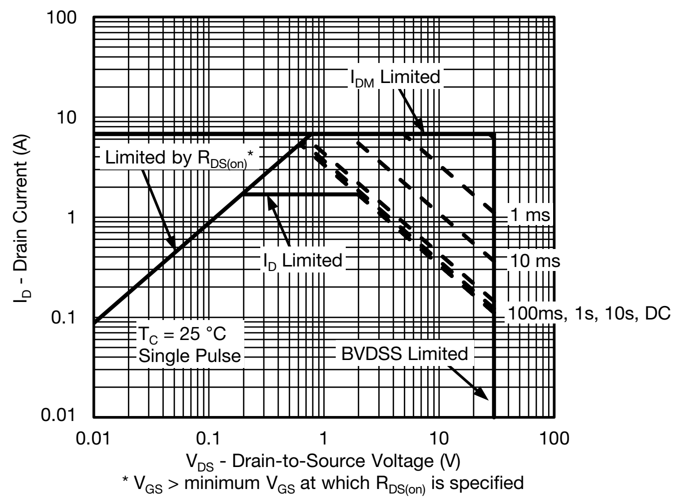
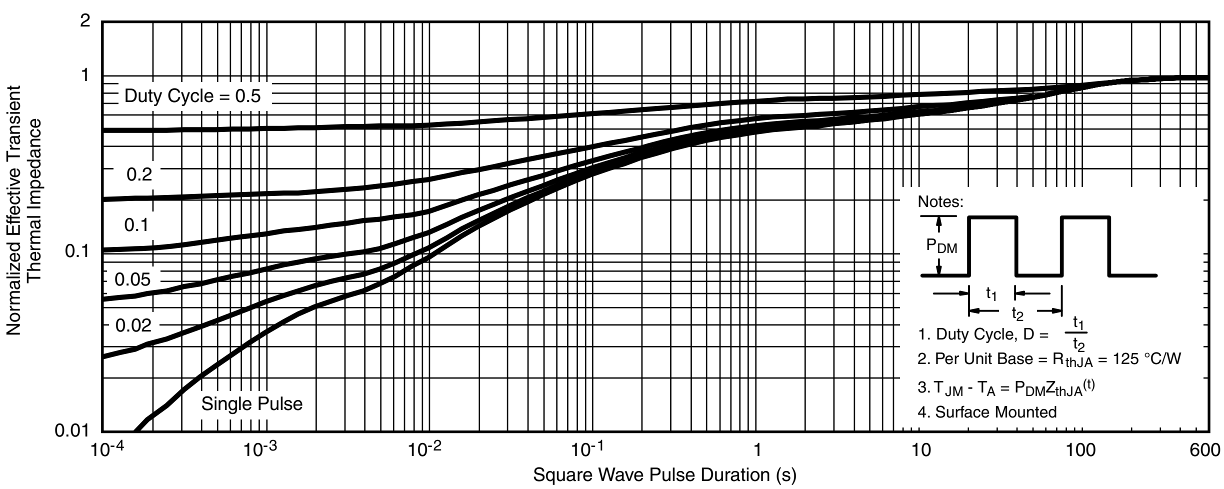
THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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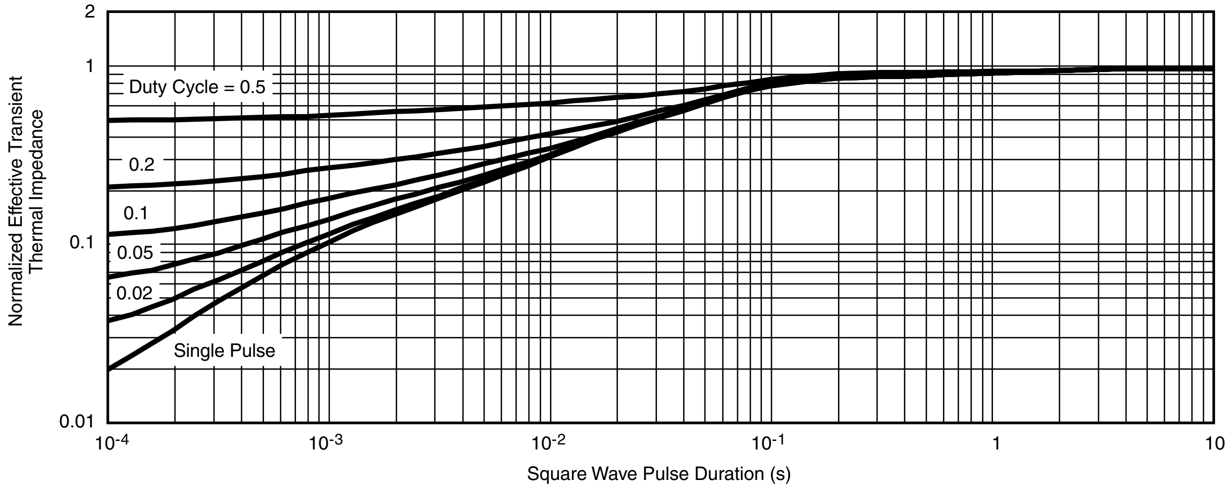
THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

Note

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

  are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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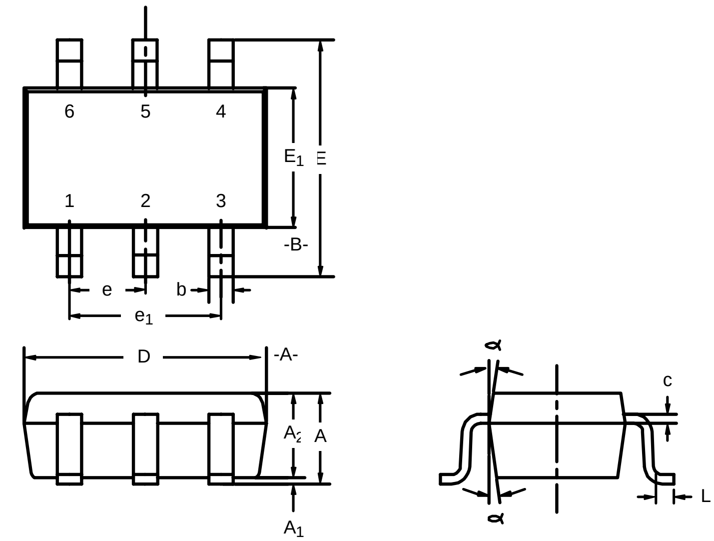
SC-70: 6-LEADS



Dim	MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max
A	0.90	–	1.10	0.035	–	0.043
A_1	–	–	0.10	–	–	0.004
A_2	0.80	–	1.00	0.031	–	0.039
b	0.15	–	0.30	0.006	–	0.012
c	0.10	–	0.25	0.004	–	0.010
D	1.80	2.00	2.20	0.071	0.079	0.087
E	1.80	2.10	2.40	0.071	0.083	0.094
E_1	1.15	1.25	1.35	0.045	0.049	0.053
e	0.65BSC			0.026BSC		
e_1	1.20	1.30	1.40	0.047	0.051	0.055
L	0.10	0.20	0.30	0.004	0.008	0.012
α	7°Nom			7°Nom		
ECN: S-03946—Rev. B, 09-Jul-01 DWG: 5550						

Single-Channel LITTLE FOOT® SC-70 6-Pin MOSFET Copper Leadframe Version Recommended Pad Pattern and Thermal Performance

INTRODUCTION

The new single 6-pin SC-70 package with a copper leadframe enables improved on-resistance values and enhanced thermal performance as compared to the existing 3-pin and 6-pin packages with Alloy 42 leadframes. These devices are intended for small to medium load applications where a miniaturized package is required. Devices in this package come in a range of on-resistance values, in n-channel and p-channel versions. This technical note discusses pin-outs, package outlines, pad patterns, evaluation board layout, and thermal performance for the single-channel version.

BASIC PAD PATTERNS

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286) for the basic pad layout and dimensions. These pad patterns are sufficient for the low to medium power applications for which this package is intended. Increasing the drain pad pattern yields a reduction in thermal resistance and is a preferred footprint. The availability of four drain leads rather than the traditional single drain lead allows a better thermal path from the package to the PCB and external environment.

PIN-OUT

Figure 1 shows the pin-out description and Pin 1 identification.The pin-out of this device allows the use of four pins as drain leads, which helps to reduce on-resistance and junction-to-ambient thermal resistance.

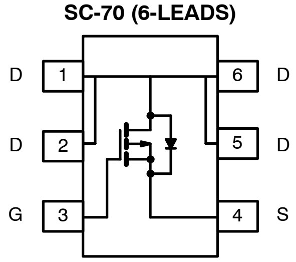


FIGURE 1.

For package dimensions see outline drawing SC-70 (6-Leads) (http://www.vishay.com/doc?71154)

EVALUATION BOARDS — SINGLE SC70-6

The evaluation board (EVB) measures 0.6 inches by 0.5 inches. The copper pad traces are the same as in Figure 2. The board allows examination from the outer pins to 6-pin DIP connections, permitting test sockets to be used in evaluation testing. See Figure 3.

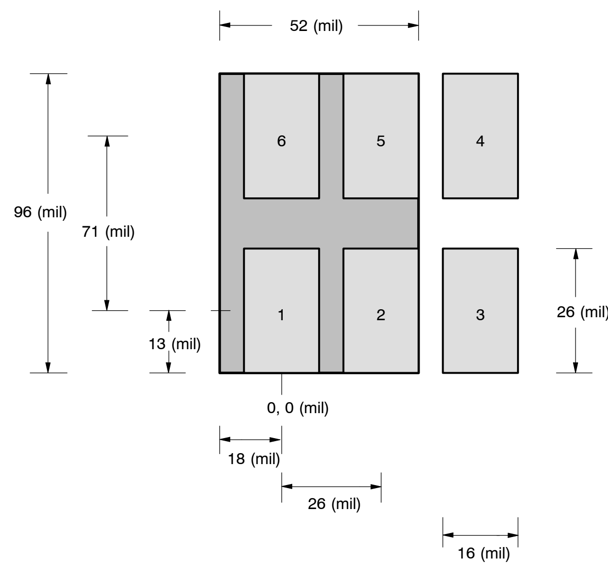


FIGURE 2. SC-70 (6 leads) Single

The thermal performance of the single 6-pin SC-70 has been measured on the EVB, comparing both the copper and Alloy 42 leadframes. This test was first conducted on the traditional Alloy 42 leadframe and was then repeated using the 1-inch^2 PCB with dual-side copper coating.

Front of Board SC70-6 Back of Board SC70-6

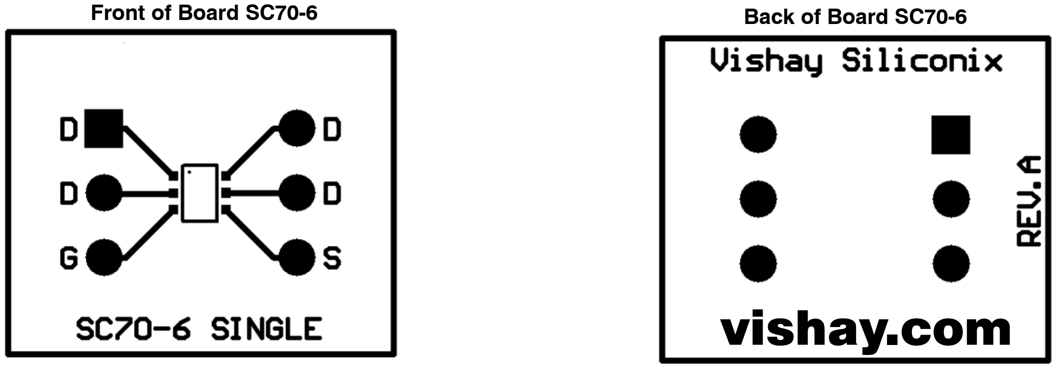


FIGURE 3.

THERMAL PERFORMANCE

Junction-to-Foot Thermal Resistance (Package Performance)

The junction to foot thermal resistance is a useful method of comparing different packages thermal performance.

A helpful way of presenting the thermal performance of the 6-Pin SC-70 copper leadframe device is to compare it to the traditional Alloy 42 version.

Thermal performance for the 6-pin SC-70 measured as junction-to-foot thermal resistance, where the "foot" is the drain lead of the device at the bottom where it meets the PCB. The junction-to-foot thermal resistance is typically 40°C/W in the copper leadframe and 163°C/W in the Alloy 42 leadframe — a four-fold improvement. This improved performance is obtained by the enhanced thermal conductivity of copper over Alloy 42.

Power Dissipation

The typical $R\theta_{JA}$ for the single 6-pin SC-70 with copper leadframe is 103°C/W steady-state, compared with 212°C/W for the Alloy 42 version. The figures are based on the 1-inch^2 FR4 test board. The following example shows how the thermal resistance impacts power dissipation for the two different leadframes at varying ambient temperatures.

ALLOY 42 LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^oC - 25^oC}{212^oC/W}$	$P_D = \frac{150^oC - 25^oC}{212^oC/W}$
$P_D =$ 590 mW	$P_D =$ 425 mW

COOPER LEADFRAME	
Room Ambient 25 °C	Elevated Ambient 60 °C
$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$	$P_D = \frac{T_{J(max)} - T_A}{R\theta_{JA}}$
$P_D = \frac{150^oC - 25^oC}{124^oC/W}$	$P_D = \frac{150^oC - 60^oC}{124^oC/W}$
$P_D =$ 1.01 W	$P_D =$ 726 mW

As can be seen from the calculations above, the compact 6-pin SC-70 copper leadframe LITTLE FOOT power MOSFET can handle up to 1 W under the stated conditions.

Testing

To further aid comparison of copper and Alloy 42 leadframes, Figure 5 illustrates single-channel 6-pin SC-70 thermal performance on two different board sizes and two different pad patterns. The measured steady-state values of $R\theta_{JA}$ for the two leadframes are as follows:

LITTLE FOOT 6-PIN SC-70		
	Alloy 42	Copper
1) Minimum recommended pad pattern on the EVB board V (see Figure 3.	329.7°C/W	208.5°C/W
2) Industry standard 1-inch^2 PCB with maximum copper both sides.	211.8°C/W	103.5°C/W

The results indicate that designers can reduce thermal resistance ($R\theta_{JA}$) by 36% simply by using the copper leadframe device rather than the Alloy 42 version. In this example, a 121°C/W reduction was achieved without an increase in board area. If increasing in board size is feasible, a further 105°C/W reduction could be obtained by utilizing a 1-inch^2 square PCB area.

The copper leadframe versions have the following suffix:

Single:	Si14xxEDH
Dual:	Si19xxEDH
Complementary:	Si15xxEDH

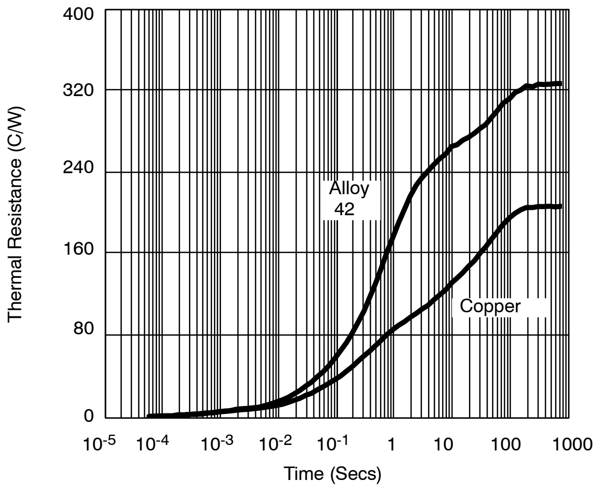


FIGURE 4. Leadframe Comparison on EVB

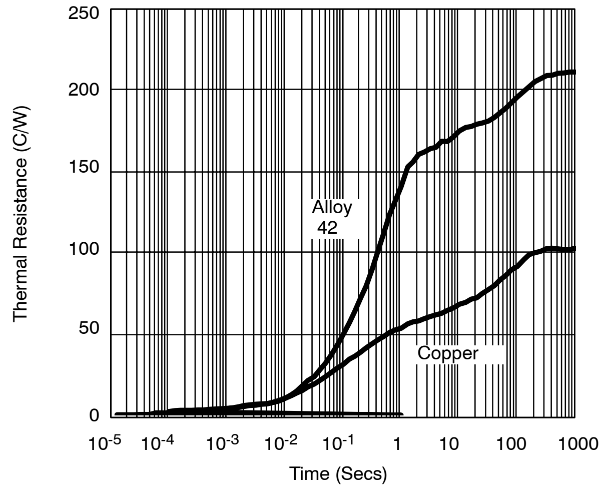
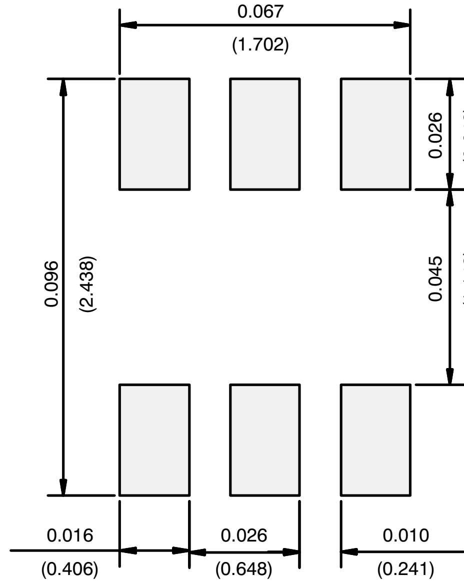


FIGURE 5. Leadframe Comparison on Alloy 42 1-inch^2 PCB

RECOMMENDED MINIMUM PADS FOR SC-70: 6-Lead



Recommended Minimum Pads
Dimensions in Inches/(mm)

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