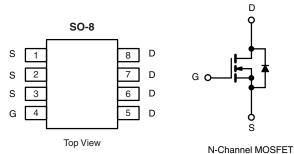
## SQ4840EY



**Vishay Siliconix** 

## Automotive N-Channel 40 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY					
V <sub>DS</sub> (V)	40				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 V$	0.009				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 V$	0.012				
I <sub>D</sub> (A)	20.7				
Configuration	Single				



#### **FEATURES**

- Halogen-free According to IEC 61249-2-21
  Definition
- TrenchFET<sup>®</sup> Power MOSFET
- AEC-Q101 Qualified
- 100 % R<sub>q</sub> and UIS Tested
- Compliant to RoHS Directive 2002/95/EC



ROHS COMPLIANT HALOGEN FREE

ORDERING INFORMATION				
Package	SO-8			
Lead (Pb)-free and Halogen-free	SQ4840EY-T1-GE3			

<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_C = 25 \degree C$ , unless otherwise noted)					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V <sub>DS</sub>	40		
Gate-Source Voltage		V <sub>GS</sub>	± 20	V	
Continuous Drain Current	T <sub>C</sub> = 25 °C	1	20.7		
	T <sub>C</sub> = 125 °C	I <sub>D</sub>	12		
Continuous Source Current (Diode Conduction)		I <sub>S</sub>	6.5	А	
Pulsed Drain Current <sup>a</sup>		I <sub>DM</sub>	82		
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	30		
Single Pulse Avalanche Energy		E <sub>AS</sub>	45	mJ	
Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> = 25 °C	D	7.1	W	
	T <sub>C</sub> = 125 °C	P <sub>D</sub>	2.4	vv	
Operating Junction and Storage Temperature Ra	nge	TJ, Tstg	- 55 to + 175	°C	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	LIMIT	UNIT	
Junction-to-Ambient	PCB Mount <sup>b</sup>	R <sub>thJA</sub>	85	°C/W	
Junction-to-Foot (Drain)		R <sub>thJF</sub>	21	0/10	

Notes

a. Pulse test; pulse width  $\leq 300~\mu s,~duty~cycle \leq 2~\%.$ 

b. When mounted on 1" square PCB (FR-4 material).

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**SQ4840EY** 

<b>SPECIFICATIONS</b> ( $T_C = 25$ °C, unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V <sub>DS</sub>	$V_{GS} = 0$ , $I_D = 250 \ \mu A$		40	-	-	v
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$		2.0	2.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$V_{DS} = 0 V, V_{GS} = \pm 20 V$		-	± 100	nA
		$V_{GS} = 0 V$	$V_{DS} = 40 V$	-	-	1.0	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS} = 40 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$	-	-	50	μA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 40 V, T <sub>J</sub> = 175 °C	-	-	150	
On-State Drain Currenta	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	30	-	-	Α
		$V_{GS} = 10 V$	I <sub>D</sub> = 14 A	-	0.0075	0.009	
Durain Source On State Desistence	Р	$V_{GS} = 10 \text{ V}$	I <sub>D</sub> = 14 A, T <sub>C</sub> = 125 °C	-	-	0.014	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	$V_{GS} = 10 V$	I <sub>D</sub> = 14 A, T <sub>C</sub> = 175 °C	-	-	0.018	Ω
		$V_{GS} = 4.5 V$	I <sub>D</sub> = 12 A	-	0.010	0.012	
Forward Transconductanceb	9 <sub>fs</sub>	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 14 A	-	45	-	S
Dynamic <sup>b</sup>		·					•
Input Capacitance	C <sub>iss</sub>		V <sub>GS</sub> = 0 V V <sub>DS</sub> = 20 V, f = 1 MHz	-	1950	2440	pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V V <sub>DS</sub>		-	505	630	
Reverse Transfer Capacitance	C <sub>rss</sub>			-	220	280	
Total Gate Charge <sup>c</sup>	Qg			-	41	62	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	V <sub>GS</sub> = 10 V	$_{\rm S}$ = 10 V V <sub>DS</sub> = 20 V, I <sub>D</sub> = 14 A	-	5.5	-	nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	8.7	-	
Gate Resistance	Rg	f = 1 MHz		0.2	-	1.6	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	14	21	
Rise Time <sup>c</sup>	t <sub>r</sub>	V <sub>DD</sub>	$V_{DD} = 20 \text{ V}, \text{ R}_{\text{I}} = 20 \Omega$		11	17	- ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong 1 \text{ A}, V_{\text{GEN}} = 10 \text{ V}, R_g = 6 \Omega$		-	45	68	
Fall Time <sup>c</sup>	t <sub>f</sub>			-	17	26	
Source-Drain Diode Ratings and Characteristics <sup>b</sup>							
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	82	A
Forward Voltage	V <sub>SD</sub>	I <sub>F</sub> :	$I_{\rm F} = 2.8  \text{A},  V_{\rm GS} = 0$		0.75	1.1	V

Notes

a. Pulse test; pulse width  $\leq 300~\mu s,$  duty cycle  $\leq 2~\%.$ 

b. Guaranteed by design, not subject to production testing.

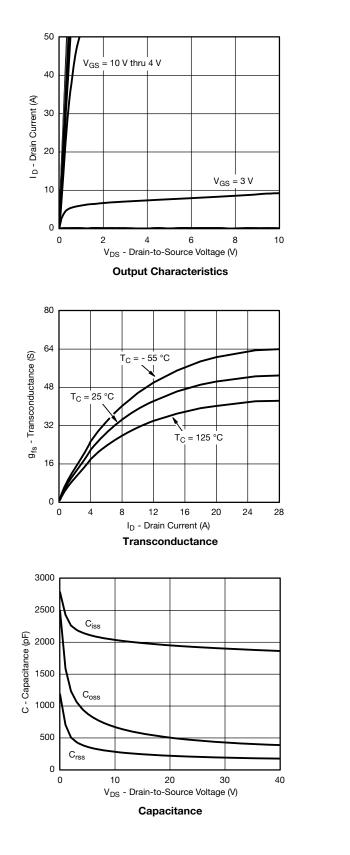
c. Independent of operating temperature.

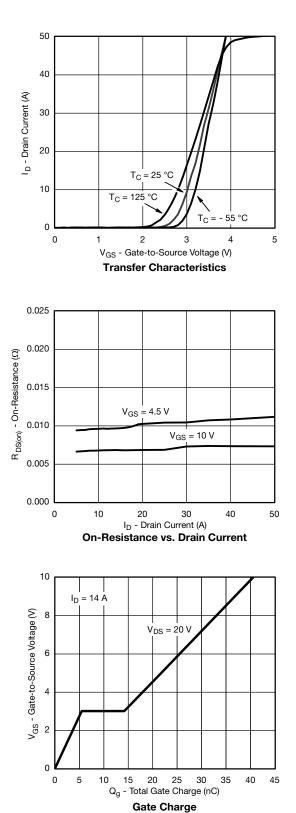
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2



#### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)





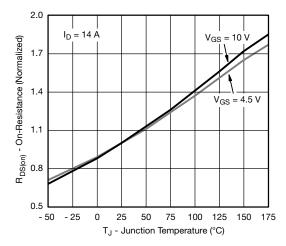
S11-2109 Rev. D, 31-Oct-11

3

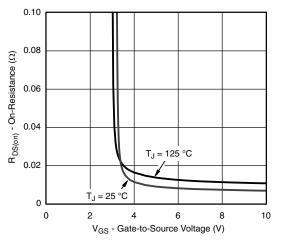
Document Number: 68669



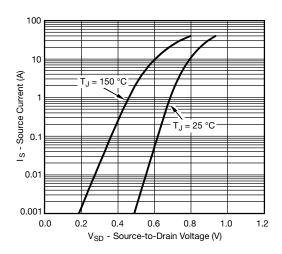
#### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



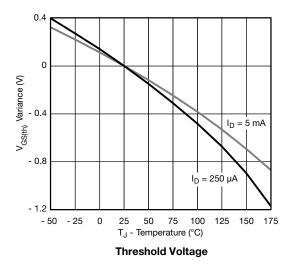
**On-Resistance vs. Junction Temperature** 

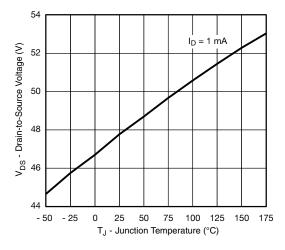


**On-Resistance vs. Gate-to-Source Voltage** 



Source Drain Diode Forward Voltage





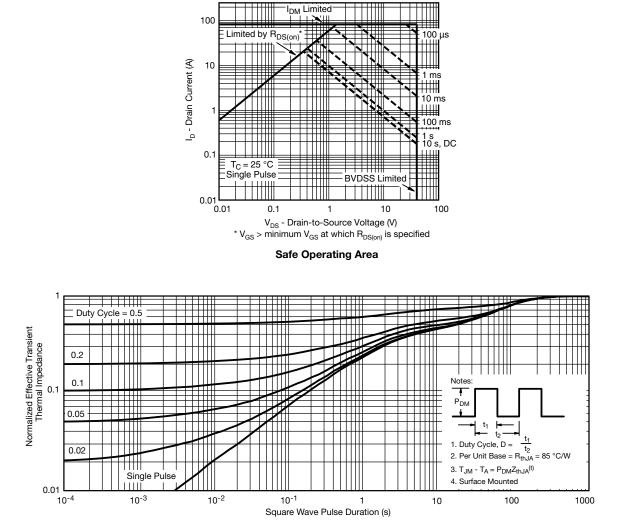
Drain Source Breakdown vs. Junction Temperature

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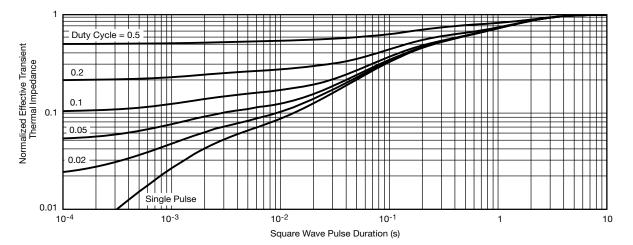
#### **THERMAL RATINGS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



#### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Foot

#### Note

• The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Foot (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?68669">www.vishay.com/ppg?68669</a>.



# Package Information

Vishay Siliconix

# SOIC (NARROW): 8-LEAD JEDEC Part Number: MS-012





	MILLIM	IETERS	INCHES		
DIM	Min	Мах	Min	Max	
A	1.35	1.75	0.053	0.069	
A <sub>1</sub>	0.10	0.20	0.004	0.008	
В	0.35	0.51	0.014	0.020	
С	0.19	0.25	0.0075	0.010	
D	4.80	5.00	0.189	0.196	
E	3.80	4.00	0.150	0.157	
е	1.27	BSC	0.050 BSC		
н	5.80	6.20	0.228	0.244	
h	0.25	0.50	0.010	0.020	
L	0.50	0.93	0.020	0.037	
q	0°	8°	0°	8°	
S	0.44	0.64	0.018	0.026	
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498					

## **Application Note 826**

Vishay Siliconix



**RECOMMENDED MINIMUM PADS FOR SO-8** 



Recommended Minimum Pads Dimensions in Inches/(mm)

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