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Vishay Siliconix

Automotive Dual N-Channel 20 V (D-S) 175 °C MOSFETs

PRODUCT SUMMARY					
	N-CHANNEL 1	N-CHANNEL 2			
V _{DS} (V)	20 20				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0088 0.0037				
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0124 0.0050				
I _D (A)	20 60				
Configuration	Dual N				
Package	PowerPAK SO-8L Dual Asymmetric				

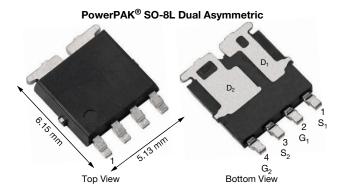
FEATURES

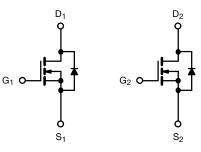
- TrenchFET® power MOSFET
- AEC-Q101 qualified d
- 100 % R_q and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912





ROHS COMPLIANT HALOGEN FREE





N-Channel 1 MOSFET

N-Channel 2 MOSFET

ABSOLUTE MAXIMUM RATINGS (To	_C = 25 °C, unless	otherwise r	oted)		
PARAMETER		SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Drain-Source Voltage		V _{DS}	20	20	V
Gate-Source Voltage		V_{GS}	±	20	V
Continuous Drain Current ^a	T _C = 25 °C	1	20	60	
Continuous Drain Current "	T _C = 125 °C	I _D	20	50	
Continuous Source Current (Diode Conduction)		I _S	20 ^a	44	Α
Pulsed Drain Current ^b		I _{DM}	80	180	
Single Pulse Avalanche Current	l 0.1 mll	I _{AS}	22	40	
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	24.2	80	mJ
Maximum Power Dissipation b	T _C = 25 °C	Б	27	48	W
iviaximum rower Dissipation 5	T _C = 125 °C	P_{D}	9	16	VV
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175		
Soldering Recommendations (Peak Temperature) e, f			2	60	°C

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	N-CHANNEL 1	N-CHANNEL 2	UNIT
Junction-to-Ambient	PCB mount c	R_{thJA}	85	85	°C/W
Junction-to-Case (Drain)		R_{thJC}	5.5	3.1	C/VV

Notes

- a. Package limited.
- b. Pulse test; pulse width $\leq 300 \,\mu\text{s}$, duty cycle $\leq 2 \,\%$.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.
- e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL		TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	
Static									
		V _{GS} =	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		20	-	_		
Drain-Source Breakdown Voltage	V_{DS}		= 0 V, I _D = 250 μA	N-Ch 2	20	-	-	İ	
		V _{DS} =	· V _{GS} , I _D = 250 μA	N-Ch 1	1	1.5	2	V	
Gate-Source Threshold Voltage	$V_{GS(th)}$	V _{DS} =	· V _{GS} , I _D = 250 μA	N-Ch 2	1	1.5	2		
		.,	21/1/	N-Ch 1	-	-	± 100	_	
Gate-Source Leakage	I _{GSS}	$V_{DS} =$	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	N-Ch 2	=	-	± 100	nA	
		V _{GS} = 0 V	V _{DS} = 20 V	N-Ch 1	-	-	1		
		V _{GS} = 0 V	V _{DS} = 20 V	N-Ch 2	-	-	1		
7 0		V _{GS} = 0 V	V _{DS} = 20 V, T _J = 125 °C	N-Ch 1	-	-	50		
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 20 V, T _J = 125 °C	N-Ch 2	-	-	50	μA	
		V _{GS} = 0 V	V _{DS} = 20 V, T _J = 175 °C	N-Ch 1	-	-	150		
		V _{GS} = 0 V	V _{DS} = 20 V, T _J = 175 °C	N-Ch 2	=	-	150		
0.01.0.10		V _{GS} = 10 V	V _{DS} ≥ 5 V	N-Ch 1	20	-	-		
On-State Drain Current a	I _{D(on)}	V _{GS} = 10 V	V _{DS} ≥ 5 V	N-Ch 2	30	-	-	A	
		V _{GS} = 10 V	I _D = 16 A	N-Ch 1	_	0.0074	0.0088		
		V _{GS} = 10 V	I _D = 20 A	N-Ch 2	-	0.0031	0.0037		
	R _{DS(on)}	V _{GS} = 10 V	I _D = 16 A, T _J = 125 °C	N-Ch 1	-	0.0110	-	Ω	
		V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	N-Ch 2	-	0.0036	-		
Drain-Source On-State Resistance ^a		V _{GS} = 10 V	I _D = 16 A, T _J = 175 °C	N-Ch 1	-	0.0124	-		
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	N-Ch 2	-	0.0063	-		
		V _{GS} = 4.5 V	I _D = 14 A	N-Ch 1	-	0.0095	0.0124		
		V _{GS} = 4.5 V	I _D = 19 A	N-Ch 2	-	0.0039	0.0050	:	
		V _{DS}	= 10 V, I _D = 10 A	N-Ch 1	-	55	-		
Forward Transconductance b	9 _{fs}	V _{DS}	= 10 V, I _D = 10 A	N-Ch 2	_	60	-	S	
Dynamic ^b		L							
		$V_{GS} = 0 V$	V _{DS} = 10 V, f = 1 MHz	N-Ch 1	-	723	975		
Input Capacitance	C_{iss}	V _{GS} = 0 V	V _{DS} = 10 V, f = 1 MHz	N-Ch 2	=	1937	2525		
0.1.10	-	V _{GS} = 0 V	V _{DS} = 10 V, f = 1 MHz	N-Ch 1	-	269	675	_	
Output Capacitance	C_{oss}	V _{GS} = 0 V	V _{DS} = 10 V, f = 1 MHz	N-Ch 2	-	655	870	pF	
		V _{GS} = 0 V	V _{DS} = 10 V, f = 1 MHz	N-Ch 1	-	112	340		
Reverse Transfer Capacitance	C_{rss}	V _{GS} = 0 V	V _{DS} = 10 V, f = 1 MHz	N-Ch 2	_	264	350		
		V _{GS} = 10 V	V _{DS} = 10 V, I _D = 20 A	N-Ch 1	-	12	18		
Total Gate Charge c	Q_g	V _{GS} = 10 V	$V_{DS} = 10 \text{ V}, I_{D} = 60 \text{ A}$	N-Ch 2	-	29	43		
	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 10 \text{ V}, I_{D} = 20 \text{ A}$	N-Ch 1	-	1.6	-	nC	
Gate-Source Charge c		V _{GS} = 10 V	V _{DS} = 10 V, I _D = 60 A	N-Ch 2	-	4.1	-	1	
0	_	V _{GS} = 10 V	V _{DS} = 10 V, I _D = 20 A	N-Ch 1	-	2.5	-		
Gate-Drain Charge ^c	Q _{gd}	V _{GS} = 10 V	V _{DS} = 10 V, I _D = 60 A	N-Ch 2	-	6	-		
	_			N-Ch 1	1.1	2.3	3.5		
Gate Resistance	R_g	f = 1 MHz		N-Ch 2	0.4	1	1.4	Ω	



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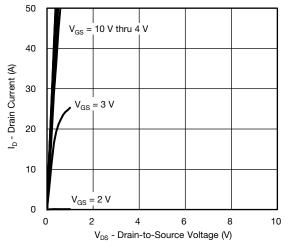
SPECIFICATIONS (T _C = 2	25 °C, unless o	therwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Turn On Delay Time C		$\begin{aligned} V_{DD} &= 6 \text{ V}, \text{ R}_L = 0.3 \Omega \\ I_D &\cong 20 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	N-Ch 1	-	4	6	
Turn-On Delay Time ^c	t _{d(on)}	$V_{DD} = 6 \text{ V}, \text{ R}_{L} = 0.1 \Omega$ $I_{D} \cong 60 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$	N-Ch 2	-	7	9	
Dies Time C		$\begin{aligned} V_{DD} &= 6 \text{ V}, \text{ R}_L = 0.3 \Omega \\ I_D &\cong 20 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	N-Ch 1	-	18	23	
Rise Time ^c	t _r -	$\begin{aligned} V_{DD} &= 6 \text{ V}, \text{ R}_L = 0.1 \Omega \\ I_D &\cong 60 \text{ A}, V_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	N-Ch 2	-	17	23	
Turn-Off Delay Time ^c		$\begin{aligned} V_{DD} &= 6 \text{ V}, \text{ R}_L = 0.3 \Omega \\ I_D &\cong 20 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	N-Ch 1	-	13	17	ns
	t _{d(off)}	$V_{DD} = 6 \text{ V}, \text{ R}_{L} = 0.1 \Omega$ $I_{D} \cong 60 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$	N-Ch 2	-	19	25	
Fall Time °		$\begin{aligned} V_{DD} &= 6 \text{ V}, \text{ R}_L = 0.3 \Omega \\ I_D &\cong 20 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega \end{aligned}$	N-Ch 1	-	13	17	
raii Tillie v	t _f	$V_{DD} = 6 \text{ V}, \text{ R}_L = 0.1 \Omega$ $I_D \cong 60 \text{ A}, V_{GEN} = 10 \text{ V}, \text{ R}_g = 1 \Omega$	N-Ch 2	-	14	28	
Source-Drain Diode Ratings and	l Characteristics	b					
Pulsed Current ^a	la.		N-Ch 1	-	-	80	^
	I _{SM}		N-Ch 2	-	=	180	Α
Forward Voltage	V	I _F = 10 A, V _{GS} = 0 V	N-Ch 1	N-Ch 1 -		1.2	V
	V_{SD}	I _F = 20 A, V _{GS} = 0 V	N-Ch 2	-	0.8	1.2	\ \

Notes

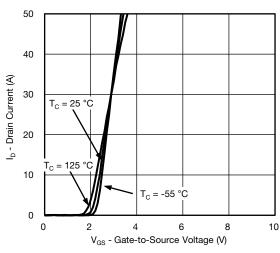
- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

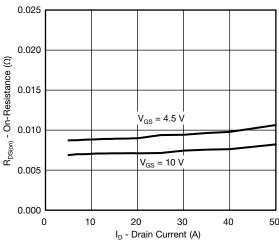




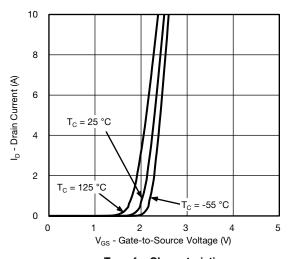
Output Characteristics



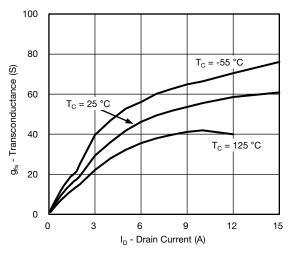
Transfer Characteristics



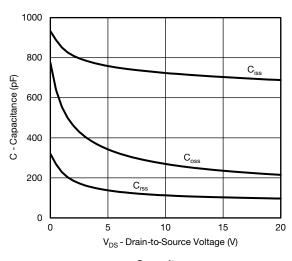
On-Resistance vs. Drain Current



Transfer Characteristics

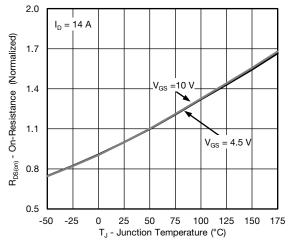


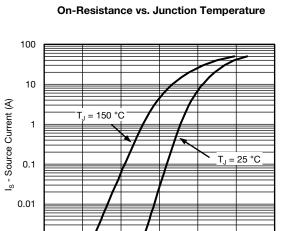
Transconductance



Capacitance

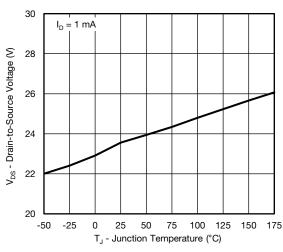




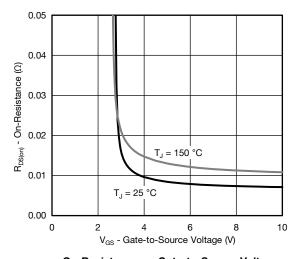


 V_{SD} - Source-to-Drain Voltage (V) **Source Drain Diode Forward Voltage**

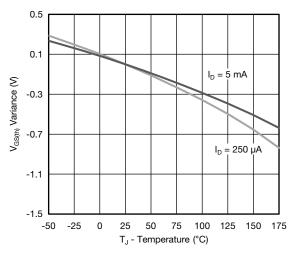
0.6



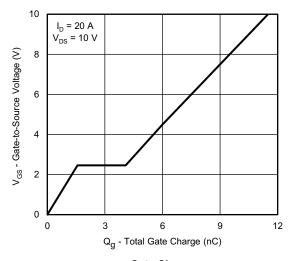
Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage



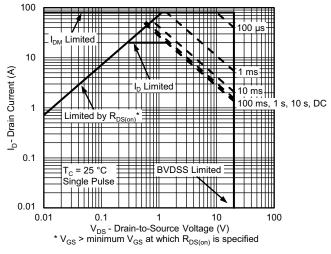
Threshold Voltage



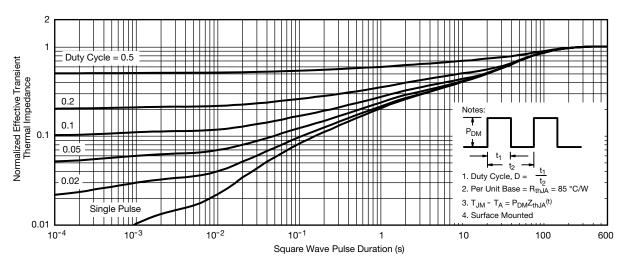
Gate Charge

0.001



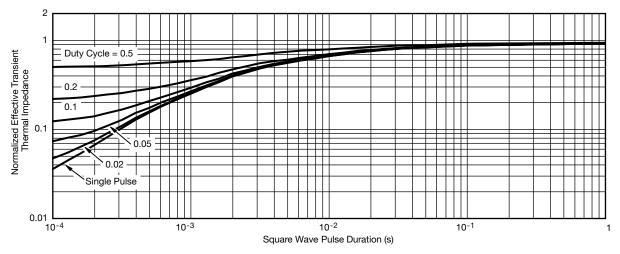


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient





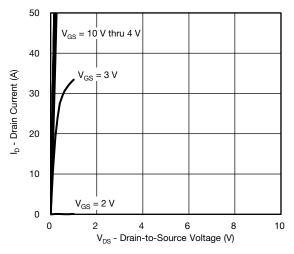
Normalized Thermal Transient Impedance, Junction-to-Case

Note

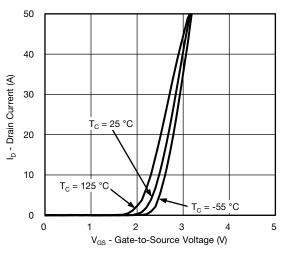
- The characteristics shown in the graph:
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C) is given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000

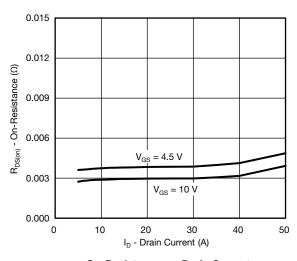




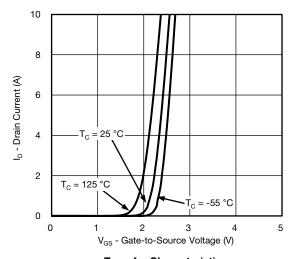
Output Characteristics



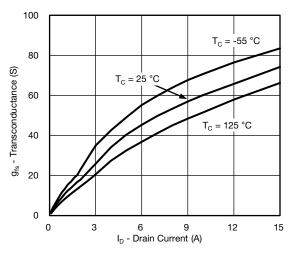
Transfer Characteristics



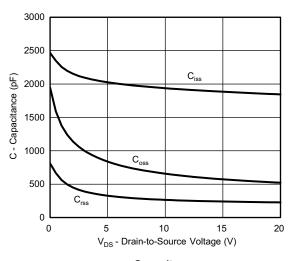
On-Resistance vs. Drain Current



Transfer Characteristics

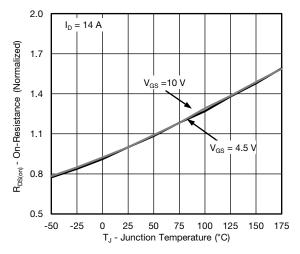


Transconductance

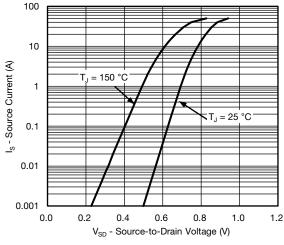


Capacitance

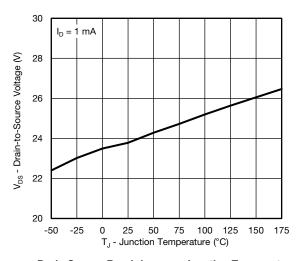




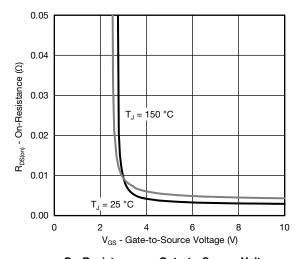
On-Resistance vs. Junction Temperature



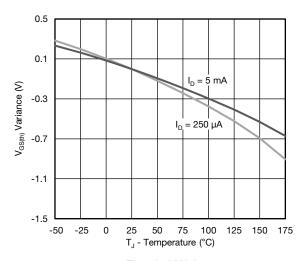
Source Drain Diode Forward Voltage



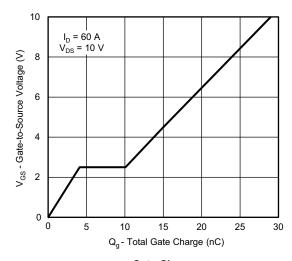
Drain Source Breakdown vs. Junction Temperature



On-Resistance vs. Gate-to-Source Voltage

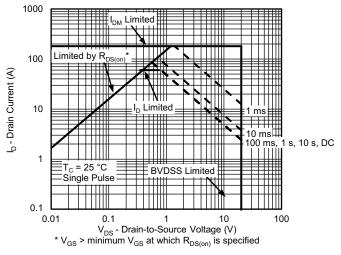


Threshold Voltage

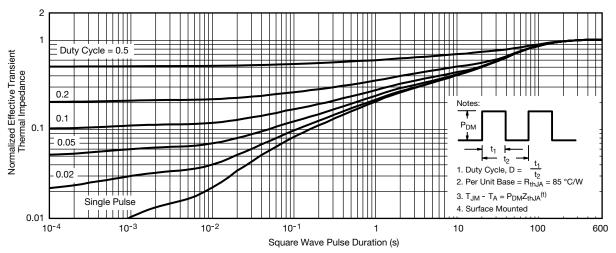


Gate Charge





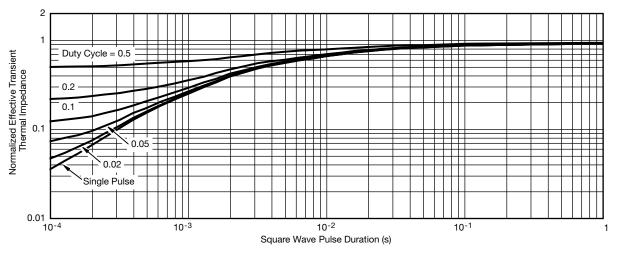
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

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N-CHANNEL 2 TYPICAL CHARACTERISTICS ($T_A = 25$ °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the graph:
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C) is given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg267774.



PowerPAK® SO-8L

Ordering codes for the SQ rugged series power MOSFETs in the PowerPAK SO-8L package:

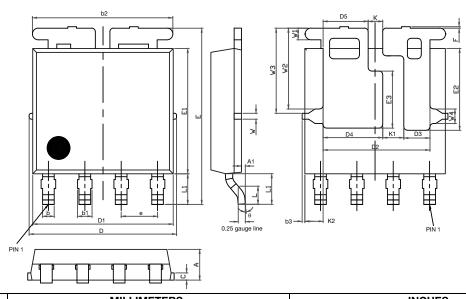
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	SQJ968EP	SQJ968EP-T1-GE3	SQJ968EP-T1_GE3
SQJ992EP	SQJ980AEP	SQJ980AEP-T1-GE3	SQJ980AEP-T1_GE3
	SQJ992EP	SQJ992EP-T1-GE3	SQJ992EP-T1_GE3

Note

a. Old ordering code is obsolete and no longer valid for new orders



PowerPAK® SO-8L Assymetric Case Outline



DIM.		MILLIMETERS		INCHES		
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
Α	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	0.06	0.13	0.000	0.003	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3	0.04	0.12	0.20	0.002	0.005	0.008
С	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.63	3.73	3.83	0.143	0.147	0.151
D3	0.81	0.91	1.01	0.032	0.036	0.040
D4	1.98	2.08	2.18	0.078	0.082	0.086
D5	1.47	1.57	1.67	0.058	0.062	0.066
е	1.20	1.27	1.34	0.047	0.050	0.053
Е	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
E3	1.89	1.99	2.09	0.074	0.078	0.082
F	0.05	0.12	0.19	0.002	0.005	0.007
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.41	0.51	0.61	0.016	0.020	0.024
K1	0.64	0.74	0.84	0.025	0.029	0.033
K2	0.54	0.64	0.74	0.021	0.025	0.029
W	0.13	0.23	0.33	0.005	0.009	0.013
W1	0.31	0.41	0.51	0.012	0.016	0.020
W2	2.72	2.82	2.92	0.107	0.111	0.115
W3	2.86	2.96	3.06	0.113	0.117	0.120
W4	0.41	0.51	0.61	0.016	0.020	0.024
θ	5°	10°	12°	5°	10°	12°

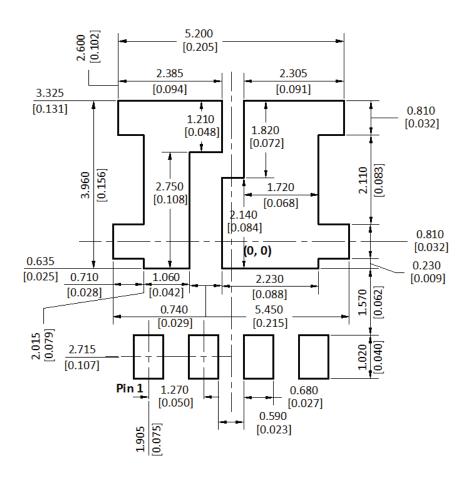
DWG: 6009

Note

Millimeters will govern



RECOMMENDED MINIMUM PADs FOR PowerPAK® SO-8L DUAL ASYMMETRIC



Recommended Minimum Pads Dimensions in mm [inches]



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Vishay

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Please note that some Vishay documentation may still make reference to RoHS Directive 2002/95/EC. We confirm that all the products identified as being compliant to Directive 2002/95/EC conform to Directive 2011/65/EU.

Vishay Intertechnology, Inc. hereby certifies that all its products that are identified as Halogen-Free follow Halogen-Free requirements as per JEDEC JS709A standards. Please note that some Vishay documentation may still make reference to the IEC 61249-2-21 definition. We confirm that all the products identified as being compliant to IEC 61249-2-21 conform to JEDEC JS709A standards.

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