

Vishay Siliconix

Automotive Dual N-Channel 30 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	30			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 10 \text{ V}$	0.0166			
$R_{DS(on)}(\Omega)$ at $V_{GS} = 4.5 \text{ V}$	0.0276			
I _D (A) per leg	8			
Configuration	Dual			
Package	PowerPAK SO-8L			

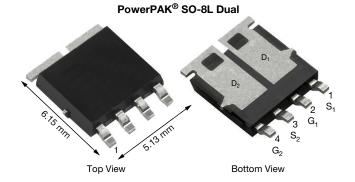
FEATURES

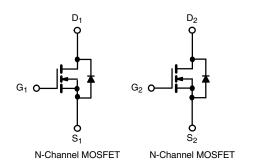
- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE





ABSOLUTE MAXIMUM RATINGS	$T_C = 25 ^{\circ}C$, unless	s otherwise noted	d)			
PARAMETER		SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V _{DS}	30	V		
Gate-Source Voltage		V_{GS}	± 20	V		
Continuous Drain Current ^a $ T_{C} = 25 ^{\circ}C $ $ T_{C} = 125 ^{\circ}C $		- I _D	8	А		
			8			
Continuous Source Current (Diode Conduction) a		I _S	8			
Pulsed Drain Current ^b		I _{DM}	32			
Single Pulse Avalanche Current	L = 0.1 mH	I _{AS}	23			
Single Pulse Avalanche Energy	L=0.11IIII	E _{AS}	26	mJ		
Maximum Power Dissipation ^b	T _C = 25 °C	D	48	W		
Maximum Power Dissipation 5	T _C = 125 °C	P_{D}	16	VV		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to +175	°C		
Soldering Recommendations (Peak Temperature) d, e			260	30		

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount c	R _{thJA}	85	°C/W
Junction-to-Case (Drain)		R _{thJC}	3.1	C/VV

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.



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PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static					•		
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	= 0, I _D = 250 μA	30	-	-	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	· V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA
		$V_{GS} = 0 V$	V _{DS} = 30 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{GS} = 0 V$	$V_{DS} = 30 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$	-	-	50	μΑ
		$V_{GS} = 0 V$	$V_{DS} = 30 \text{ V}, T_{J} = 175 ^{\circ}\text{C}$	-	-	150	
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	30	-	-	Α
		V _{GS} = 10 V	I _D = 7.6 A	-	0.0138	0.0166	
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}$	$I_D = 5.9 A$	-	0.0230	0.0276	Ω
	1 (DS(On)	V _{GS} = 10 V	I _D = 7.6 A, T _J = 125 °C	-	-	0.0252	
		V _{GS} = 10 V	$I_D = 7.6 \text{ A}, T_J = 175 ^{\circ}\text{C}$	-	-	0.0300	
Forward Transconductance b	9 _{fs}	V _{DS} :	= 15 V, I _D = 7.6 A	-	20	-	S
Dynamic ^b	1	T				Т	
Input Capacitance	C _{iss}			-	929	1161	
Output Capacitance	C _{oss}	$V_{GS} = 0 V$	$V_{DS} = 15 \text{ V}, f = 1 \text{ MHz}$	-	280	350	pF
Reverse Transfer Capacitance	C _{rss}			-	93	116	
Total Gate Charge ^c	Qg			-	17	26	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 15 \text{ V}, I_D = 10 \text{ A}$	-	3	-	nC
Gate-Drain Charge ^c	Q_{gd}			-	3	-	
Gate Resistance	R_g		f = 1 MHz	1.1	-	5	Ω
Turn-On Delay Time ^c	t _{d(on)}			-	4.5	7	
Rise Time ^c	t _r	V _{DD} :	$V_{DD} = 15 \text{ V}, R_1 = 15 \Omega$		10	15	ns
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 1$ A, $V_{GEN} = 10$ V, $R_g = 6$ Ω		-	20	30	
Fall Time ^c	t _f			-	7	10	
Source-Drain Diode Ratings and Chara	acteristics b	1					
Pulsed Current ^a	I _{SM}			-	-	32	Α
Forward Voltage	V _{SD}	I _F = 4.3 A, V _{GS} = 0		-	0.8	1.2	V

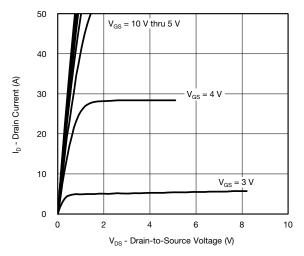
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

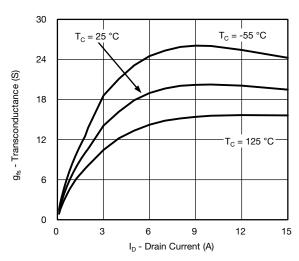
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



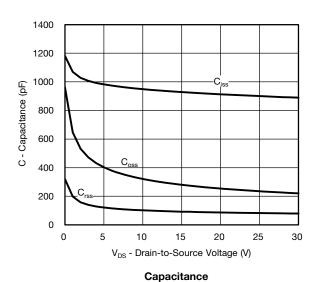
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)

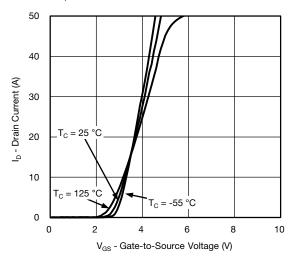


Output Characteristics

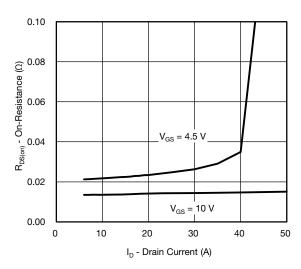


Transconductance

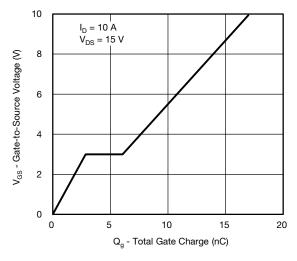




Transfer Characteristics

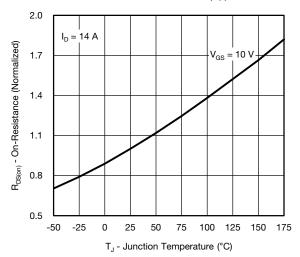


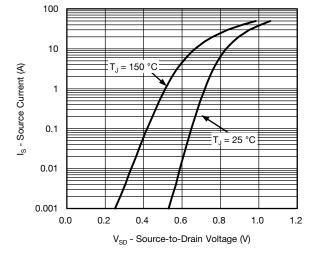
On-Resistance vs. Drain Current



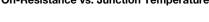


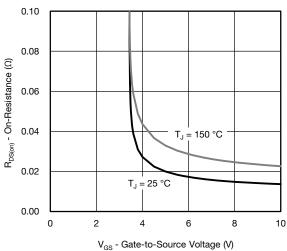
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



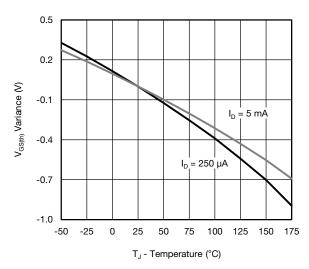


On-Resistance vs. Junction Temperature



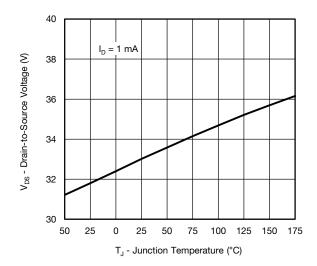


Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage

Threshold Voltage

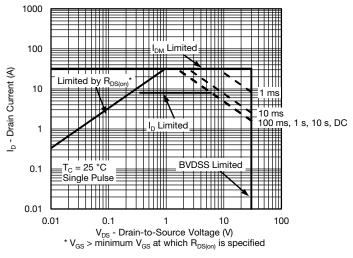


Drain Source Breakdown vs. Junction Temperature

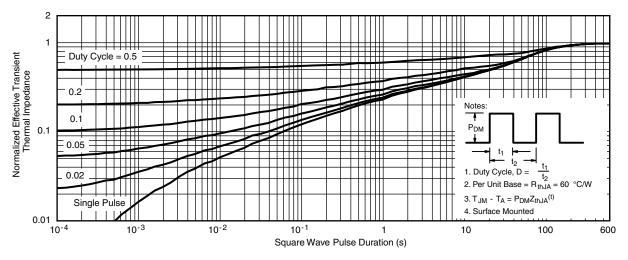
For technical questions, contact: automostech



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



Safe Operating Area

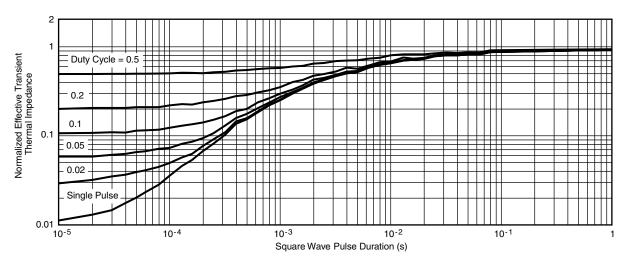


Normalized Thermal Transient Impedance, Junction-to-Ambient

ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg262832.



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Vishay Siliconix

REVISION	HISTORY a	
REVISION	DATE	DESCRIPTION OF CHANGE
В	04-Aug-15	Revised R _g minimum limit

Note

a. As of April 2014



PowerPAK® SO-8L

Ordering codes for the SQ rugged series power MOSFETs in the PowerPAK SO-8L package:

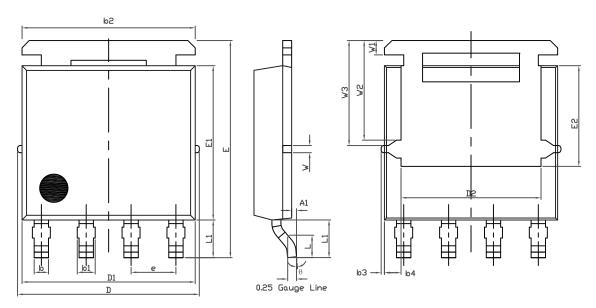
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	SQJ968EP	SQJ968EP-T1-GE3	SQJ968EP-T1_GE3
SQJ992EP	SQJ980AEP	SQJ980AEP-T1-GE3	SQJ980AEP-T1_GE3
	SQJ992EP	SQJ992EP-T1-GE3	SQJ992EP-T1_GE3

Note

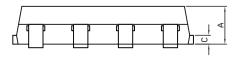
a. Old ordering code is obsolete and no longer valid for new orders

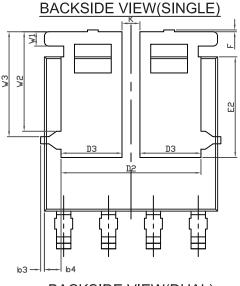
Vishay Siliconix

PowerPAK® SO-8L Case Outline for all Parts



TOPSIDE VIEW





BACKSIDE VIEW(DUAL)



Vishay Siliconix

DIM	MILLIMETERS			INCHES		
DIM.	MIN.	NOM.	MAX.	MIN. NOM.		MAX.
А	1.00	1.07	1.14	0.039	0.042	0.045
A1	0.00	-	0.127	0.00	-	0.005
b	0.33	0.41	0.48	0.013	0.016	0.019
b1	0.44	0.51	0.58	0.017	0.020	0.023
b2	4.80	4.90	5.00	0.189	0.193	0.197
b3		0.094			0.004	
b4		0.47			0.019	
С	0.20	0.25	0.30	0.008	0.010	0.012
D	5.00	5.13	5.25	0.197	0.202	0.207
D1	4.80	4.90	5.00	0.189	0.193	0.197
D2	3.86	3.96	4.06	0.152	0.156	0.160
D3	1.63	1.73	1.83	0.064	0.068	0.072
е		1.27 BSC			0.050 BSC	
Е	6.05	6.15	6.25	0.238	0.242	0.246
E1	4.27	4.37	4.47	0.168	0.172	0.176
E2	2.75	2.85	2.95	0.108	0.112	0.116
F	-	-	0.15	-	-	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K		0.51			0.020	
W	0.23			0.009		
W1	0.41			0.016		
W2	2.82			0.111		
W3	2.96			0.117		
q	0°	-	10°	0°	_	10°

ECN: C15-1203-Rev. A, 07-Sep-15

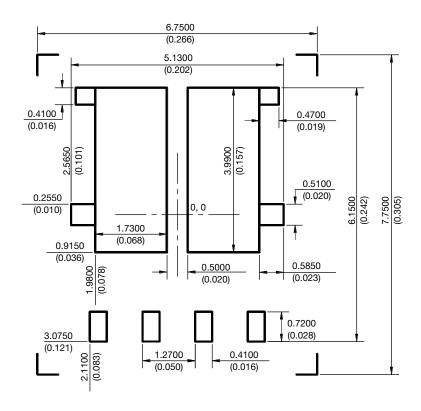
DWG: 6044

Note

· Millimeters will gover



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL



Recommended Minimum Pads Dimensions in mm (inches) Keep-out 6.75 (0.266) x 7.75 (0.305)



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Vishay

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Revision: 02-Oct-12 Document Number: 91000

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