

Vishay Siliconix

Automotive N-Channel 150 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY					
V _{DS} (V)	150				
$R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$	0.0355				
$R_{DS(on)}$ (Ω) at $V_{GS} = 7.5 \text{ V}$	0.0395				
I _D (A)	24.5				
Configuration	Single				
Package	PowerPAK SO-8L				

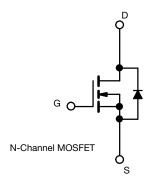
FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Material categorization: for definitions of compliance please see www.vishav.com/doc?99912





ROHS COMPLIANT HALOGEN FREE



ABSOLUTE MAXIMUM RATINGS	(T _C = 25 °C, unles	s otherwise noted	d)		
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-source voltage		V _{DS}	150	V	
Gate-source voltage	V _{GS}	V _{GS} ± 20			
Continuous drain current	T _C = 25 °C	1_	24.5		
Continuous drain current	T _C = 125 °C	I _D	14		
Continuous source current (diode conduction)		Is	50	Α	
Pulsed drain current ^a		I _{DM}	90		
Single pulse avalanche current	L = 0.1 mH	I _{AS}	30		
Single pulse avalanche energy	L = 0.1 IIII	E _{AS}	45	mJ	
Maximum power dissipation ^a	T _C = 25 °C	P _D	55	W	
	T _C = 125 °C	r _D	18	VV	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature) c, d			260	C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount b	R _{thJA}	70	°C/W
Junction-to-case (drain)		R_{thJC}	2.7	C/VV

Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. When mounted on 1" square PCB (FR4 material)
- c. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- d. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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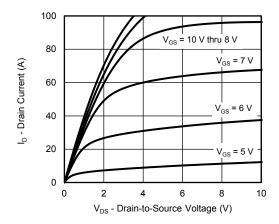
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static						l	L
Drain-source breakdown voltage	V_{DS}	V _{GS}	= 0, I _D = 250 μA	150	-	-	V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	2.5	3.0	3.5	V
Gate-source leakage	I _{GSS}	V _{DS} =	$0 \text{ V}, \text{V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		V _{GS} = 0 V	V _{DS} = 150 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	$V_{GS} = 0 V$	V _{DS} = 150 V, T _J = 125 °C	-	-	50	μΑ
		$V_{GS} = 0 V$	V _{DS} = 150 V, T _J = 175 °C	-	-	200	
On-state drain current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	10	-	-	Α
		V _{GS} = 10 V	I _D = 10 A	-	0.0293	0.0355	
Duning and an atota projetom and	В	V _{GS} = 7.5 V	I _D = 8 A	-	0.0326	0.0395	Ω
Drain-source on-state resistance ^a	$R_{DS(on)}$	V _{GS} = 10 V	I _D = 10 A, T _J = 125 °C	1	-	0.0681	
		V _{GS} = 10 V	I _D = 10 A, T _J = 175 °C	-	-	0.0896	
Forward transconductance b	9fs	V _{DS}	= 15 V, I _D = 10 A	1	16	-	S
Dynamic ^b							
Input capacitance	C _{iss}			-	746	1045	
Output capacitance	Coss	$V_{GS} = 0 V$	V _{DS} = 25 V, f = 1 MHz	1	504	710	рF
Reverse transfer capacitance	C _{rss}			1	23	35	
Total gate charge c	Qg			-	14	22	
Gate-source charge c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 75 \text{ V}, I_{D} = 5 \text{ A}$	1	3.5	-	nC
Gate-drain charge ^c	Q _{gd}	1		-	4	-	
Gate resistance	R_g		f = 1 MHz	0.45	0.98	1.50	Ω
Turn-on delay time ^c	t _{d(on)}			1	9	20	
Rise time ^c	t _r	V _{DD} :	= 75 V, R _L = 15 Ω	1	4	10	
Turn-off delay time c	t _{d(off)}	$I_D \cong 5 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$		-	19	40	ns
Fall time ^c	t _f	1		1	8	20	
Source-Drain Diode Ratings and Charac	teristics ^b	•				l	l.
Pulsed current a	I _{SM}			-	_	90	Α
Forward voltage	V _{SD}	I _F :	= 10 A, V _{GS} = 0	-	0.82	1.2	V
Body diode reverse recovery time	t _{rr}			-	63	130	ns
Body diode reverse recovery charge	Q_{rr}	1	A -11/-11 - 400 A/ -	-	154	310	nC
Reverse recovery fall time	ta	$I_F = 5$	A, di/dt = 100 A/μs	-	53	-	
Reverse recovery rise time	t _b	1		-	10	-	ns
Body diode peak reverse recovery current	I _{RM(REC)}	1		_	-4.3	_	Α

Notes

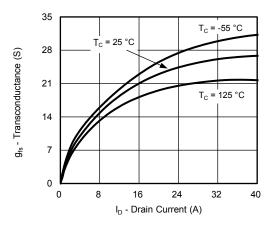
- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

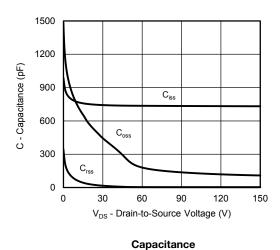




Output Characteristics

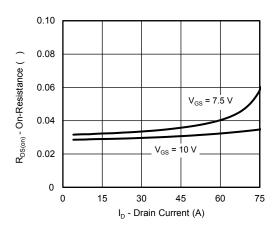


Transconductance

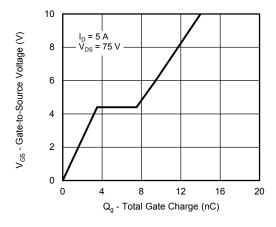


60 48 48 48 36 12 T_C = 25 °C T_C = 125 °C T_C = -55 °C 0 2 4 6 8 10 V_{GS} - Gate-to-Source Voltage (V)

Transfer Characteristics

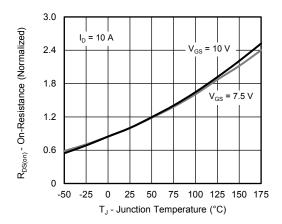


On-Resistance vs. Drain Current

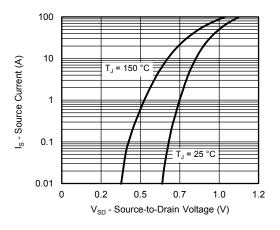


Gate Charge

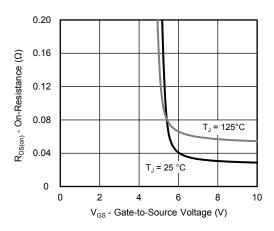




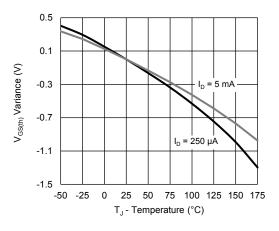
On-Resistance vs. Junction Temperature



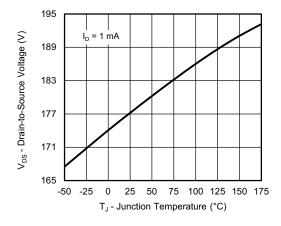
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to Source Voltage

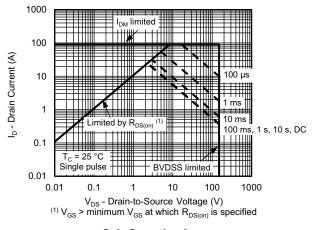


Threshold Voltage

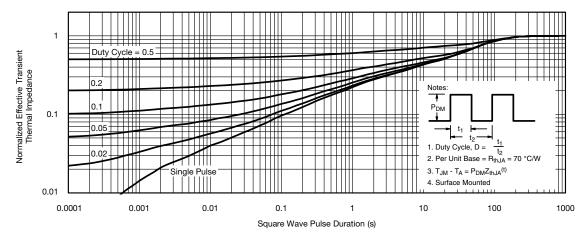


Drain Source Breakdown vs. Junction Temperature



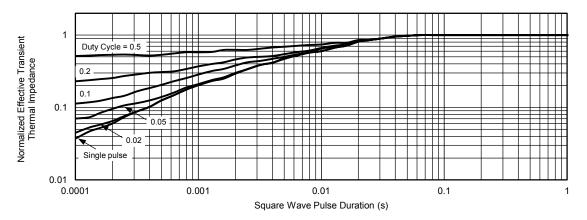


Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient





Normalized Thermal Transient Impedance, Junction-to-Case

Note

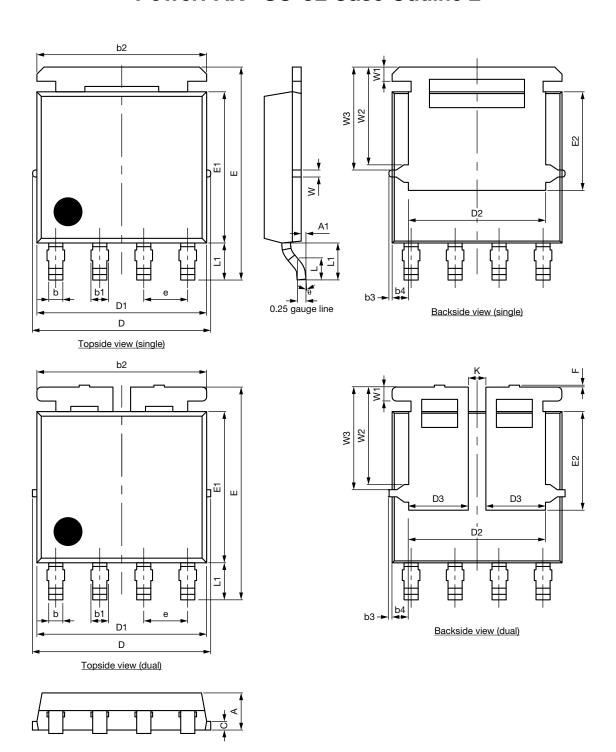
- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg276483.



PowerPAK® SO-8L Case Outline 2



Vishay Siliconix

DIM.		MILLIMETERS		INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094		0.004			
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC		0.050 BSC			
Е	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	2.75	2.85	2.95	0.108	0.112	0.116	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K		0.51		0.020			
W	0.23		0.009				
W1	0.41		0.016				
W2	2.82		0.111				
W3	2.96			0.117			
θ	0°	-	10°	0°	-	10°	

ECN: C21-1498-Rev. C, 01-Nov-2021

DWG: 6044

Note

• Millimeters will govern



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L SINGLE



Recommended Minimum Pads Dimensions in mm (inches)



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