

Automotive Dual N-Channel 75 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY	
V _{DS} (V)	75
$R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$	0.050
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5 \text{ V}$	0.066
I _D (A) per leg	8
Configuration	Dual

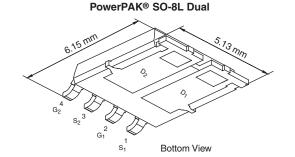
FEATURES

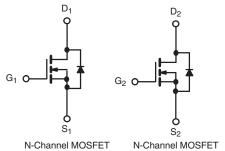
- TrenchFET® Power MOSFET
- AEC-Q101 Qualified^d
- 100 % Rq and UIS Tested
- Material categorization:
 For definitions of compliance please see www.vishav.com/doc?99912











ORDERING INFORMATION	
Package	PowerPAK SO-8L
Lead (Pb)-free and Halogen-free	SQJ980AEP-T1-GE3

ABSOLUTE MAXIMUM RATINGS	$S(1_C = 25 ^{\circ}C, \text{ unles})$	s otnerwise noted	1)		
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	75	٧	
Gate-Source Voltage		V _{GS}	± 20	V	
Continuous Drain Currenta	T _C = 25 °C	1	17		
Continuous Drain Current	T _C = 125 °C	I _D	10		
Continuous Source Current (Diode Conduction) ^a		I _S	30	А	
Pulsed Drain Current ^b		I _{DM}	68		
Single Pulse Avalanche Current		I _{AS}	14		
Single Pulse Avalanche Energy	L = 0.1 mH	E _{AS}	10	mJ	
Maximum Power Dissipation ^b	T _C = 25 °C	D	34	W	
Maximum Fower Dissipation	T _C = 125 °C	P_{D}	11	vv	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to + 175	°C	
Soldering Recommendations (Peak Temperature) ^{e, f}		-	260	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount ^c	R _{thJA}	85	°C/W
Junction-to-Case (Drain)		R_{thJC}	4.3	C/VV

Notes

- a. Package limited.
- b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.
- e. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection..
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components.

ARE SUBJECT TO SPECIFIC DISCLAIMERS, SET FORTH AT www.vishay.com/doc?91000



PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS}	= 0, I _D = 250 μA	75		=.	V
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	1.5	2.0	2.5	V
Gate-Source Leakage	I _{GSS}	V _{DS} =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	-	-	± 100	nA
		V _{GS} = 0 V	V _{DS} = 75 V	-	-	1	
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 75 V, T _J = 125 °C	-	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 75 V, T _J = 175 °C	-	-	150	1
On-State Drain Current ^a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	30	-		Α
		V _{GS} = 10 V	I _D = 3.8 A	=.	0.041	0.050	
Drain-Source On-State Resistance ^a		V _{GS} = 10 V	I _D = 3.8 A, T _J = 125 °C	=.	-	0.089	Ω
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 3.8 A, T _J = 175 °C	-	-	0.116	
		V _{GS} = 4.5 V	I _D = 3.3 A	-	0.055	0.066	
Forward Transconductanceb	9 _{fs}	V _{DS} = 15 V, I _D = 3.8 A		-	14	-	S
Dynamic ^b							
Input Capacitance	C _{iss}		V _{GS} = 0 V V _{DS} = 35 V, f = 1 MHz	=.	630	790	pF
Output Capacitance	C _{oss}	$V_{GS} = 0 V$		=.	84	105	
Reverse Transfer Capacitance	C _{rss}			-	36	45	
Total Gate Charge ^c	Qg			-	14	21	
Gate-Source Charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 35 \text{ V}, I_D = 9.7 \text{ A}$	-	2.3	-	nC
Gate-Drain Charge ^c	Q _{gd}			=.	2.9	-	
Gate Resistance	R _g	f = 1 MHz		1.3	2.67	4	Ω
Turn-On Delay Time ^c	t _{d(on)}			-	9	14	
Rise Time ^c	t _r	$V_{DD} = 35 \text{ V}, \text{ R}_{L} = 35 \Omega$ $I_{D} \cong 1 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	10	15	ns
Turn-Off Delay Time ^c	t _{d(off)}			-	16	24	
Fall Time ^c	t _f			-	12	18	
Source-Drain Diode Ratings and Chara	acteristics ^b						
Pulsed Current ^a	I _{SM}			-	-	68	Α
Forward Voltage	V_{SD}	I _F = 2.4 A, V _{GS} = 0		_	0.8	1.1	V

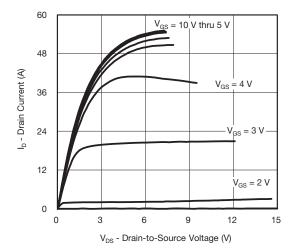
Notes

- a. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.
- c. Independent of operating temperature.

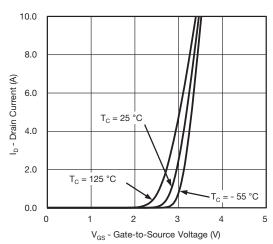
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



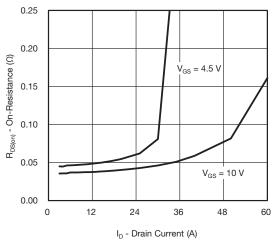
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



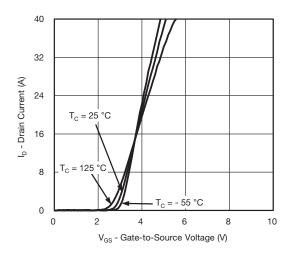
Output Characteristics



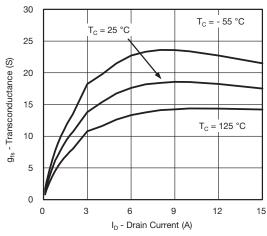
Transfer Characteristics



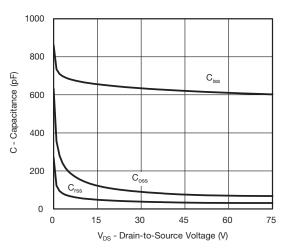
On-Resistance vs. Drain Current



Transfer Characteristics



Transconductance

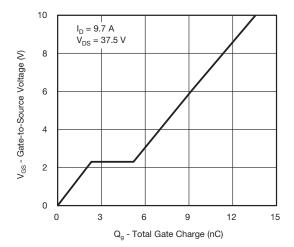


Capacitance

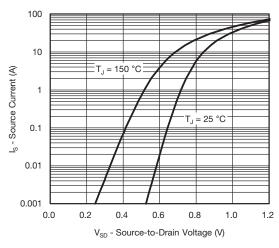
150 175



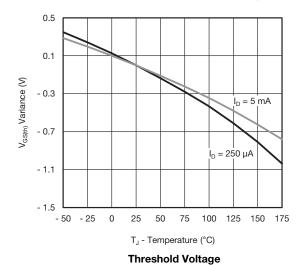
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



Gate Charge



Source Drain Diode Forward Voltage



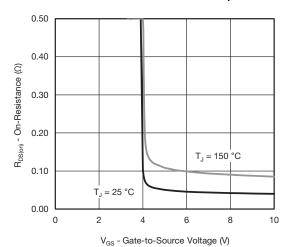
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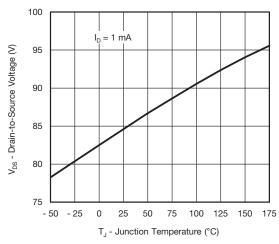
- 50

- 25 0 25 50 75 100 125

$\label{eq:TJ-Junction} T_{J} \text{ - Junction Temperature (°C)}$ $\mbox{On-Resistance vs. Junction Temperature}$



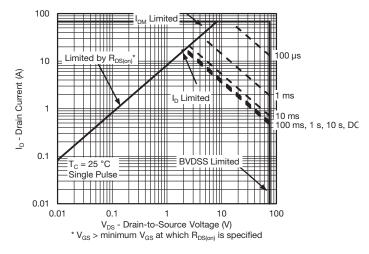
On-Resistance vs. Gate-to-Source Voltage



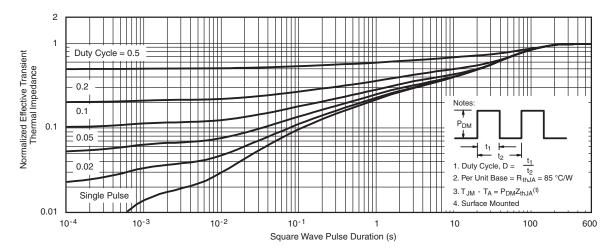
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



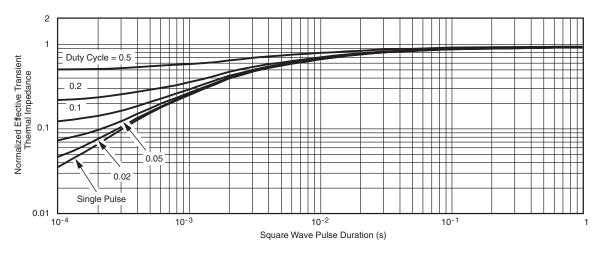
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

Note

- The characteristics shown in the two graphs
- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?62833.



PowerPAK® SO-8L

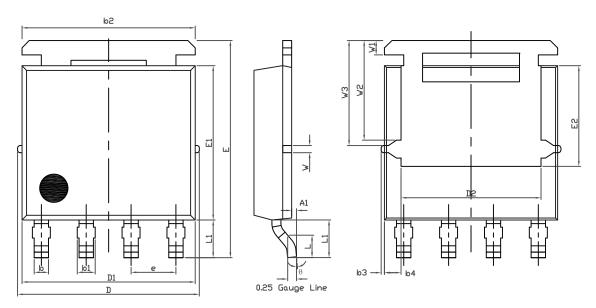
Ordering codes for the SQ rugged series power MOSFETs in the PowerPAK SO-8L package:

SQJ200EP SQJ200EPTIGE3 SQJ202EPTIGE3 SQJ202EPTIGE3 SQJ401EP SQJ401EPTIGE3 SQJ402EPTIGE3 SQJ402EPTIGE3 SQJ402EPTIGE3 SQJ403EEPTIGE3 SQJ403EEPTIGE3 SQJ403EEPTIGE3 SQJ403EPTIGE3 SQJ403EPTIGE3 SQJ410EP SQJ410EPTIGE3 SQJ410EPTIGE3 SQJ412EPTIGE3 SQJ412EP SQJ412EPTIGE3 SQJ412EPTIGE3 SQJ412EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ43EPTIGE3 SQJ44SEP SQJ45EPTIGE3 SQJ44SEPTIGE3 SQJ44SEPTIGE3 SQJ44SEPTIGE3 SQJ44SEPTIGE3 SQJ44SEPTIGE3 SQJ44SEPTIGE3 SQJ44SEPTIGE3 SQJ44SEPTIGE3 SQJ46GEP SQJ46GEPTIGE3 SQJ46GEPTIGE3 SQJ46GEPTIGE3 SQJ46GEPTIGE3 SQJ46GEPTIGE3 SQJ46GEPTIGE3 SQJ46GE	DATASHEET PART NUMBER	OLD ORDERING CODE a	NEW ORDERING CODE
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	SQJ992EP	SQJ992EP-T1-GE3	SQJ992EP-T1_GE3

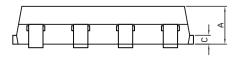
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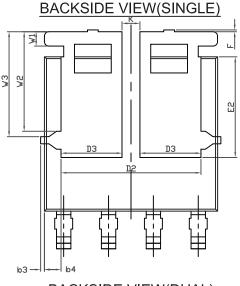
a. Old ordering code is obsolete and no longer valid for new orders

PowerPAK® SO-8L Case Outline for all Parts



TOPSIDE VIEW





BACKSIDE VIEW(DUAL)



DIM	MILLIMETERS		INCHES				
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
А	1.00	1.07	1.14	0.039	0.042	0.045	
A1	0.00	-	0.127	0.00	-	0.005	
b	0.33	0.41	0.48	0.013	0.016	0.019	
b1	0.44	0.51	0.58	0.017	0.020	0.023	
b2	4.80	4.90	5.00	0.189	0.193	0.197	
b3		0.094			0.004		
b4		0.47			0.019		
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	5.00	5.13	5.25	0.197	0.202	0.207	
D1	4.80	4.90	5.00	0.189	0.193	0.197	
D2	3.86	3.96	4.06	0.152	0.156	0.160	
D3	1.63	1.73	1.83	0.064	0.068	0.072	
е		1.27 BSC			0.050 BSC		
Е	6.05	6.15	6.25	0.238	0.242	0.246	
E1	4.27	4.37	4.47	0.168	0.172	0.176	
E2	2.75	2.85	2.95	0.108	0.112	0.116	
F	-	-	0.15	-	-	0.006	
L	0.62	0.72	0.82	0.024	0.028	0.032	
L1	0.92	1.07	1.22	0.036	0.042	0.048	
K		0.51			0.020		
W	0.23		0.009				
W1	0.41		0.016				
W2		2.82		0.111			
W3		2.96			0.117		
q	0°	-	10°	0°	_	10°	

ECN: C15-1203-Rev. A, 07-Sep-15

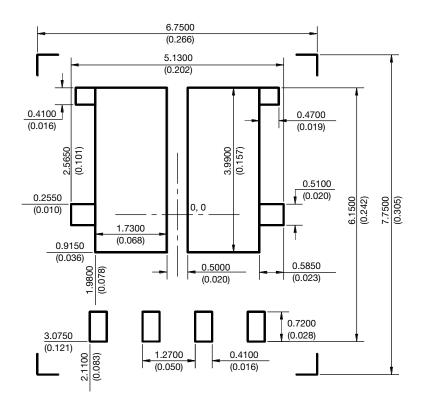
DWG: 6044

Note

· Millimeters will gover



RECOMMENDED MINIMUM PAD FOR PowerPAK® SO-8L DUAL



Recommended Minimum Pads Dimensions in mm (inches) Keep-out 6.75 (0.266) x 7.75 (0.305)



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Vishay

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Revision: 02-Oct-12 Document Number: 91000

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