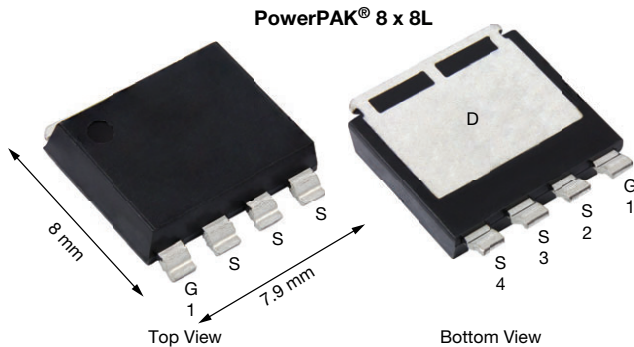


## Automotive P-Channel 30 V (D-S) 175 °C MOSFET

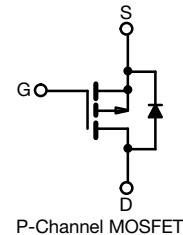


**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



### FEATURES

- AEC-Q101 qualified
- 100 % R<sub>g</sub> and UIS tested
- Thin 1.6 mm package
- Very low thermal resistance
- Material categorization:  
for definitions of compliance please see  
[www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



PRODUCT SUMMARY	
V <sub>DS</sub> (V)	-30
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = -10 V	0.0014
I <sub>D</sub> (A)	-280
Configuration	Single
Package	PowerPAK 8 x 8L

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	-30	V
Gate-source voltage		V <sub>GS</sub>	±20	
Continuous drain current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	-280	A
	T <sub>C</sub> = 125 °C		-280	
Continuous source current (diode conduction)		I <sub>S</sub>	545	
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	-280	
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	63	
Single pulse avalanche energy		E <sub>AS</sub>	198	
Maximum power dissipation	T <sub>C</sub> = 25 °C	P <sub>D</sub>	600	W
	T <sub>C</sub> = 125 °C		200	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C
Soldering recommendations (peak temperature) <sup>d</sup>			260	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>c</sup>	R <sub>thJA</sub>	44	°C/W
Junction-to-case (drain)		R <sub>thJC</sub>	0.25	

### Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)
- See solder profile ([www.vishay.com/doc?73257](http://www.vishay.com/doc?73257)). The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection



<b>SPECIFICATIONS</b> ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-source breakdown voltage	$V_{DS}$	$V_{GS} = 0, I_D = 250\text{ }\mu\text{A}$		-30	-	-	V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		-1.5	-2	-2.5	
Gate-source leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100$	nA
Zero gate voltage drain current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = -30\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = -30\text{ V}, T_J = 125\text{ }^\circ\text{C}$	-	-	200	
		$V_{GS} = 0\text{ V}$	$V_{DS} = -30\text{ V}, T_J = 175\text{ }^\circ\text{C}$	-	-	330	
On-state drain current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = -10\text{ V}$		-100	-	-	A
Drain-source on-state resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}$	$V_{DS} \geq -5\text{ V}, I_D = -8\text{ A}$	-	0.0015	0.0022	$\Omega$
		$V_{GS} = -10\text{ V}$	$I_D = -10\text{ A}$	-	0.0010	0.0014	
		$V_{GS} = -10\text{ V}$	$I_D = -10\text{ A}, T_J = 125\text{ }^\circ\text{C}$	-	-	0.0019	
		$V_{GS} = -10\text{ V}$	$I_D = -10\text{ A}, T_J = 175\text{ }^\circ\text{C}$	-	-	0.0022	
Forward transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = -15\text{ V}, I_D = -50\text{ A}$		-	180	-	S
<b>Dynamic <sup>b</sup></b>							
Input capacitance	$C_{ISS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 15\text{ V}, f = 1\text{ MHz}$	-	23 588	33 050	$\text{pF}$
Output capacitance	$C_{OSS}$			-	2443	3420	
Reverse transfer capacitance	$C_{RSS}$			-	2267	3174	
Total gate charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = -15\text{ V}, I_D = -30\text{ A}$	-	487	731	$\text{nC}$
Gate-source charge <sup>c</sup>	$Q_{gs}$			-	86	-	
Gate-drain charge <sup>c</sup>	$Q_{gd}$			-	82	-	
Gate resistance	$R_g$	$f = 1\text{ MHz}$		1	2.1	3.2	$\Omega$
Turn-on delay time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = -15\text{ V}, R_L = 0.5\text{ }\Omega$ $I_D \cong -30\text{ A}, V_{GEN} = -10\text{ V}, R_g = 1\text{ }\Omega$		-	20	30	$\text{ns}$
Rise time <sup>c</sup>	$t_r$			-	30	45	
Turn-off delay time <sup>c</sup>	$t_{d(off)}$			-	194	291	
Fall time <sup>c</sup>	$t_f$			-	78	117	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Reverse recovery time	$t_a$	$V_{DD} = -24\text{ V}, I_{FM} = -20\text{ A},$ $di/dt = 100\text{ A}/\mu\text{s}$		20	-	-	$\text{ns}$
	$t_b$			24	-	-	
	$t_{rr}$			-	43	86	
Reverse recovery charge	$Q_{rr}$			-	45	90	$\text{nC}$
Reverse recovery current	$I_{RM}$	-	-	1.9	A		
Pulsed current <sup>a</sup>	$I_{SM}$	-	-	1100	A		
Forward voltage	$V_{SD}$	$I_F = -50\text{ A}, V_{GS} = 0$		-	-0.8	-1.1	V

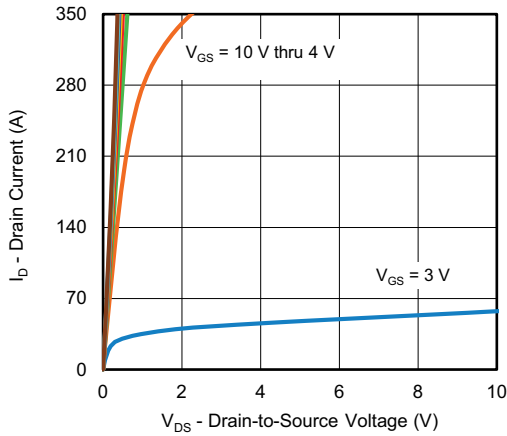
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

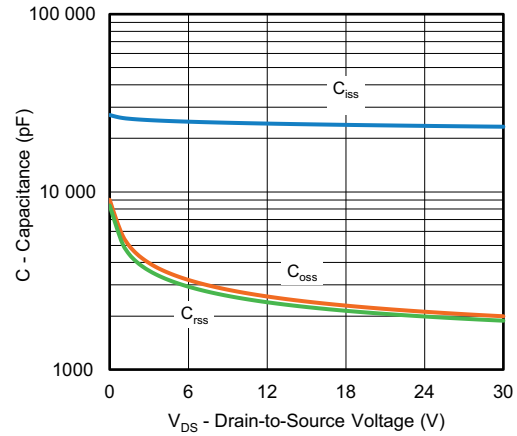
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



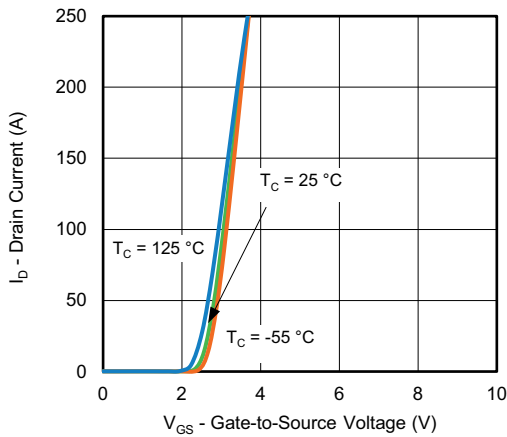
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



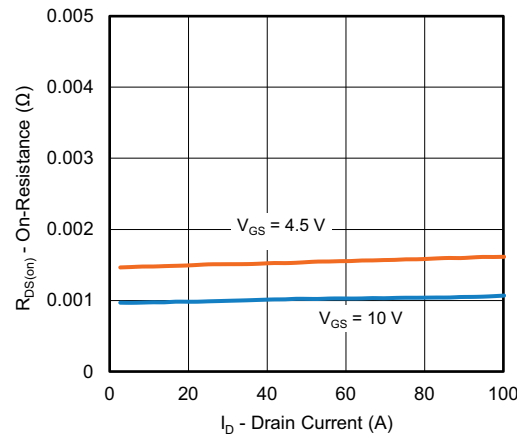
Output Characteristics



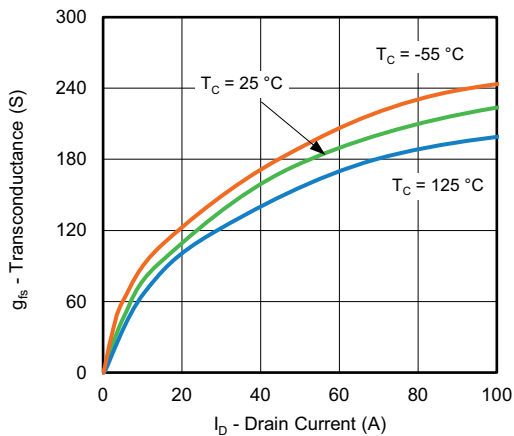
Capacitance



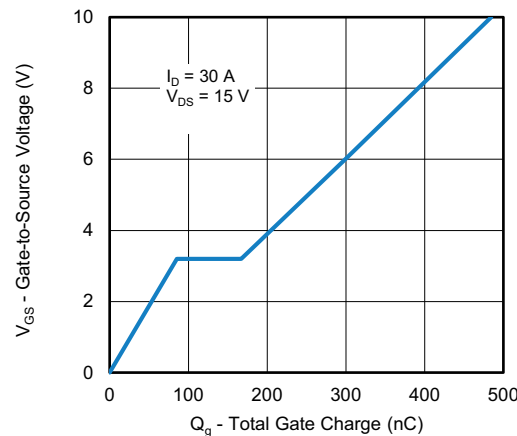
Transfer Characteristics



On-Resistance vs. Drain Current



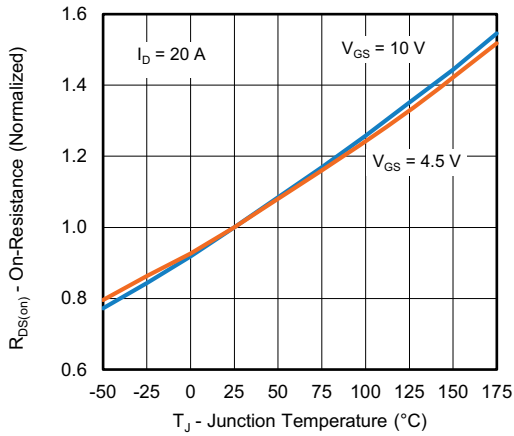
Transconductance



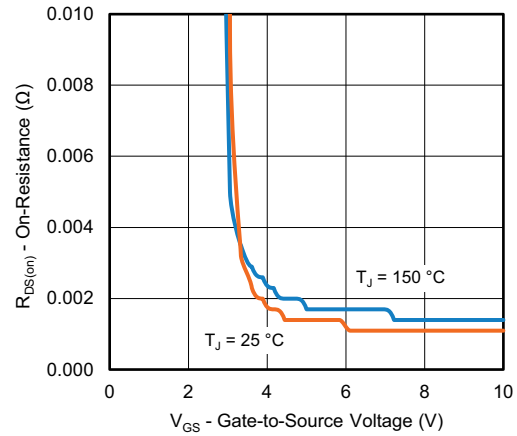
Gate Charge



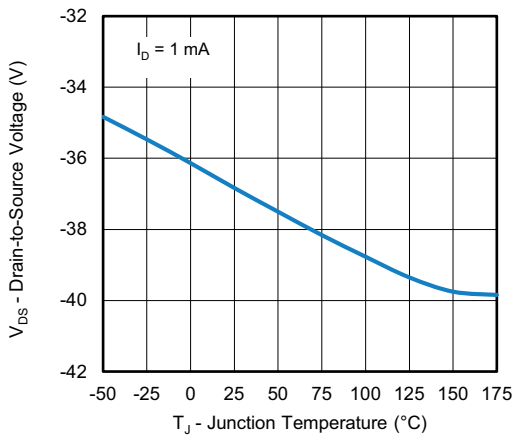
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



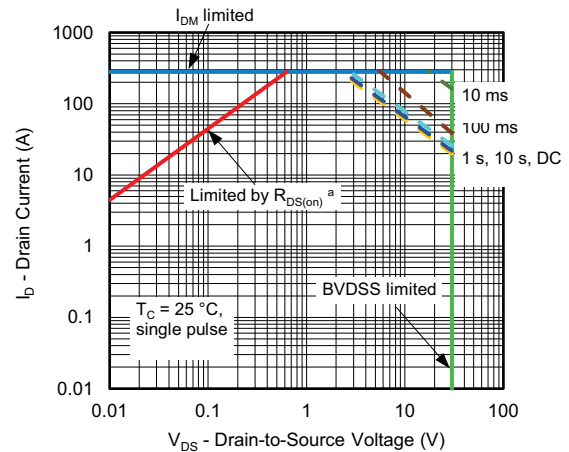
On-Resistance vs. Junction Temperature



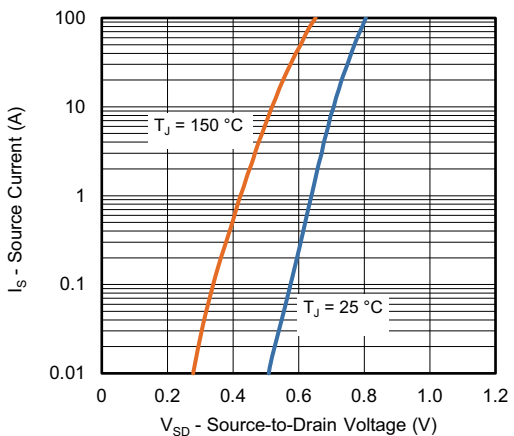
On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature



Safe Operating Area



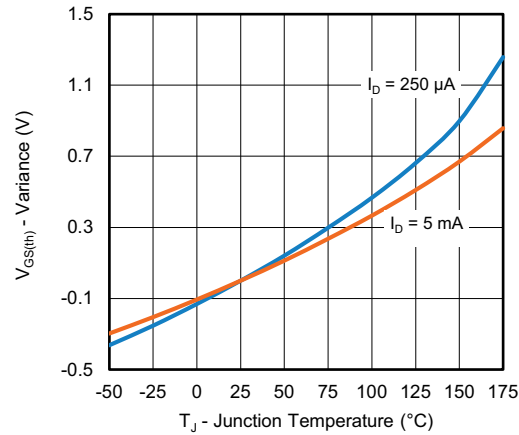
Source Drain Diode Forward Voltage

Note

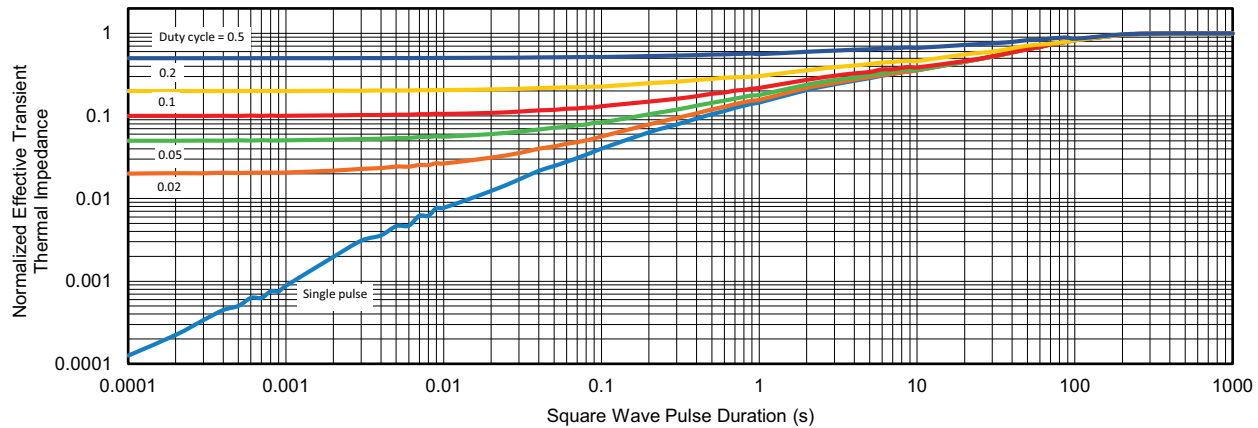
a. V<sub>GS</sub> > minimum V<sub>GS</sub> at which R<sub>DS(on)</sub> is specified



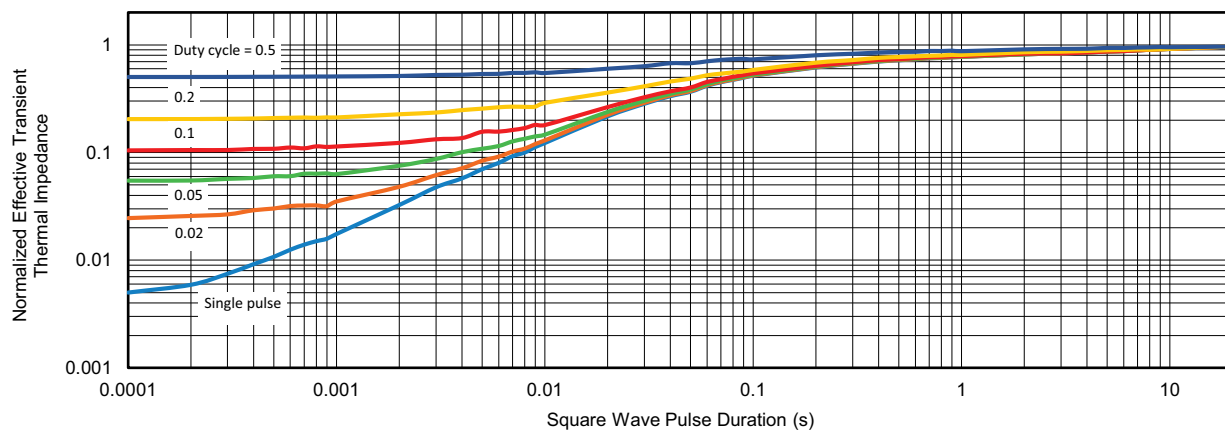
**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Threshold Voltage**



**Normalized Thermal Transient Impedance, Junction-to-Ambient**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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### PowerPAK<sup>®</sup> 8 x 8L BWL Case Outline 2



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.50	1.60	1.70	0.059	0.063	0.067
A1	0.00	-	0.127	0.000	-	0.005
A2	0.655	0.705	0.755	0.026	0.028	0.030
b	0.92	1.00	1.08	0.036	0.039	0.043
b1	1.02	1.10	1.18	0.040	0.043	0.046
b2	6.84	6.94	7.04	0.269	0.273	0.277
c	0.20	0.25	0.30	0.008	0.010	0.012
D1	7.80	7.90	8.00	0.307	0.311	0.315
D2	6.70	6.80	6.90	0.264	0.268	0.272
D5	0.37	0.47	0.57	0.015	0.019	0.022
D6	2.49	2.59	2.69	0.098	0.102	0.106
e	1.97	2.00	2.03	0.078	0.079	0.080
E	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	4.21	4.31	4.41	0.166	0.170	0.174
E3	4.92	5.02	5.12	0.194	0.198	0.202
E4	3.80	3.90	4.00	0.150	0.154	0.157
E5	0.65	0.75	0.85	0.026	0.030	0.033
L	0.61	0.68	0.75	0.024	0.027	0.030
L1	1.00	1.07	1.15	0.039	0.042	0.045
W1	0.30	0.40	0.50	0.012	0.016	0.020
W4	0.32	0.37	0.42	0.013	0.015	0.017
z1	0.45	0.55	0.65	0.018	0.022	0.026
z2	1.81	1.91	2.01	0.071	0.075	0.079
θ	0°	-	5°	0°	-	5°

ECN: S19-0643-Rev. B, 05-Aug-2019  
DWG: 6073

**Note**

- Millimeter will govern



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