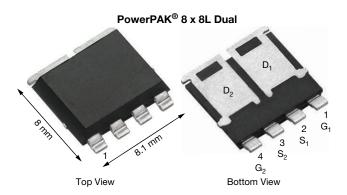


Vishay Siliconix

Automotive Dual N-Channel 40 V (D-S) 175 °C MOSFET



PRODUCT SUMMARY						
V _{DS} (V)	40					
$R_{DS(on)}$ (Ω) at $V_{GS} = 10 \text{ V}$	0.0039					
$R_{DS(on)}$ (Ω) at $V_{GS} = 4.5 \text{ V}$	0.0047					
I _D (A) per leg	100					
Configuration	Dual					
Package	PowerPAK 8 x 8L					

FEATURES

- TrenchFET® power MOSFET
- AEC-Q101 qualified
- 100 % R_q and UIS tested
- Fully lead (Pb)-free device
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE

G ₁ O S ₁	G_2 G_2 G_2 G_2 G_2 G_2 G_2 G_2 G_3 G_4 G_4 G_5 G_5 G_5
N-Channel MOSFET	N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS	(T _C = 25 °C, unles	s otherwise noted	1)	
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	40	V
Gate-source voltage		V _{GS}	± 20	V
Continuous drain current	T _C = 25 °C a	1	100	
Continuous drain current	T _C = 125 °C	I _D	60	
Continuous source current (diode conduction)	I _S	68	Α	
Pulsed drain current ^b	I _{DM}	400		
Single pulse avalanche current L = 0.1 mH		I _{AS}	50	
Single pulse avalanche energy	E _{AS}	125	mJ	
Maximum power dissipation ^b	T _C = 25 °C	В	75	W
Maximum power dissipation -	T _C = 125 °C	P_D	25	VV
Operating junction and storage temperature rai	T _J , T _{stg}	-55 to +175	°C	
Soldering recommendations (peak temperature	-	260	C	

THERMAL RESISTANCE RATINGS							
PARAMETER	SYMBOL	LIMIT	UNIT				
Junction-to-ambient PCE	B mount ^c R _{thJA}	80	°C/W				
Junction-to-case (drain)	R _{thJC}	2	G/VV				

Notes

- a. Package limited
- b. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. See solder profile (www.vishay.com/doc?73257). The PowerPAK 8 x 8L is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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PARAMETER	SYMBOL	TES	MIN.	TYP.	MAX.	UNIT	
Static							
Drain-source breakdown voltage	V _{DS}	V _{GS}	= 0, I _D = 250 μA	40	-	-	.,
Gate-source threshold voltage	V _{GS(th)}	V _{DS} =	= V _{GS} , I _D = 250 μA	1.5	2	2.5	V
Gate-source leakage	I _{GSS}	V _{DS} =	0 V, V _{GS} = ± 20 V	-	-	± 100	nA
		V _{GS} = 0 V	V _{DS} = 20 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{GS} = 0 V	V _{DS} = 40 V, T _J = 125 °C	-	-	50	μΑ
		V _{GS} = 0 V	V _{DS} = 40 V, T _J = 175 °C	-	-	150	
On-state drain current a	I _{D(on)}	V _{GS} = 10 V	$V_{DS} \ge 5 V$	40	-	-	Α
		V _{GS} = 10 V	I _D = 20 A	-	0.0034	0.0039	Ω
Due in account of the control of the	Б	V _{GS} = 4.5 V	I _D = 10 A	-	0.0039	0.0047	
Drain-source on-state resistance ^a	R _{DS(on)}	V _{GS} = 10 V	I _D = 20 A, T _J = 125 °C	-	-	0.0074	
		V _{GS} = 10 V	I _D = 20 A, T _J = 175 °C	-	-	0.0091	
Forward transconductance b		V _{DS} = 15 V, I _D = 15 A		-	105	1	S
Dynamic ^b							
Input capacitance	C _{iss}			-	4695	5900	
Output capacitance	C _{oss}	$V_{GS} = 0 V$	V V _{DS} = 20 V, f = 1 MHz		637	800	pF
Reverse transfer capacitance	C _{rss}	7		-	259	330	1
Total gate charge ^c	Qg			-	85	120	
Gate-source charge ^c	Q _{gs}	V _{GS} = 10 V	$V_{DS} = 20 \text{ V}, I_D = 40 \text{ A}$	-	10	-	nC
Gate-drain charge ^c	Q _{gd}	7		-	12	-	
Gate resistance	R_g	f = 1 MHz		0.7	1.5	3.0	Ω
Turn-on delay time ^c	t _{d(on)}			-	14	30	
Rise time ^c	t _r	$V_{DD} = 20 \text{ V}, \text{ R}_{L} = 0.5 \Omega$ $I_{D} \cong 40 \text{ A}, \text{ V}_{GEN} = 10 \text{ V}, \text{ R}_{g} = 1 \Omega$		-	7.5	15	ns
Turn-off delay time ^c	t _{d(off)}			-	30	60	
Fall time ^c	t _f			-	14	30	
Source-Drain Diode Ratings and Char	acteristics ^b	•					
Pulsed current ^a	I _{SM}			-	-	200	А
Forward voltage	V _{SD}	I _F = 40 A, V _{GS} = 0		_	1	1.2	V

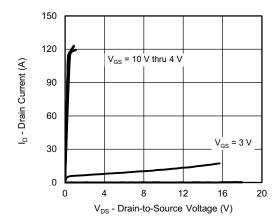
Notes

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

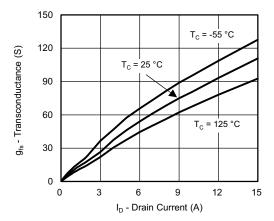
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



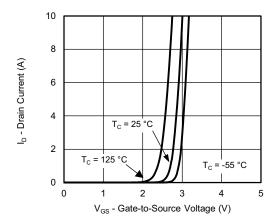
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



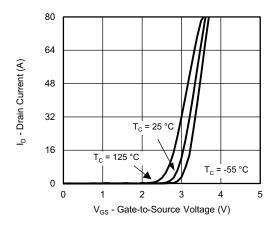
Output Characteristics



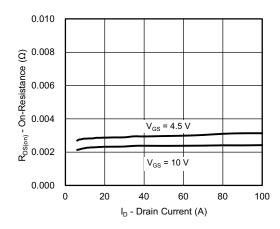
Transconductance



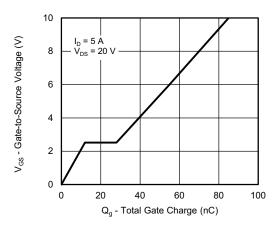
Transfer Characteristics



Transfer Characteristics



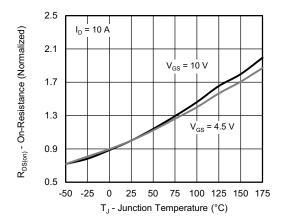
On-Resistance vs. Drain Current



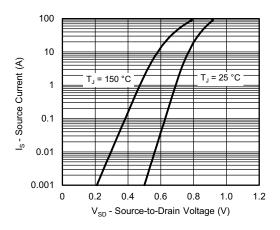
Gate Charge



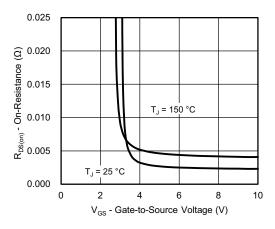
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



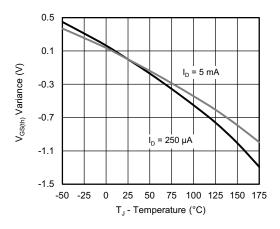
On-Resistance vs. Junction Temperature



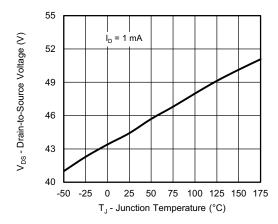
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



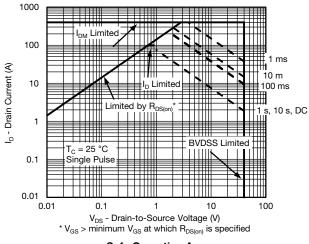
Threshold Voltage



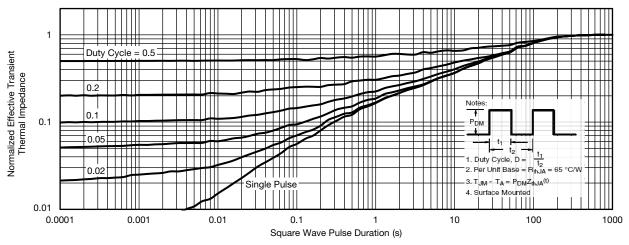
Drain Source Breakdown vs. Junction Temperature



THERMAL RATINGS ($T_A = 25$ °C, unless otherwise noted)



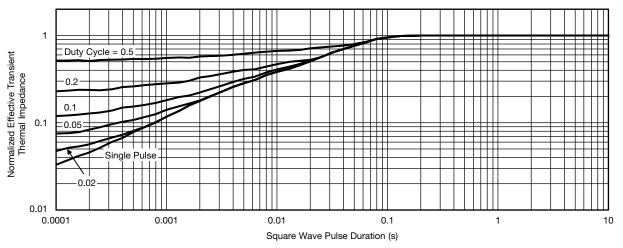
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



THERMAL RATINGS (T_A = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

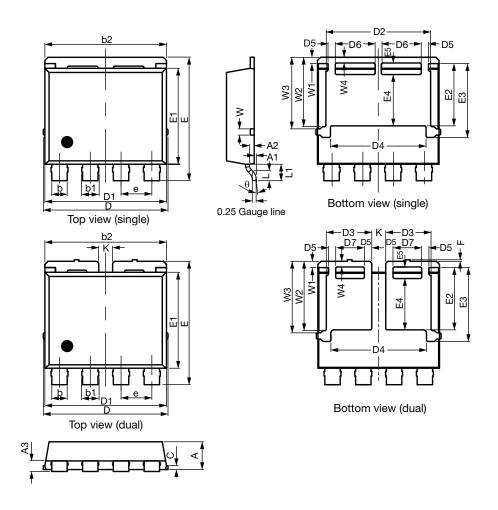
Note

- The characteristics shown in the two graphs
 - Normalized Transient Thermal Impedance Junction to Ambient (25 °C)
 - Normalized Transient Thermal Impedance Junction to Case (25 °C) are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg262796.



PowerPAK® 8 x 8L Case Outline



DIM		MILLIMETERS			INCHES		
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	1.70	1.80	1.90	0.067	0.071	0.075	
A1	0.00	0.08	0.13	0.000	0.003	0.005	
A2	0.25	0.30	0.35	0.010	0.012	0.014	
A3	0.55	0.62	0.70	0.022	0.024	0.028	
b	0.92	1.00	1.08	0.036	0.039	0.043	
b1	1.02	1.10	1.18	0.040	0.043	0.046	
b2	7.80	7.90	8.00	0.307	0.311	0.315	
С	0.20	0.25	0.30	0.008	0.010	0.012	
D	8.00	8.10	8.25	0.315	0.319	0.325	
D1	7.80	7.90	8.00	0.307	0.311	0.315	
D2	6.70	6.80	6.90	0.264	0.268	0.272	
D3	2.85	2.95	3.05	0.112	0.116	0.120	
D4	6.11	6.21	6.31	0.241	0.244	0.248	
D5	0.37	0.47	0.57	0.015	0.019	0.022	
D6	2.49	2.59	2.69	0.098	0.102	0.106	
D7	1.76	1.86	1.96	0.069	0.073	0.077	

Revision: 16-Oct-17 1 Document Number: 67734





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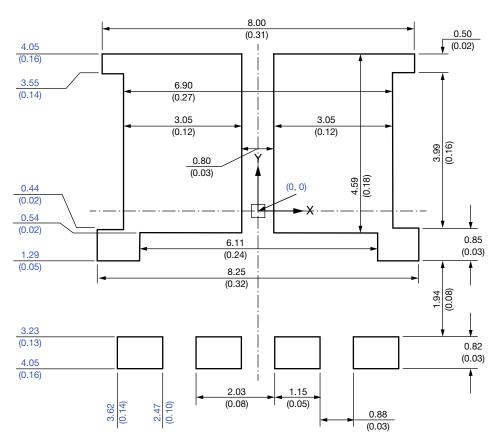
DIM.	MILLIMETERS			INCHES		
DIIVI.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
е	1.95	2.00	2.05	0.077	0.079	0.081
Е	7.90	8.00	8.10	0.311	0.315	0.319
E1	6.12	6.22	6.32	0.241	0.245	0.249
E2	3.94	4.04	4.14	0.140	0.159	0.163
E3	4.69	4.79	4.89	0.185	0.189	0.193
E4	3.23	3.33	3.43	0.127	0.131	0.135
E5	0.65	0.75	0.85	0.026	0.030	0.033
F	0.00	0.10	0.15	0.000	0.004	0.006
L	0.62	0.72	0.82	0.024	0.028	0.032
L1	0.92	1.07	1.22	0.036	0.042	0.048
K	0.80	0.90	1.00	0.031	0.035	0.039
W	0.30	0.40	0.50	0.012	0.016	0.020
W1	0.30	0.40	0.50	0.012	0.016	0.020
W2	4.39	4.49	4.59	0.173	0.177	0.181
W3	4.54	4.64	4.74	0.179	0.183	0.187
W4	0.32	0.37	0.42	0.013	0.015	0.017
θ	6°	10°	14°	6°	10°	14°

C17-1388-Rev. B, 16-Oct-17

DWG: 6026



Recommended Minimum PADs for PowerPAK® 8 x 8L Dual



Dimensions in millimeters (inches)

Note

• Linear dimensions are in black, the same information is provided in ordinate dimensions which are in blue.



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