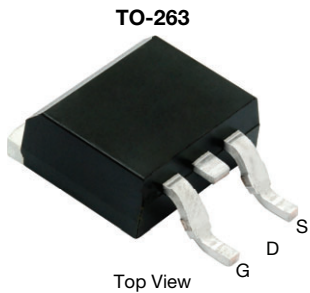


## Automotive N-Channel 60 V (D-S) 175 °C MOSFET



### FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- 100 % R<sub>g</sub> and UIS tested
- AEC-Q101 qualified
- Material categorization:  
for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



PRODUCT SUMMARY	
V <sub>DS</sub> (V)	60
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.0039
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 4.5 V	0.0050
I <sub>D</sub> (A)	100
Configuration	Single
Package	TO-263

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V <sub>DS</sub>	60	V
Gate-source voltage		V <sub>GS</sub>	± 20	
Continuous drain current	T <sub>C</sub> = 25 °C <sup>a</sup>	I <sub>D</sub>	100	A
	T <sub>C</sub> = 125 °C		80	
Continuous source current (diode conduction) <sup>a</sup>		I <sub>S</sub>	100	
Pulsed drain current <sup>b</sup>		I <sub>DM</sub>	320	
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	48	
Single pulse avalanche energy		E <sub>AS</sub>	115	mJ
Maximum power dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	150	W
	T <sub>C</sub> = 125 °C		50	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>c</sup>	R <sub>thJA</sub>	40	°C/W
Junction-to-case (drain)		R <sub>thJC</sub>	1	

### Notes

- Package limited
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- When mounted on 1" square PCB (FR4 material)



SPECIFICATIONS (T <sub>C</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	60	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	2.0	2.5	
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V	-	-	1	μA
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V, T <sub>J</sub> = 125 °C	-	-	50	
		V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 60 V, T <sub>J</sub> = 175 °C	-	-	300	μA
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> ≥ 5 V	100	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	-	0.0032	0.0039	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A	-	0.0041	0.0050	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C	-	-	0.0063	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C	-	-	0.0075	
Forward transconductance <sup>b</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 20 A	-	97	-	S
<b>Dynamic <sup>b</sup></b>						
Input capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz	-	4425	6100	pF
Output capacitance	C <sub>oss</sub>		-	1989	2800	
Reverse transfer capacitance	C <sub>rss</sub>		-	67	95	
Total gate charge <sup>c</sup>	Q <sub>g</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 30 V, I <sub>D</sub> = 50 A	-	60	90	nC
Gate-source charge <sup>c</sup>	Q <sub>gs</sub>		-	16.3	-	
Gate-drain charge <sup>c</sup>	Q <sub>gd</sub>		-	4.8	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	0.6	1.24	1.9	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 30 V, R <sub>L</sub> = 0.6 Ω I <sub>D</sub> ≅ 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 1 Ω	-	15	25	ns
Rise time <sup>c</sup>	t <sub>r</sub>		-	7	15	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>		-	33	50	
Fall time <sup>c</sup>	t <sub>f</sub>		-	7	15	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>						
Pulsed current <sup>a</sup>	I <sub>SM</sub>		-	-	320	A
Forward voltage	V <sub>SD</sub>	I <sub>F</sub> = 25 A, V <sub>GS</sub> = 0 V	-	0.81	1.5	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = 30 A, di/dt = 100 A/μs	-	42	85	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	34	70	nC
Reverse recovery fall time	t <sub>a</sub>		-	15	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	27	-	
Body diode peak reverse recovery current	I <sub>RM(REC)</sub>			-	-1.45	-

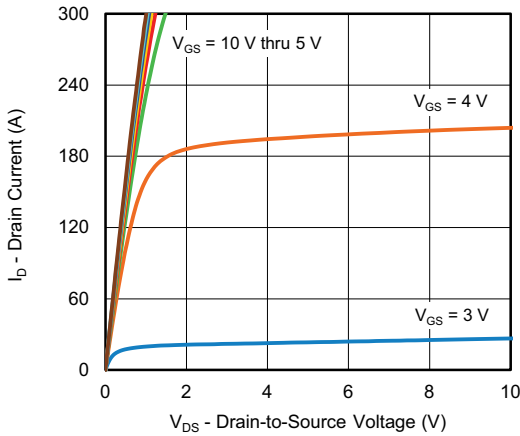
**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

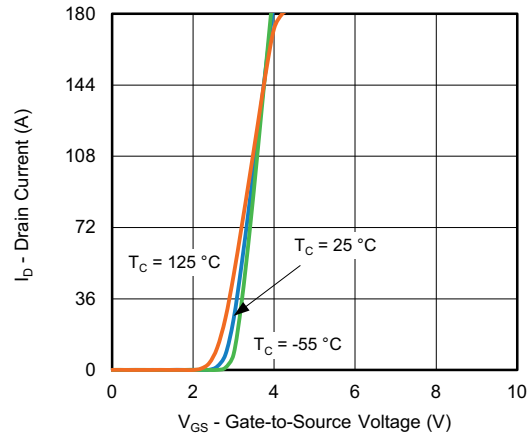
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



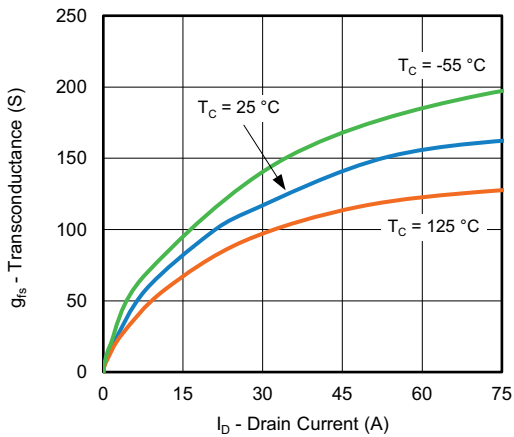
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



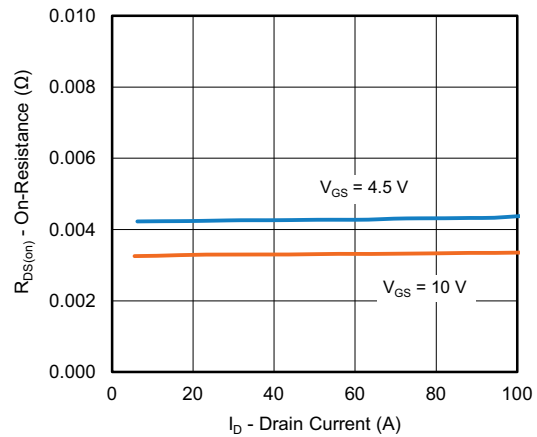
Output Characteristics



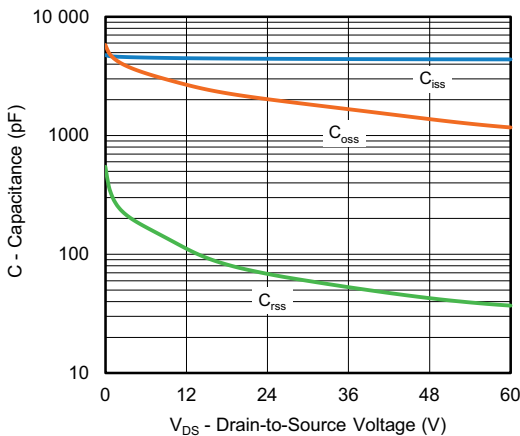
Transfer Characteristics



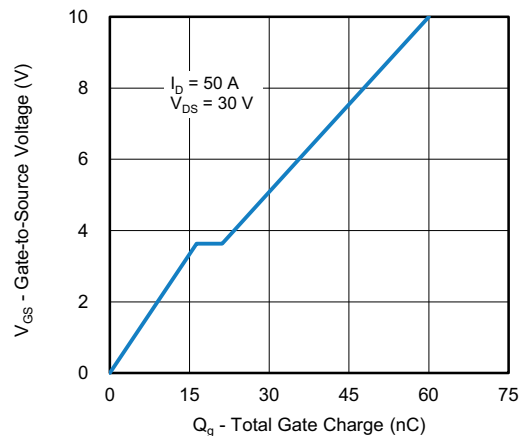
Transconductance



On-Resistance vs. Drain Current



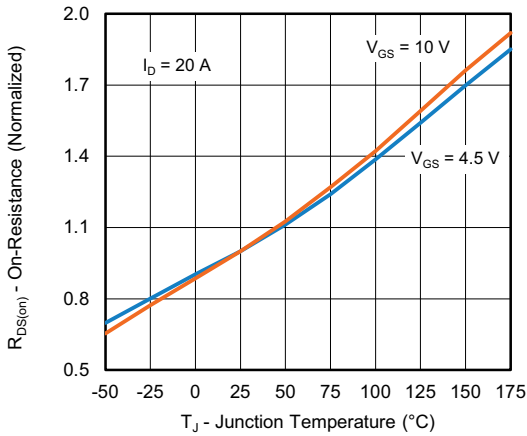
Capacitance



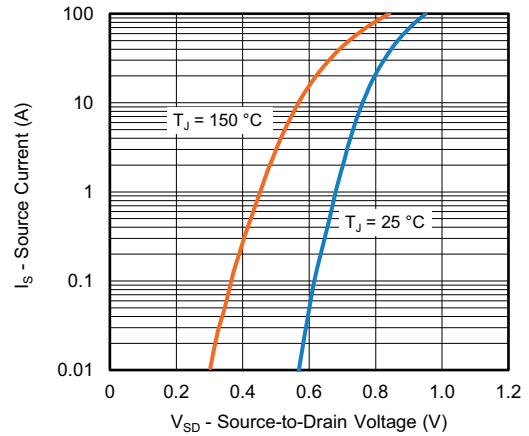
Gate Charge



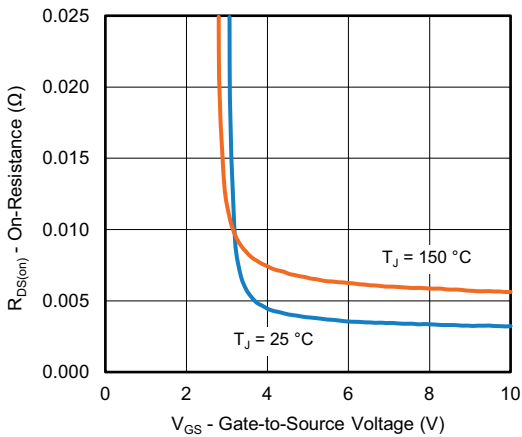
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



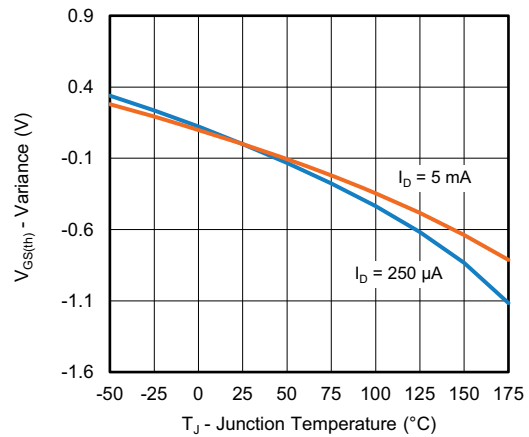
On-Resistance vs. Junction Temperature



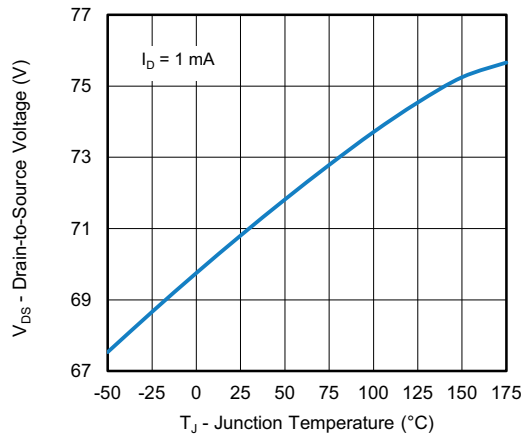
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



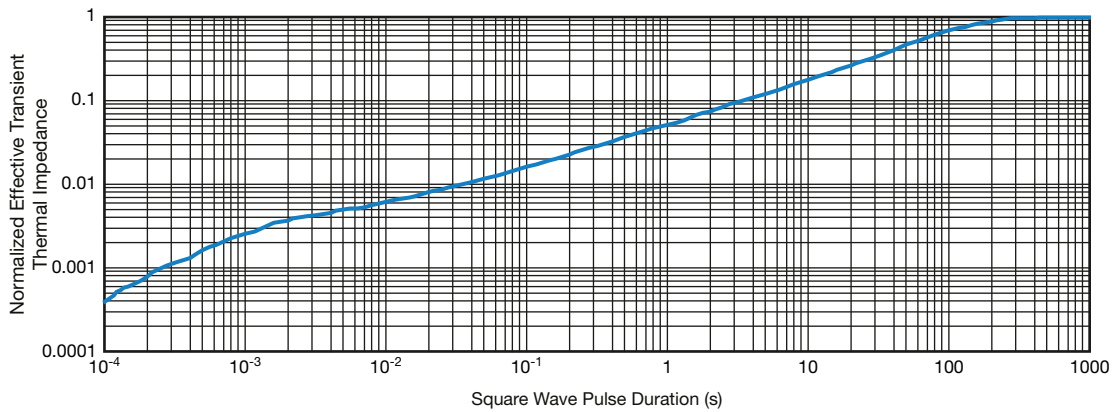
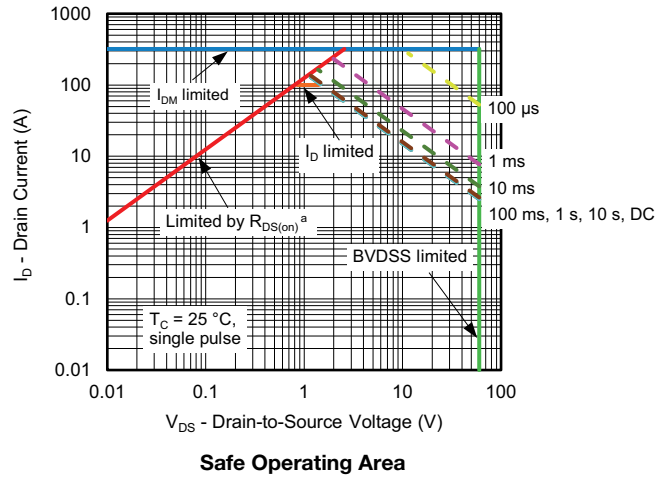
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



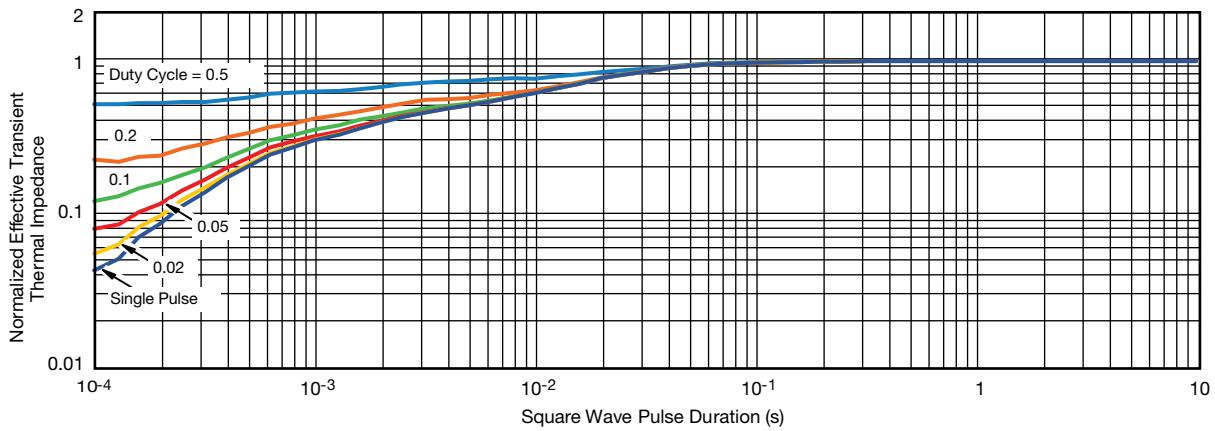
**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Note**

a.  $V_{GS} >$  minimum  $V_{GS}$  at which  $R_{DS(on)}$  is specified



**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient ( $25\text{ }^\circ\text{C}$ )
  - Normalized Transient Thermal Impedance Junction-to-Case ( $25\text{ }^\circ\text{C}$ )
 are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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# TO-263 (D<sup>2</sup>PAK): 3-LEAD



DIM.	INCHES		MILLIMETERS		
	MIN.	MAX.	MIN.	MAX.	
A	0.160	0.190	4.064	4.826	
b	0.020	0.039	0.508	0.990	
b1	0.020	0.035	0.508	0.889	
b2	0.045	0.055	1.143	1.397	
c*	Thin lead	0.013	0.018	0.330	0.457
	Thick lead	0.023	0.028	0.584	0.711
c1	Thin lead	0.013	0.017	0.330	0.431
	Thick lead	0.023	0.027	0.584	0.685
c2	0.045	0.055	1.143	1.397	
D	0.340	0.380	8.636	9.652	
D1	0.220	0.240	5.588	6.096	
D2	0.038	0.042	0.965	1.067	
D3	0.045	0.055	1.143	1.397	
D4	0.044	0.052	1.118	1.321	
E	0.380	0.410	9.652	10.414	
E1	0.245	-	6.223	-	
E2	0.355	0.375	9.017	9.525	
E3	0.072	0.078	1.829	1.981	
e	0.100 BSC		2.54 BSC		
K	0.045	0.055	1.143	1.397	
L	0.575	0.625	14.605	15.875	
L1	0.090	0.110	2.286	2.794	
L2	0.040	0.055	1.016	1.397	
L3	0.050	0.070	1.270	1.778	
L4	0.010 BSC		0.254 BSC		
M	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13					
DWG: 5843					

**Notes**

- Plane B includes maximum features of heat sink tab and plastic.
- No more than 25 % of L1 can fall above seating plane by max. 8 mils.
- Pin-to-pin coplanarity max. 4 mils.
- \*: Thin lead is for SUB, SYB.  
Thick lead is for SUM, SYM, SQM.
- Use inches as the primary measurement.
- This feature is for thick lead.

**RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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