Vishay Siliconix

# Automotive P-Channel 30 V (D-S) 175 °C MOSFET

# 

Marking code: Q030

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	-30			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -10 \text{ V}$	0.021			
$R_{DS(on)}(\Omega)$ at $V_{GS} = -4.5 \text{ V}$	0.060			
I <sub>D</sub> (A)	-16			
Configuration	Single			
Package	PowerPAK 1212-8W			

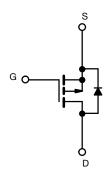
#### **FEATURES**

- TrenchFET® power MOSFET
- AEC-Q101 qualified <sup>d</sup>
- 100 % Rq and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912





ROHS COMPLIANT HALOGEN FREE



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (To	$_{\rm C}$ = 25 °C, unles	ss otherwise noted)			
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		$V_{DS}$	-30	V	
Gate-source voltage		$V_{GS}$	± 20	V	
Continuous drain current <sup>a</sup>	T <sub>C</sub> = 25 °C	-	-16		
Continuous drain current "	T <sub>C</sub> = 125 °C	I <sub>D</sub>	-16		
Continuous source current (diode conduction) <sup>a</sup>		I <sub>S</sub>	-16	Α	
Pulsed drain current b		I <sub>DM</sub>	-64		
Single pulse avalanche current	L = 0.1 mH	I <sub>AS</sub>	-22		
Single pulse avalanche energy	L = 0.111111	E <sub>AS</sub>	24	mJ	
Maximum power dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	В	62.5	W	
Maximum power dissipation -	T <sub>C</sub> = 125 °C	$P_{D}$	20	VV	
Operating junction and storage temperature range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C	
Soldering recommendations (peak temperature) e, f			260	C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-ambient	PCB mount <sup>c</sup>	R <sub>thJA</sub>	81	°C/W
Junction-to-case (drain)		$R_{thJC}$	2.4	G/ VV

#### **Notes**

- a. Package limited
- b. Pulse test; pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2 %
- c. When mounted on 1" square PCB (FR4 material)
- d. Parametric verification ongoing
- e. See solder profile (<a href="https://www.vishay.com/doc?73257">www.vishay.com/doc?73257</a>). The PowerPAK 1212-8W is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- f. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components



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<b>SPECIFICATIONS</b> (T <sub>C</sub> = 25 °C	, unless otherv	vise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> =	: 0 V, I <sub>D</sub> = -250 μA	-30	-	-	V
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	$V_{DS} = V_{GS}, I_D = -250 \mu A$		-2.0	-2.5	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	$0 \text{ V}, \text{ V}_{GS} = \pm 20 \text{ V}$	1	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = -30 V	1	-	-1	
Zero gate voltage drain current	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS} = -30 \text{ V}, T_{J} = 125 ^{\circ}\text{C}$	-	-	-50	μΑ
		$V_{GS} = 0 V$	V <sub>DS</sub> = -30 V, T <sub>J</sub> = 175 °C	-	-	-150	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>GS</sub> = -10 V	$V_{DS} \le -5 \text{ V}$	-20	-	-	Α
		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -12 A	-	0.018	0.021	
Drain-source on-state resistance b		V <sub>GS</sub> = -10 V	I <sub>D</sub> = -12 A, T <sub>J</sub> = 125 °C	-	-	0.031	
Drain-source on-state resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V	I <sub>D</sub> = -12 A, T <sub>J</sub> = 175 °C	-	-	0.035	Ω
		$V_{GS} = -4.5 \text{ V}$	I <sub>D</sub> = -9 A	-	0.040	0.060	
Forward transconductance b	9 <sub>fs</sub>	V <sub>DS</sub>	= -15 V, I <sub>D</sub> = -7 A	-	18	-	S
Dynamic <sup>b</sup>							
Input capacitance	C <sub>iss</sub>			-	1575	1975	
Output capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	$V_{DS} = -15 \text{ V}, f = 1 \text{ MHz}$	-	335	418	pF
Reverse transfer capacitance	C <sub>rss</sub>			1	240	300	
Total gate charge <sup>c</sup>	Qg			-	17	26	
Gate-source charge c	Q <sub>gs</sub>	$V_{GS} = -4.5 \text{ V}$	$V_{DS} = -15 \text{ V}, I_{D} = -10.5 \text{ A}$	-	5.9	9	nC
Gate-drain charge <sup>c</sup>	$Q_{gd}$			-	9.2	14	
Gate resistance	R <sub>g</sub>		f = 1 MHz	1.6	3.43	6	Ω
Turn-on delay time <sup>c</sup>	t <sub>d(on)</sub>			-	65	100	
Rise time <sup>c</sup>	t <sub>r</sub>	$V_{DD} =$	-15 V, $R_L = 1.78 \Omega$	-	43	65	
Turn-off delay time <sup>c</sup>	t <sub>d(off)</sub>	$I_D \cong -8.4 \text{ A}, V_{GEN} = -4.5 \text{ V}, R_g = 1 \Omega$		-	23	34	- ns -
Fall time <sup>c</sup>	t <sub>f</sub>			-	15	22	
Source-Drain Diode Ratings and Char	acteristics <sup>b</sup>						
Pulsed current <sup>a</sup>	I <sub>SM</sub>			-		-64	Α
Forward voltage	$V_{SD}$	I <sub>F</sub> =	-8.8 A, V <sub>GS</sub> = 0 V	-	-0.8	-1.2	V

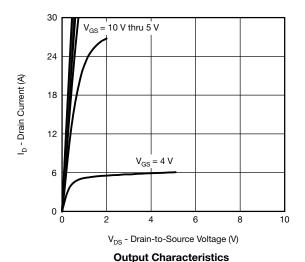
#### **Notes**

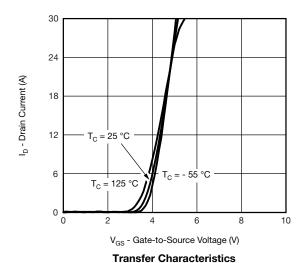
- a. Pulse test; pulse width  $\leq 300~\mu\text{s},$  duty cycle  $\leq 2~\%$
- b. Guaranteed by design, not subject to production testing
- c. Independent of operating temperature

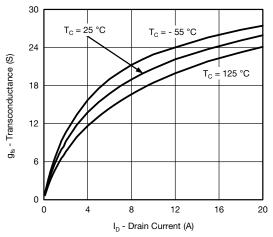
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

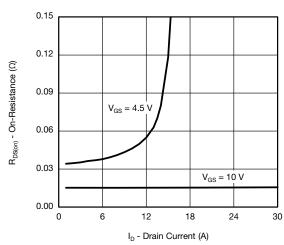


## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)

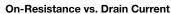


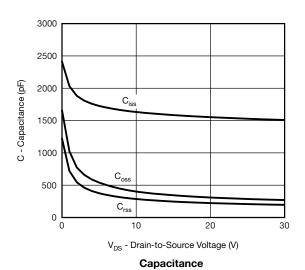


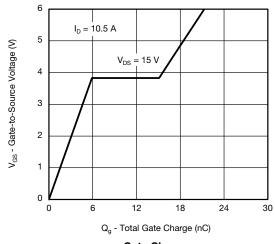






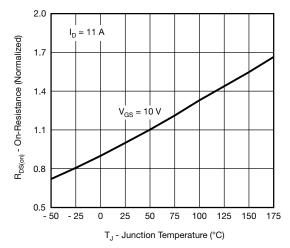




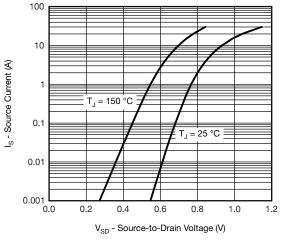




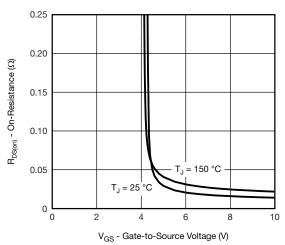
## **TYPICAL CHARACTERISTICS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



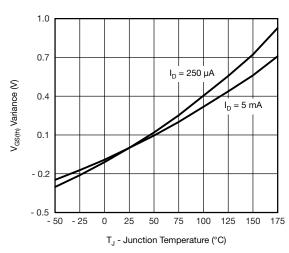
On-Resistance vs. Junction Temperature



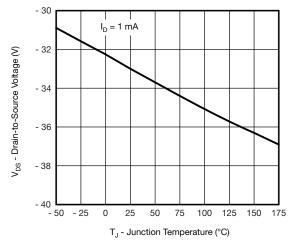
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



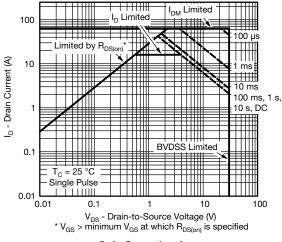
**Threshold Voltage** 



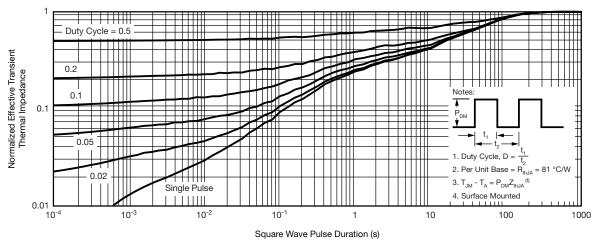
Drain Source Breakdown vs. Junction Temperature



## **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



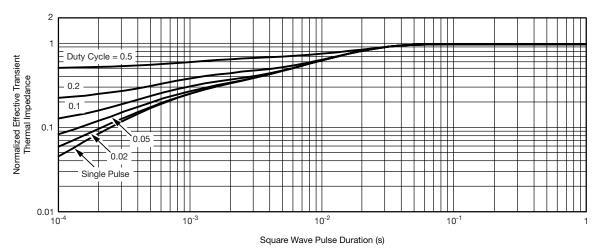
Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient



#### THERMAL RATINGS (T<sub>A</sub> = 25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

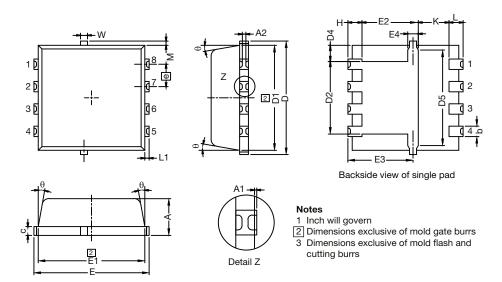
- The characteristics shown in the two graphs
  - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
  - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions

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# PowerPAK® 1212-8W Case Outline



DIM.	MILLIMETERS			INCHES			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.97	1.04	1.12	0.038	0.041	0.044	
A1	0	-	0.05	0	-	0.002	
A2	0	-	0.13	0	-	0.005	
b	0.23	0.30	0.41	0.009	0.012	0.016	
С	0.23	0.28	0.33	0.009	0.011	0.013	
D	3.20	3.30	3.40	0.126	0.130	0.134	
D1	2.95	3.05	3.15	0.116	0.120	0.124	
D2	1.98	2.11	2.24	0.078	0.083	0.088	
D4	0.47 typ.				0.0185 typ.		
D5		2.3 typ.		0.090 typ.			
Е	3.20	3.30	3.40	0.126	0.130	0.134	
E1	2.95	3.05	3.15	0.116	0.120	0.124	
E2	1.47	1.60	1.73	0.058	0.063	0.068	
E3	1.75	1.85	1.98	0.069	0.073	0.078	
E4		0.34 typ.			0.013 typ.		
е		0.65 BSC.		0.026 BSC			
K		0.86 typ.		0.034 typ.			
Н	0.30	0.41	0.51	0.012	0.016	0.020	
L	0.30	0.43	0.56	0.012	0.017	0.022	
L1	0.06	0.13	0.20	0.002	0.005	0.008	
θ	0°	-	12°	0°	-	12°	
W	0.15	0.25	0.36	0.006	0.010	0.014	
М		0.125 typ.			0.005 typ.		

DWG: 6032



## RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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