



# N-Channel 250-V (D-S) 175 °C MOSFET

PRODUCT SUMMARY		
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
250	0.058 at $V_{GS} = 10$ V	45
	0.062 at $V_{GS} = 6$ V	43

## FEATURES

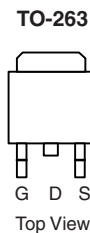
- TrenchFET<sup>®</sup> Power MOSFETS
- 175 °C Junction Temperature
- New Low Thermal Resistance Package



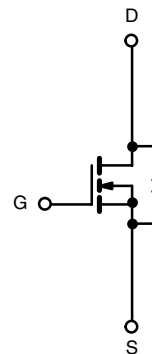
RoHS COMPLIANT

## APPLICATIONS

- Primary Side Switch
- Plasma Display Panel Sustainer Function



Ordering Information: SUM45N25-58-E3 (Lead (Pb)-free)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_C = 25$ °C, unless otherwise noted				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	250	V
Typical Avalanche Voltage <sup>d</sup>		$V_{DS(Avalanche)TYP}$	300	
Gate-Source Voltage		$V_{GS}$	$\pm 30$	
Continuous Drain Current ( $T_J = 175$ °C)	$T_C = 25$ °C	$I_D$	45	A
	$T_C = 125$ °C		25	
Pulsed Drain Current		$I_{DM}$	90	
Avalanche Current		$I_{AR}$	35	
Repetitive Avalanche Energy <sup>a</sup>	L = 0.1 mH	$E_{AR}$	61	mJ
Maximum Power Dissipation <sup>a</sup>	$T_C = 25$ °C	$P_D$	375 <sup>b</sup>	W
	$T_A = 25$ °C <sup>c</sup>		3.75	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to 175	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mount) <sup>c</sup>	$R_{thJA}$	40	°C/W
Junction-to-Case (Drain)	$R_{thJC}$	0.4	

Notes:

- Duty cycle  $\leq 1$  %.
- See SOA curve for voltage derating.
- When Mounted on 1" square PCB (FR-4 material).
- Guaranteed by design

<b>SPECIFICATIONS</b> $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{DS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	250			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2		4	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 30\text{ V}$			$\pm 250$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 250\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 250\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$			50	
		$V_{DS} = 250\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 175\text{ }^\circ\text{C}$			250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$ , $V_{GS} = 10\text{ V}$	70			A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$		0.047	0.058	$\Omega$
		$V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$			0.121	
		$V_{GS} = 10\text{ V}$ , $I_D = 20\text{ A}$ , $T_J = 175\text{ }^\circ\text{C}$			0.163	
		$V_{GS} = 6\text{ V}$ , $I_D = 15\text{ A}$		0.049	0.062	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 20\text{ A}$		70		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$		5000		$\mu\text{F}$
Output Capacitance	$C_{oss}$			300		
Reverse Transfer Capacitance	$C_{rss}$			170		
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 125\text{ V}$ , $V_{GS} = 10\text{ V}$ , $I_D = 45\text{ A}$		95	140	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			28		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			34		
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		1.6		$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 100\text{ V}$ , $R_L = 2.78\text{ }\Omega$ $I_D \equiv 45\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 2.5\text{ }\Omega$		22	35	ns
Rise Time <sup>c</sup>	$t_r$			220	330	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			40	60	
Fall Time <sup>c</sup>	$t_f$			145	220	
<b>Source-Drain Diode Ratings and Characteristics</b> ( $T_C = 25\text{ }^\circ\text{C}$ ) <sup>b</sup>						
Continuous Current	$I_S$				45	A
Pulsed Current	$I_{SM}$				70	
Forward Voltage <sup>a</sup>	$V_{SD}$	$I_F = 45\text{ A}$ , $V_{GS} = 0\text{ V}$		1.0	1.5	V
Reverse Recovery Time	$t_{rr}$	$I_F = 45\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		150	225	ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			12	18	A
Reverse Recovery Charge	$Q_{rr}$			0.9	2	$\mu\text{C}$

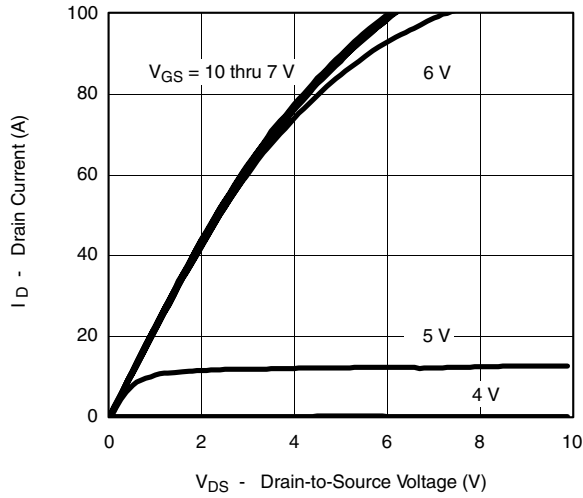
## Notes:

- Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

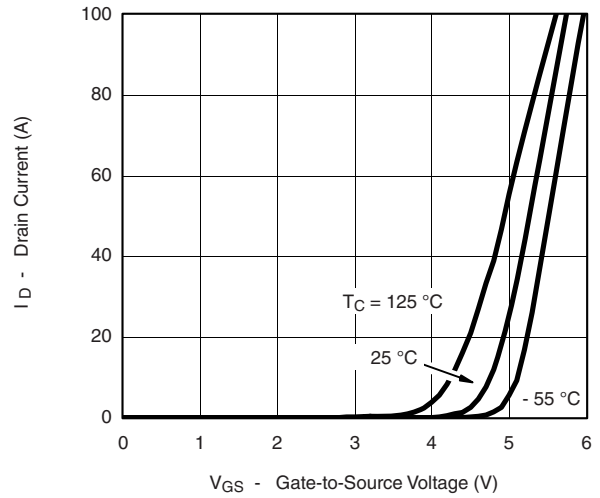
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



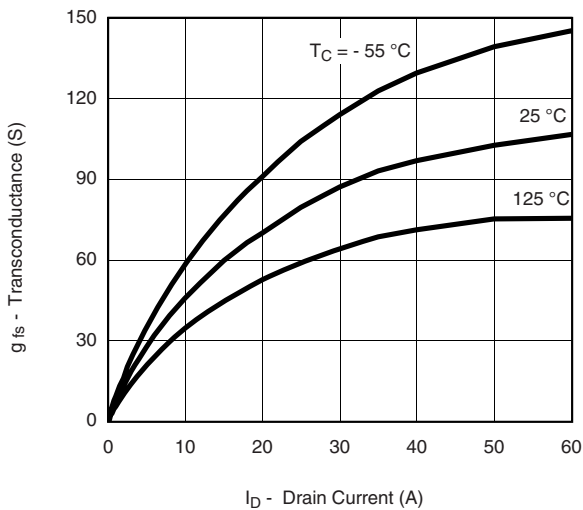
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



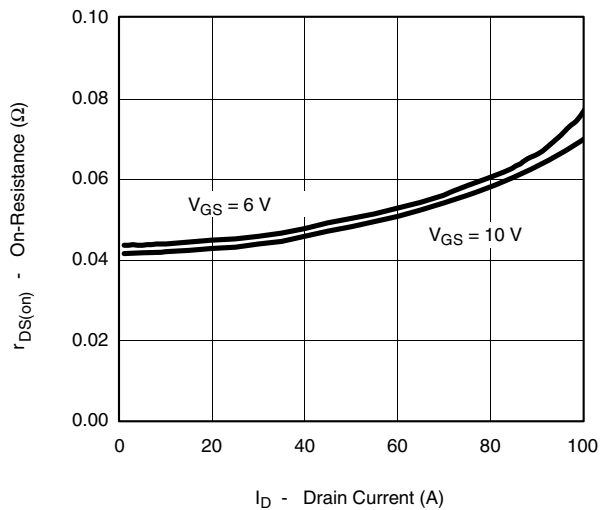
**Output Characteristics**



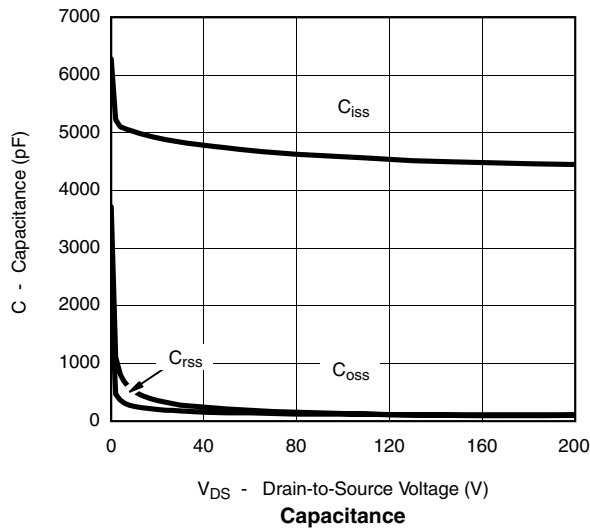
**Transfer Characteristics**



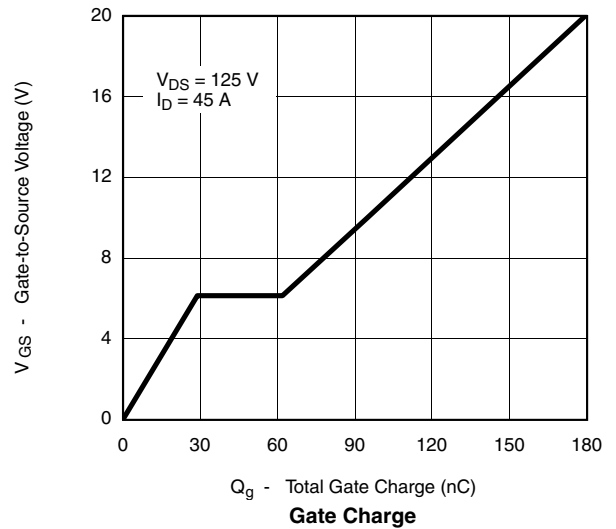
**Transconductance**



**On-Resistance vs. Drain Current**



**Capacitance**



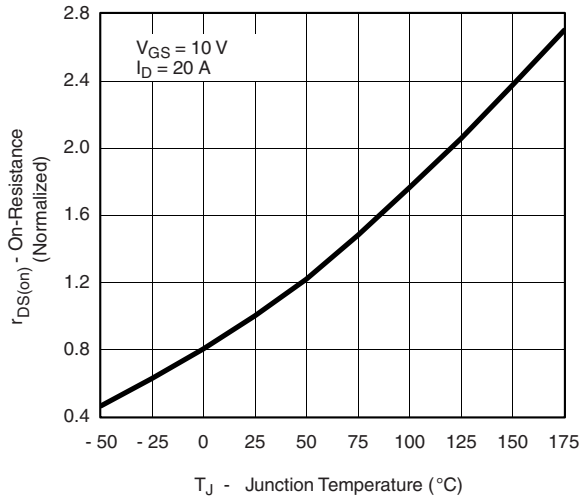
**Gate Charge**

# SUM45N25-58

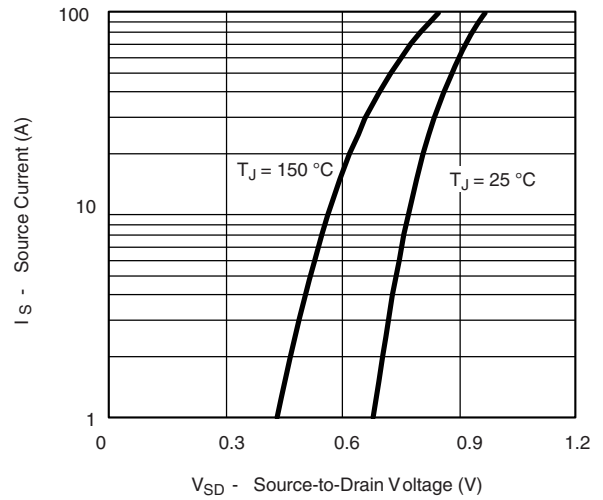


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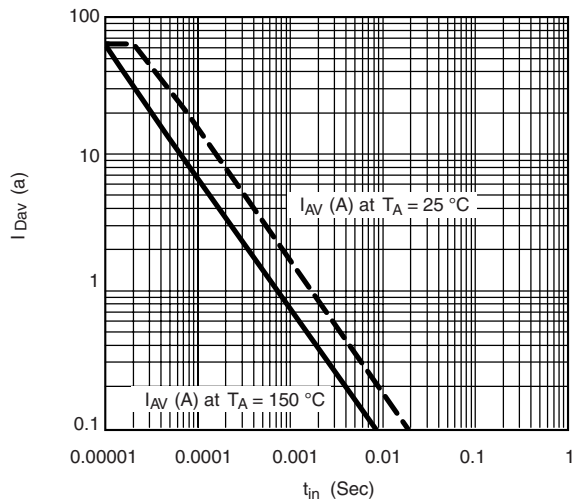
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



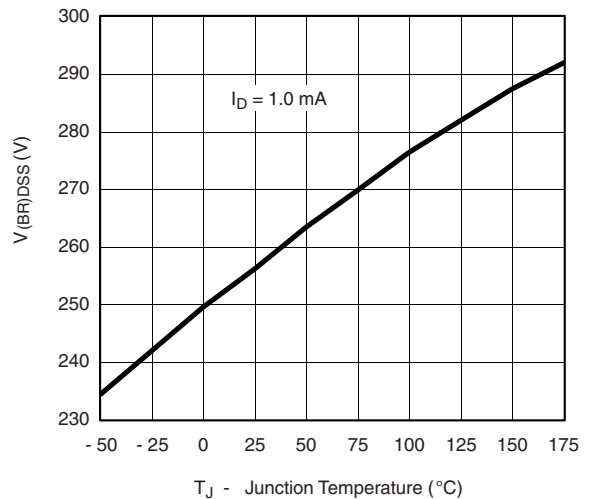
**On-Resistance vs. Junction Temperature**



**Source-Drain Diode Forward Voltage**



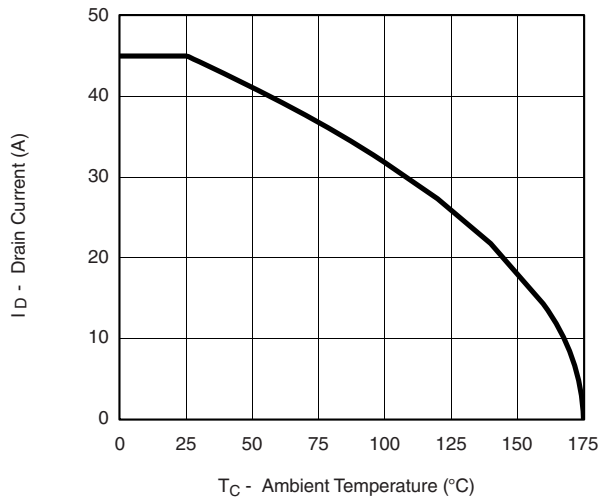
**Avalanche Current vs. Time**



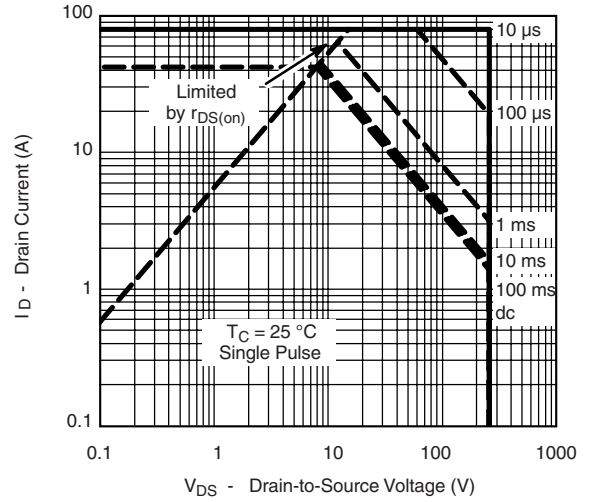
**Drain Source Breakdown vs. Junction Temperature**



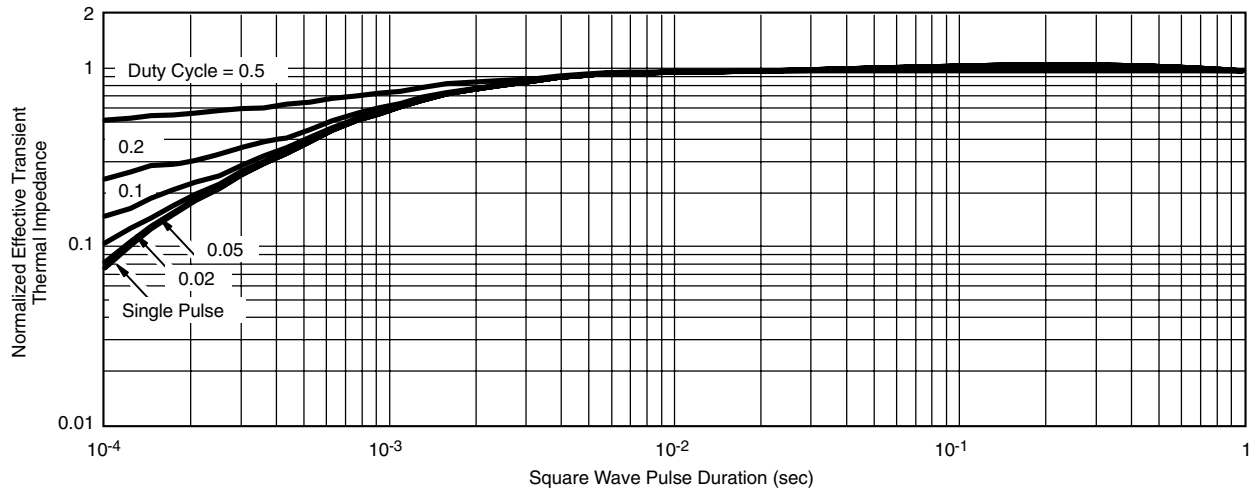
**THERMAL RATINGS**



**Maximum Avalanche and Drain Current vs. Case Temperature**



**Safe Operating Area, Case Temperature**



**Normalized Thermal Transient Impedance, Junction-to-Case**

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