

COMPLIANT

## N-Channel 20-V (D-S) 175 °C MOSFET

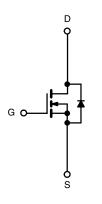
PRODUCT SUMMARY				
V <sub>(BR)DSS</sub> (V)	(BR)DSS (V) r <sub>DS(on)</sub> (Ω)			
20	0.0039 at V <sub>GS</sub> = 10 V	60		
	0.0052 at V <sub>GS</sub> = 4.5 V	60		

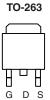
#### **FEATURES**

- TrenchFET<sup>®</sup> Power MOSFET
- 175 °C Junction Temperature
- 100 % R<sub>g</sub> Tested
- 100 % UIS Tested

#### **APPLICATIONS**

• OR-ing





Top View

DRAIN connected to TAB

Ordering Information: SUM60N02-3m9P-E3 (Lead (Pb)-free)

N-Channel MOSFET

<b>ABSOLUTE MAXIMUM RATINGS</b> $T_A = 25 \degree C$ , unless otherwise noted					
Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V <sub>DS</sub>	20	v	
Gate-Source Voltage		V <sub>GS</sub>	± 20	- V	
Continuous Drain Current (T 175 %C)	T <sub>C</sub> = 25 °C	1-	60 <sup>a</sup>		
Continuous Drain Current ( $T_J = 175 \ ^{\circ}C$ )	T <sub>C</sub> = 100 °C	– I <sub>D</sub> –	60 <sup>a</sup>	•	
Pulsed Drain Current		I <sub>DM</sub>	120	A	
Single Pulse Avalanche Current	L = 0.1 mH	I <sub>AS</sub>	50		
Single Pulse Avalanche Energy		E <sub>AS</sub>	125	mJ	
	T <sub>C</sub> = 25 °C	P	120 <sup>c</sup>		
Maximum Power Dissipation <sup>b</sup>	T <sub>A</sub> = 25 °C <sup>d</sup>	– P <sub>D</sub> –	3.75	W	
Operating Junction and Storage Temperature Ra	nge	T <sub>J</sub> , T <sub>stg</sub>	- 55 to 175	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Limit	Unit		
Junction-to-Ambient (PCB Mount) <sup>d</sup>	R <sub>thJA</sub>	40	°C/W		
Junction-to-Case	R <sub>thJC</sub>	1.25			

Notes:

a. Package limited.

a. Factage innica.
b. Duty cycle ≤ 1 %.
c. See SOA curve for voltage derating.
d. When mounted on 1" square PCB (FR-4 material).

# SUM60N02-3m9P

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static			1				
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{DS} = 0 \text{ V}, \text{ I}_{D} = 250 \mu\text{A}$	20				
Gate-Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \ \mu A$	1.0		3	V	
Gate-Body Leakage	I <sub>GSS</sub>	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = 20 V, V_{GS} = 0 V$			1		
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$			50	μA	
		$V_{DS} = 20 \text{ V}, \text{ V}_{GS} = 0 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$			250		
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	100			Α	
		$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0031	0.0039	Ω	
		$V_{GS}$ = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C			0.0059		
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	$V_{GS}$ = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C			0.007		
		$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 20 \text{ A}$		0.0042	0.0052		
Forward Transconductance <sup>a</sup>	9 <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A		95		S	
Dynamic <sup>b</sup>			•	•	• •		
Input Capacitance	C <sub>iss</sub>			5950		pF	
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 10 V, f = 1 MHz		985			
Reverse Transfer Capacitance	C <sub>rss</sub>			365			
Total Gate Charge <sup>b</sup>	Qg			33	50	nC	
Gate-Source Charge <sup>b</sup>	Q <sub>gs</sub>	$V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_{D}$ = 50 A		18			
Gate-Drain Charge <sup>b</sup>	Q <sub>gd</sub>			7			
Gate Resistance	R <sub>g</sub>		0.75	1.5	2.3	Ω	
Turn-On Delay Time <sup>b</sup>	t <sub>d(on)</sub>			15	25		
Rise Time <sup>b</sup>	t <sub>r</sub>	$V_{DD}$ = 10 V, $R_L$ = 0.2 $\Omega$		7	11	ns	
Turn-Off Delay Time <sup>b</sup>	t <sub>d(off)</sub>	$\text{I}_\text{D} \cong$ 50 A, $\text{V}_\text{GEN}$ = 10 V, $\text{R}_\text{g}$ = 1.0 $\Omega$		35	55		
Fall Time <sup>b</sup>	t <sub>f</sub>			8	12		
Source-Drain Diode Ratings and Cha	aracteristics T	$T_{\rm C} = 25 \ ^{\circ}{\rm C}^{\rm C}$					
Continuous Current	ا <sub>S</sub>				60	- A	
Pulsed Current	I <sub>SM</sub>				100		
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	$I_{F} = 20 \text{ A}, V_{GS} = 0 \text{ V}$		0.85	1.5	V	
Reverse Recovery Time	t <sub>rr</sub>			45	90	ns	
Peak Reverse Recovery Current	I <sub>RM</sub>	$I_{F} = 20 \text{ A}, \text{ di/dt} = 100 \text{ A/}\mu\text{s}$		1.7	3.4	Α	
Reverse Recovery Charge	Q <sub>rr</sub>	$\neg$		0.039	0.155	μC	

Notes:

a. Pulse test; pulse width  $\leq$  300  $\mu s,$  duty cycle  $\leq$  2 %

b. Independent of operating temperature.

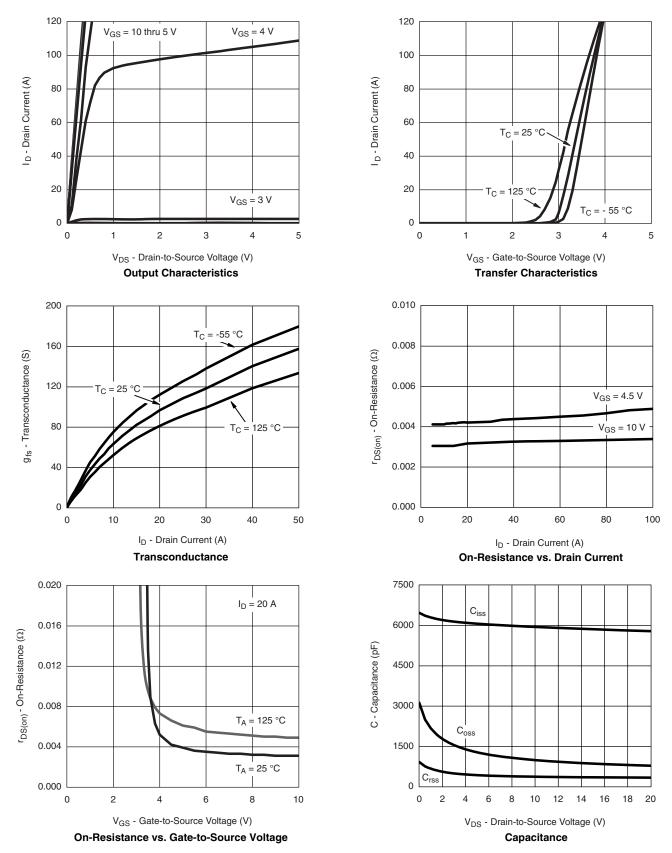
c. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



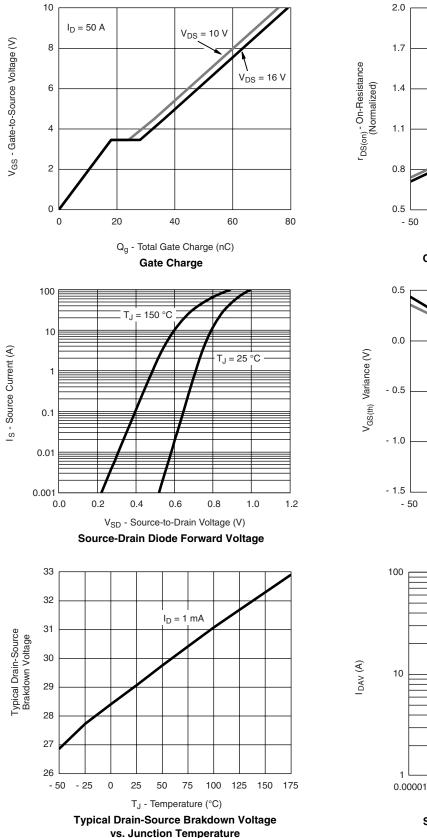
### TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

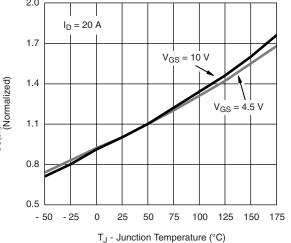
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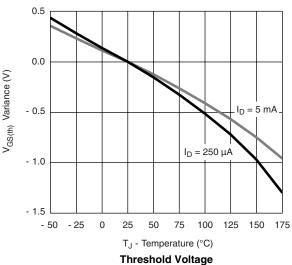
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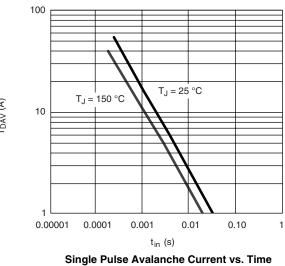


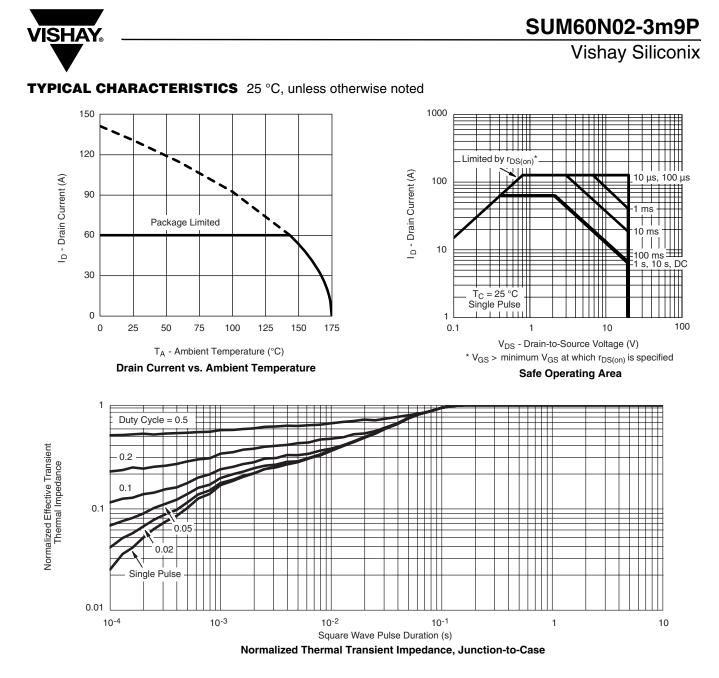


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**On-Resistance vs. Junction Temperature** 







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TO-263 (D<sup>2</sup>PAK): 3-LEAD









DETAIL A (ROTATED 90°)



		INCHES		MILLIN	IETERS	
DIM.		MIN.	MAX.	MIN.	MAX.	
А		0.160	0.190	4.064	4.826	
	b	0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
с*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
D4		0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
	е	0.100	0.100 BSC 2.54 BS		BSC	
	К	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
	L1	0.090	0.110	2.286	2.794	
	L2	0.040	0.055	1.016	1.397	
	L3	0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
	М	M - 0.002 - 0.050		0.050		
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843						

#### Notes

- 1. Plane B includes maximum features of heat sink tab and plastic. 2. No more than 25 % of L1 can fall above seating plane by
- max. 8 mils.3. Pin-to-pin coplanarity max. 4 mils.
- 4. \*: Thin lead is for SUB, SYB.
  - Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

This feature is for thick lead.

Revison: 30-Sep-13



### **RECOMMENDED MINIMUM PADS FOR D<sup>2</sup>PAK: 3-Lead**



Recommended Minimum Pads Dimensions in Inches/(mm)

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