

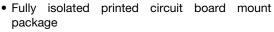
IGBT SIP Module (Fast IGBT)



IMS-2

PRIMARY CHARACTERISTICS						
OUTPUT CURRENT IN A TYPICAL 5.0 kHz MOTOR DRIVE						
$V_{\sf CES}$	600 V					
I_{RMS} per phase (3.1 kW total) with $T_C = 90 ^{\circ}C$						
T _J 125 °C						
Supply voltage	360 V _{DC}					
Power factor	0.8					
Modulation depth (see fig. 1)	115 %					
$V_{CE(on)}$ (typical) at $I_C = 8.7$ A, 25 °C	1.37 V					
Speed	1 kHz to 10 kHz					
Package	SIP					
Circuit configuration	Three phase inverter					

FEATURES





· Switching-loss rating includes all "tail" losses

ROHS

- HEXFRED® soft ultrafast diodes
- Optimized for medium speed 1 kHz to 10 kHz, see fig. 1 for current vs. frequency curve
- · Designed and qualified for industrial level
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

The IGBT technology is the key to Vishay's Semiconductors advanced line of IMS (insulated metal substrate) power modules. These modules are more efficient than comparable bipolar transistor modules, while at the same time having the simpler gate-drive requirements of the familiar power MOSFET. This superior technology has now been coupled to a state of the art materials system that maximizes power throughput with low thermal resistance. This package is highly suited to motor drive applications and where space is at a premium.

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS	MAX.	UNITS	
Collector to emitter voltage	V _{CES}		600	V	
Continuous collector current, each IGBT		T _C = 25 °C	16		
	I _C	T _C = 100 °C	8.7		
Pulsed collector current	I _{CM} ⁽¹⁾		50	Α	
Clamped inductive load current	I _{LM} (2)		50	A	
Diode continuous forward current	I _F	T _C = 100 °C	6.1		
Diode maximum forward current	I _{FM}		50		
Gate to emitter voltage	V_{GE}		± 20	V	
Isolation voltage	V _{ISOL}	Any terminal to case, t = 1 min	2500	V_{RMS}	
Maximum navvar dissination and ICDT	В	T _C = 25 °C	36	W	
Maximum power dissipation, each IGBT	P_{D}	$T_{C} = 100 ^{\circ}C$]	
Operating junction and storage temperature range	T _J , T _{Stg}	-40		°C	
Soldering temperature	_	For 10 s, (0.063" (1.6 mm) from case) 30		C	
Mounting torque		6-32 or M3 screw	5 to 7 (0.55 to 0.8)	lbf · in (N · m)	

Notes

⁽¹⁾ Repetitive rating; V_{GE} = 20 V, pulse width limited by maximum junction temperature (see fig. 20)

 $^{^{(2)}}$ V_{CC} = 80 % (V_{CES}), V_{GE} = 20 V, L = 10 μ H, R_g = 22 Ω (see fig. 19)





THERMAL AND MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TYP.	MAX.	UNITS	
Junction to case, each IGBT, one IGBT in conduction	R _{thJC}	-	3.5		
Junction to case, each DIODE, one DIODE in conduction	R_{thJC}	-	5.5	°C/W	
Case to sink, flat, greased surface	R _{thCS}	0.10	-		
Weight of module		20	-	g	
Weight of module		0.7	-	oz.	

ELECTRICAL SPECIFICATIONS (T _J = 25 °C unless otherwise specified)							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNITS
Collector to emitter breakdown voltage	V _{(BR)CES} (1)	$V_{GE} = 0 \text{ V}, I_{C} = 250 \mu\text{A}$	V _{GE} = 0 V, I _C = 250 μA		-	-	V
Temperature coefficient of breakdown voltage	$\Delta V_{(BR)CES}/\Delta T_J$	$V_{GE} = 0 \text{ V}, I_{C} = 1.0 \text{ mA}$		-	0.69	-	V/°C
Collector to emitter saturation voltage	V _{CE(on)}	I _C = 8.7 A	V _{GE} = 15 V see fig. 2, 5	-	1.37	1.5	V
		I _C = 16 A		-	1.63	-	
		I _C = 8.7 A, T _J = 150 °C	300 fig. 2, 3	-	1.37	-	V
Gate threshold voltage	V _{GE(th)}	V - V I - 250 HA		3.0	-	6.0	
Temperature coefficient of threshold voltage	$\Delta V_{GE(th)}/\Delta T_{J}$	$V_{CE} = V_{GE}$, $I_C = 250 \mu A$		-	- 11	-	mV/°C
Forward transconductance	9 _{fe} ⁽²⁾	V _{CE} = 100 V, I _C = 8.7 A		6.0	8.0	-	S
Zero gate voltage collector current	I _{CES}	$V_{GE} = 0 \text{ V}, V_{CE} = 600 \text{ V}$		-	-	250	μΑ
		$V_{GE} = 0 \text{ V}, V_{CE} = 600 \text{ V},$	T _J = 150 °C	-	-	2500	μΑ
Diode forward voltage drop	V _{FM}	I _C = 12 A	see fig. 13	-	1.3	1.7	V
		I _C = 12 A, T _J = 150 °C		-	1.2	1.6	V
Gate to emitter leakage current	I _{GES}	V _{GE} = ± 20 V		-	-	± 100	nA

Notes

 $^{^{(1)}~}$ Pulse width $\leq 80~\mu s,~duty~factor \leq 0.1~\%$

⁽²⁾ Pulse width 5.0 µs; single shot



PARAMETER	SYMBOL	T	EST CONDIT	IONS	MIN.	TYP.	MAX.	UNITS
Total gate charge (turn-on)	Qg	$I_{\rm C} = 8.7 \; {\rm A}$			-	54	82	
Gate to emitter charge (turn-on)	Q _{ge}		V _{CC} = 400 V		-	8.1	12	nC
Gate to collector charge (turn-on)	Q _{gc}	V _{GE} = 15 V see fig. 8			-	21	32]
Turn-on delay time	t _{d(on)}				-	39	-	
Rise time	t _r	T _{.1} = 25 °C	T ₁ = 25 °C				-	_
Turn-off delay time	t _{d(off)}	$I_{\rm C} = 8.7 \text{A, V}$			-	220	330	ns
Fall time	t _f	V _{GE} = 15 V,		l" and diode	-	160	240	
Turn-on switching loss	Eon		Energy losses include "tail" and diode reverse recovery. see fig. 9, 10, 11, 18				-	
Turn-off switching loss	E _{off}	see fig. 9, 10					-	mJ
Total switching loss	E _{ts}	1					1.3	
Turn-on delay time	t _{d(on)}	T _J = 150 °C,	-	37	-			
Rise time	t _r	$I_{\rm C} = 8.7 \text{A, V}$	$I_C = 8.7 \text{ A}, V_{CC} = 480 \text{ V}$				-	
Turn-off delay time	t _{d(off)}	V_{GE} = 15 V, R_{G} = 22 Ω Energy losses include "tail" and diode reverse recovery			-	400	-	ns
Fall time	t _f				-	290	-	
Total switching loss	E _{ts}	see fig. 9, 10	see fig. 9, 10, 11, 18			1.57	-	mJ
Input capacitance	C _{ies}	V _{GE} = 0 V	V _{GE} = 0 V V _{CC} = 30 V f = 1.0 MHz		-	1100	-	
Output capacitance	Coes				-	74	-	pF
Reverse transfer capacitance	C _{res}	see fig. 7	-		-	14	-	
Diada assaultina		T _J = 25 °C	E- 11		-	42	60	
Diode reverse recovery time	t _{rr}	T _J = 125 °C	see fig. 14	see fig. 14	-	80	120	ns
Diada pagla valvava vaga vaga abava		T _J = 25 °C	$T_{J} = 25 \degree C$ $T_{J} = 125 \degree C$ see fig. 15		-	3.5	6.0	Α
Diode peak reverse recovery charge	I _{rr}	T _J = 125 °C		See fig. 15 $I_F = 12 \text{ A}$ $V_B = 200 \text{ V}$	-	5.6	10	
Diada rayaraa ragayany aharaa	0	T _J = 25 °C		dl/dt = 200 A/μs	-	80	180	nC
Diode reverse recovery charge	Q_{rr}	T _J = 125 °C		See lig. 10		220	600	IIC
Diode peak rate of fall of recovery	dl _{(rec)M} /dt	T _J = 25 °C	see fig. 17		-	180	-	A/µs
during t _b	ai(rec)M/at	T _J = 125 °C see fig. 1	366 lig. 17	56 lig. 17	-	116	-	Ανμο

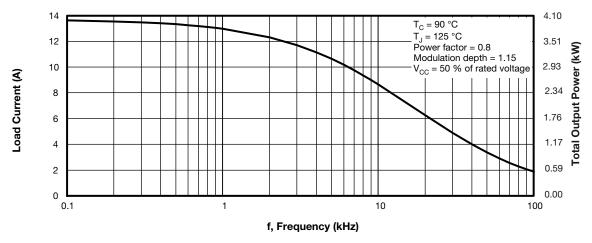
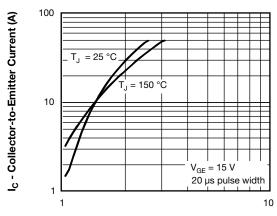


Fig. 1 - Typical Load Current vs. Frequency (Load Current = I_{RMS} of Fundamental)



V_{CF} - Collector-to-Emitter Voltage (V)

Fig. 2 - Typical Output Characteristics

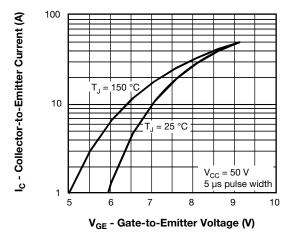


Fig. 3 - Typical Transfer Characteristics

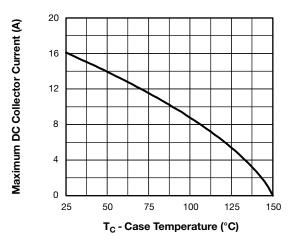


Fig. 4 - Maximum Collector Current vs. Case Temperature

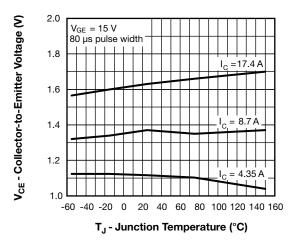


Fig. 5 - Typical Collector to Emitter Voltage vs. Junction Temperature

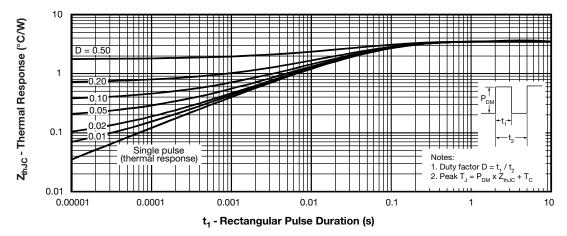


Fig. 6 - Maximum Effective Transient Thermal Impedance, Junction to Case

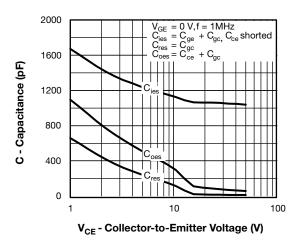


Fig. 7 - Typical Capacitance vs. Collector to Emitter Voltage

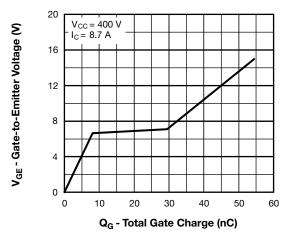


Fig. 8 - Typical Gate Charge vs. Gate to Emitter Voltage

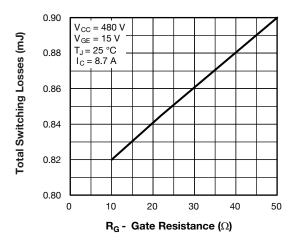


Fig. 9 - Typical Switching Losses vs. Gate Resistance

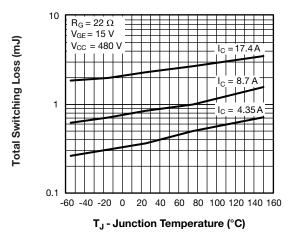


Fig. 10 - Typical Switching Losses vs. Junction Temperature

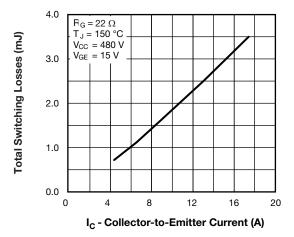


Fig. 11 - Typical Switching Losses vs. Collector to Emitter Current

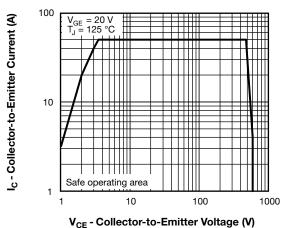


Fig. 12 - Turn-Off SOA

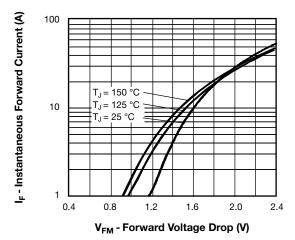


Fig. 13 - Maximum Forward Voltage Drop vs. Instantaneous Forward Current

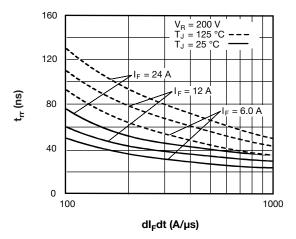


Fig. 14 - Typical Reverse Recovery Time vs. dl_F/dt

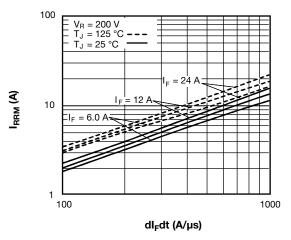


Fig. 15 - Typical Recovery Current vs. dl_E/dt

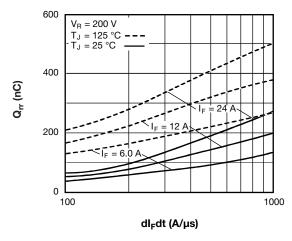


Fig. 16 - Typical Stored Charge vs. dI_F/dt

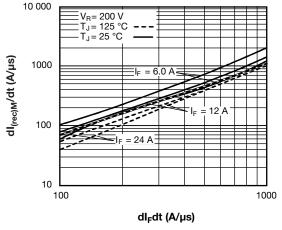


Fig. 17 - Typical $dI_{(rec)M}/dt$ vs dI_F/dt



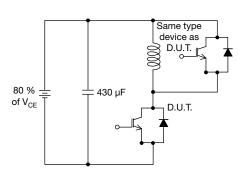


Fig.18a - Test Circuit for Measurements of I_{LM} , E_{on} , $E_{off(diode)}$, t_{rr} , Q_{rr} , I_{rr} , $t_{d(on)}$, t_r , $t_{d(off)}$, t_f

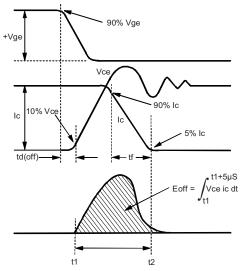


Fig.18c - Test Waveforms for Circuit of Fig. 18a, Defining $E_{\text{off}},\,t_{\text{d(off)}},\,t_{\text{f}}$

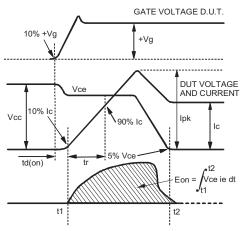


Fig.18b - Test Waveforms for Circuit of Fig. 18a, Defining $E_{on},\,t_{d(on)},\,t_{r}$

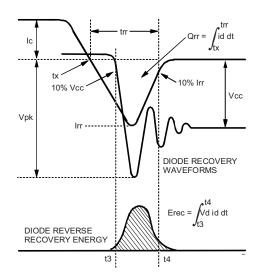


Fig. 18d - Test Waveforms for Circuit of Fig. 18a, Defining E_{rec} , t_{rr} , Q_{rr} , I_{rr}

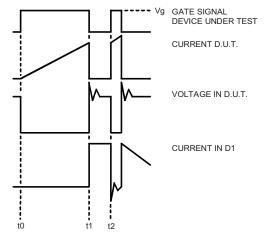


Fig.18e - Macro Waveforms for Figure 18a's Test Circuit



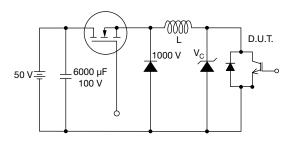


Fig.19 - Clamped Inductive Load Test Circuit

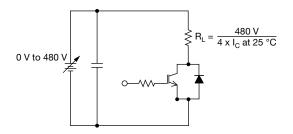
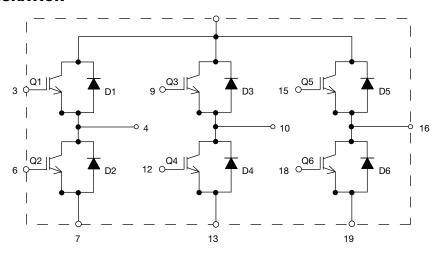


Fig. 20 - Pulsed Collector Current Test Circuit

CIRCUIT CONFIGURATION

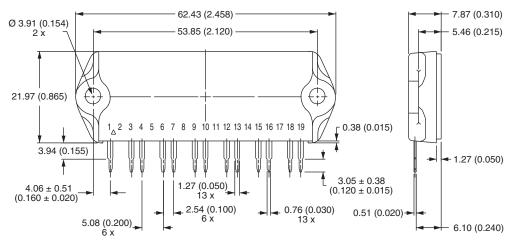


LINKS TO RELATED DOCUMENTS				
Dimensions	www.vishay.com/doc?95066			



IMS-2 (SIP)

DIMENSIONS in millimeters (inches)



IMS-2 Package Outline (13 Pins)

Notes

- $^{(1)}$ Tolerance uless otherwise specified \pm 0.254 mm (0.010")
- (2) Controlling dimension: inch
- (3) Terminal numbers are shown for reference only

Document Number: 95066 Revision: 30-Jul-07



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