VIS2007

5V/8A High-Efficiency Synchronous Boost Converter

Description

The VIS2007 is a high efficiency, current mode, fully integrated boost converter, which can start up from an input voltage as low as 1.8V and convert up to 5.5V output voltage. During shutdown, it can disconnect the output from the input.

The converter integrates 10mΩ/30mΩ power MOSFETs and can deliver up to 3A output current at 5V output with 2.5V input supply. When the output is shorted, the VIS2007 enters hiccup protection mode and recovers automatically when the output short is removed.

The VIS2007 also includes input under voltage lockout, output over voltage protection, cycle-by-cycle over current protection, short circuit protection and thermal shutdown to prevent damage in the event of output overload. The VIS2007 is available in a low profile 10-pin 2mmx2mm FCQFN package.

Applications

- Tablets
- USB Power Supply
- Battery Powered Products
- Power Banks, Battery Backup Units

Features

- 1.8V Minimum Input Voltage
- Output Voltage Range: 2.5V to 5.5V
- 8A Peak Switching Current Limit
- 10mΩ(LS) / 30mΩ(HS) Power MOSFETs
- High Efficiency (96.2% at V_{IN} = 3.7V, V_{OUT} = 5V, I_{OUT} = 3A)
- True Load Disconnection from Input
- ±1% Accurate Reference Voltage
- Internal Compensation and Soft Start
- Low Shutdown Current < 1μA
- Over-Current and Short-Circuit Protection
- Output Overvoltage Protection
- Thermal Shutdown
- 2x2mm FCQFN 10-Pin Package
- This is a Pb−Free Device

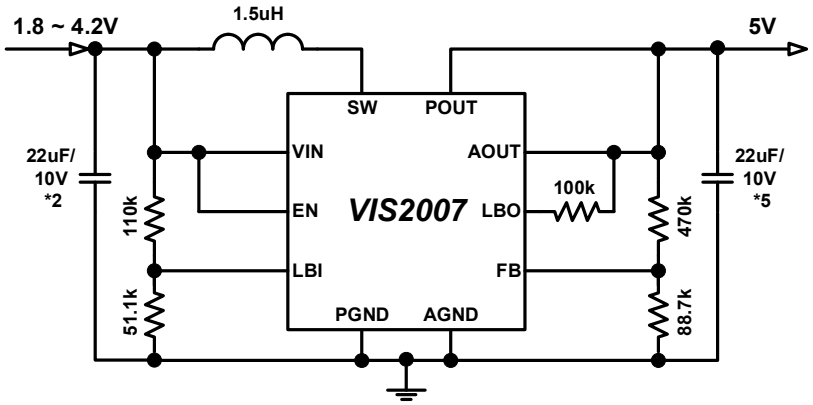
Ordering Information

Device	Package	Top Marking*	Shipping†
VIS2007	FCQFN-10 (2x2mm)	2007 YWLL	3000 Tape & Reel

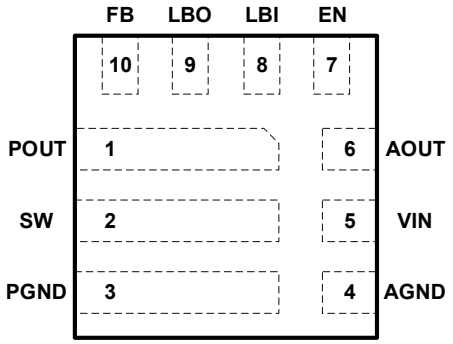
* Top Marking Code: Y is Year, W is Week, LL is Lot.

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications.

Typical Application Circuit



Pinout (Top View)



FCQFN-10 (2x2mm)

Pin Functions

Pin	Name	Description
1	POUT	Power Output. POUT must be locally bypassed.
2	SW	Switch Node. SW is connected to the internal high-side MOSFET and low-side MOSFET.
3	PGND	Power Ground.
4	AGND	Analog Ground.
5	VIN	Input Supply. VIN must be locally bypassed.
6	AOUT	Analog Output. AOUT must be locally bypassed.
7	EN	Enable pin of the chip. This pin is internally integrated with a 1MΩ pull-down resistor.
8	LBI	Low Battery Comparator Input (comparator enabled with EN).
9	LBO	Low Battery Comparator Output (open drain).
10	FB	Feedback Input. Connecting a resistor divider from V_{OUT} to this pin to adjust V_{OUT} voltage.

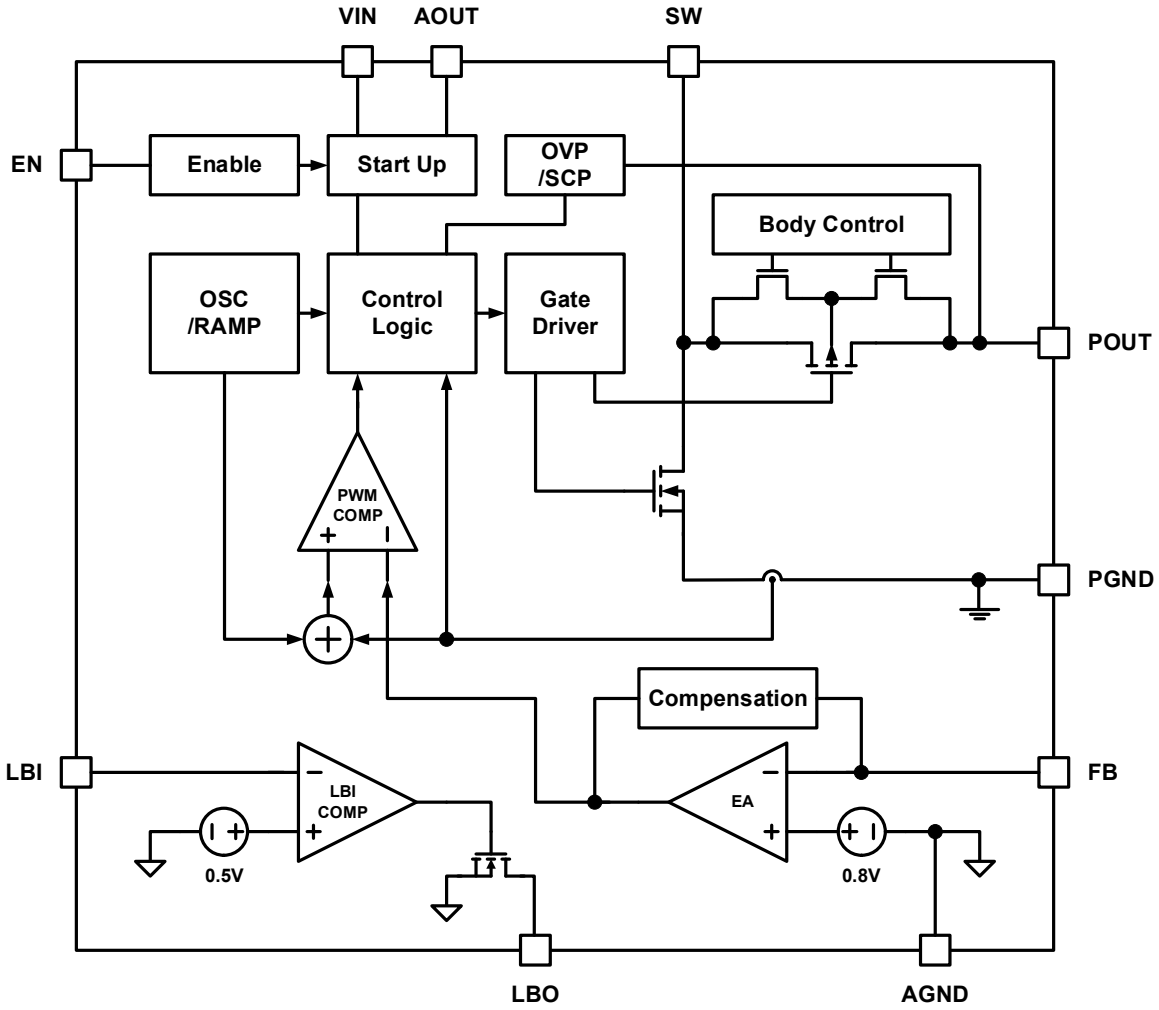


Figure 1. Functional Block Diagram

Absolute Maximum Ratings (1)

All Pins	-0.3V to +6V
Junction Temperature	150°C
Lead Temperature	260°C
Storage Temperature	-65°C to 150°C
Continuous Power Dissipation (T_A= 25°C) (2)	2.5W

Recommended Operating Conditions (3)

Supply Voltage V_{IN}	1.8V to 5.25V
Output Voltage V_{OUT}	2.5V to 5.5V
Operating Junction Temperature	-40°C to +125°C

Thermal Resistance (4)

Junction to Case Θ_{JC}	10°C/W
Junction to Ambient Θ_{JA}	50°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) The thermal resistance values are dependent of the internal losses split between devices and the PCB heat dissipation. These data are based on a typical operation condition with a 4−layer FR−4 PCB board, which has two, 1−ounce copper internal power and ground planes and 2−ounce copper traces on top and bottom layers with approximately 80% copper coverage. No airflow and no heat sink applied (reference JEDEC 51.7). It also does not account for other heat sources that may be present on the PCB next to the device.

Electrical Characteristics

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, typical values are tested at T_A = 25°C, unless otherwise noted.

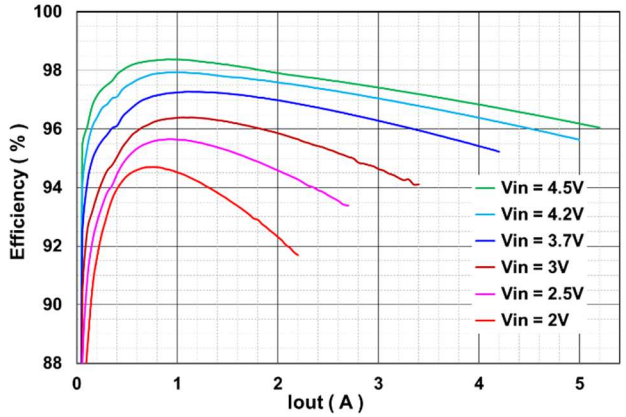
Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating Input Voltage	V_{IN}		1.8		5.25	V
Undervoltage Rising	V_{INUVLO_R}	V_{IN} rising			1.75	V
Undervoltage Falling	V_{INUVLO_F}	V_{IN} falling		650		mV
Supply Current (Shutdown)	I_{INS}	V_{EN} = 0V, measured at V_{IN}		0.1	1	μA
Supply Current (Quiescent)	I_{INQ}	IC enabled, no load, no switching, measured at V_{IN}		1.8		μA
	I_{OUTQ}	IC enabled, no load, no switching, measured at V_{OUT}		190		μA
Switching Frequency	F_S			600		kHz
Maximum Duty Cycle	D_{MAX}		90	95		%
EN High Threshold	V_{ENH}	V_{EN} rising	1.2			V
EN Low Threshold	V_{ENL}	V_{EN} falling			0.4	V
EN Pull-down Resistor	R_{EN}	V_{EN} = 3.3V		1000		kΩ
Feedback Voltage	V_{FB}		792	800	808	mV
High-side MOSFET On-resistance	R_{ONH}			30		mΩ
Low-side MOSFET On-resistance	R_{ONL}			10		mΩ
Linear Charge Current Limit (5)	I_{LIM_LN}	V_{OUT} = 0V		0.6		A
		V_{OUT} = 1V		1.6		
SW Current Limit (5)	I_{LIM_SW}		8			A
Output Overvoltage Protection Threshold	V_{OVP}			5.7		V
LBI Threshold	V_{LBI}	V_{LBI} falling	490	500	510	mV
LBI Hysteresis	V_{LBIhys}			8		mV
LBI Leakage Current	I_{LBI}	V_{EN}= V_{IN}			20	nA
LBO Low Voltage	V_{LBO}	V_{OUT} = 3.3V, I_{LBO} = 100 μA			0.4	V
LBO Leakage Current	I_{LBO}	V_{LBO} = 5.5V			0.1	μA
Thermal Shutdown (5)	T_{SD}			150		°C
Thermal Shutdown Hysteresis (5)	T_{SDhys}			25		°C

Notes:
5) Guaranteed by characterization, not production tested.

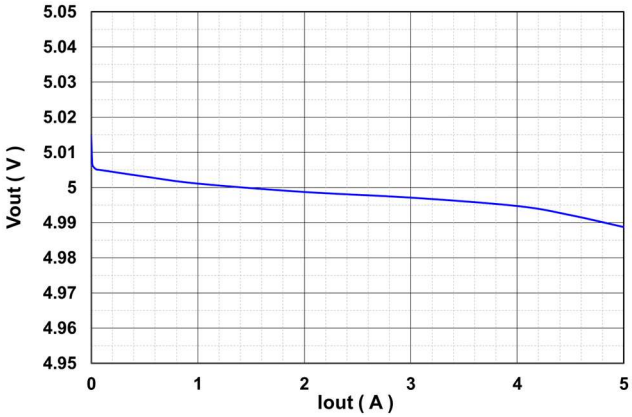
Typical Performance Characteristics

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 0A, T_A = 25°C, L = 1.5uH, C = 22uF * 5, unless otherwise noted.

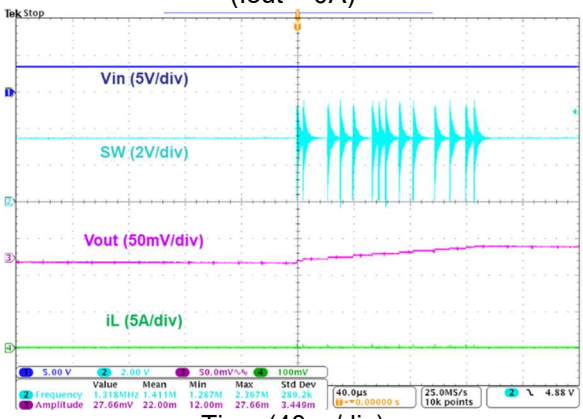
Efficiency



Output Voltage Regulation

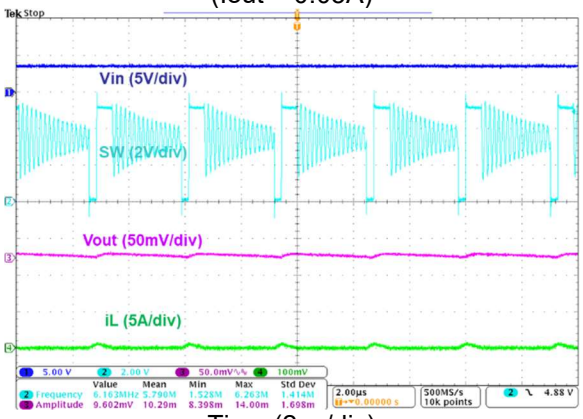


Steady State
(Iout = 0A)



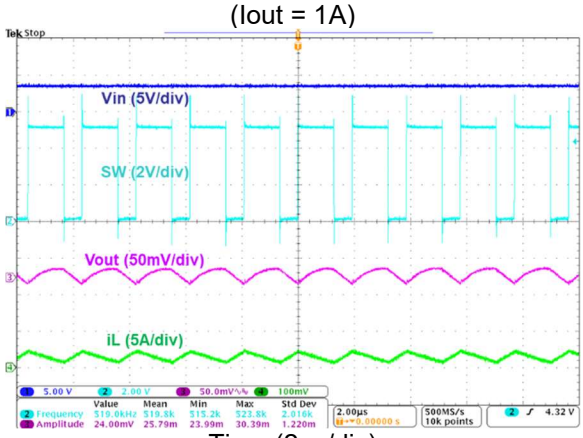
Time (40us/div)

Steady State
(Iout = 0.05A)



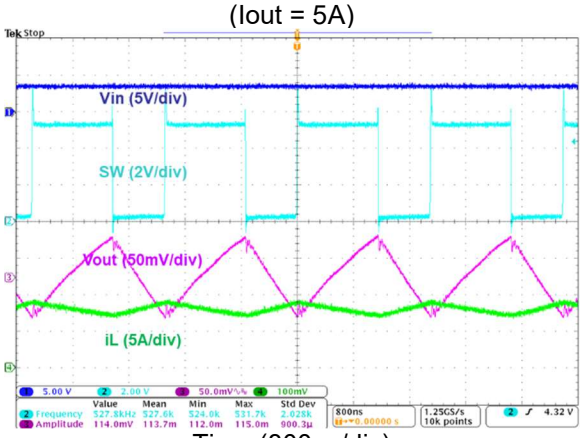
Time (2us/div)

Steady State
(Iout = 1A)



Time (2us/div)

Steady State
(Iout = 5A)

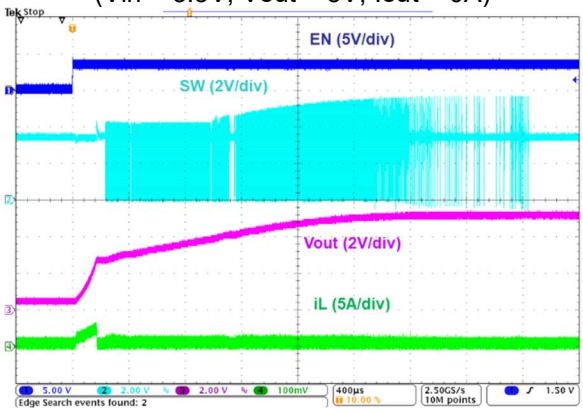


Time (800ns/div)

Typical Performance Characteristics (Continued)

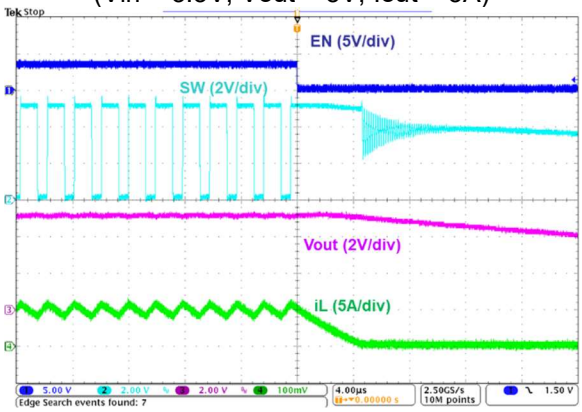
V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, I_{OUT} = 0A, T_A = 25°C, L = 1.5uH, C = 22uF * 5, unless otherwise noted.

Power Up
(Vin = 3.3V, Vout = 5V, Iout = 0A)



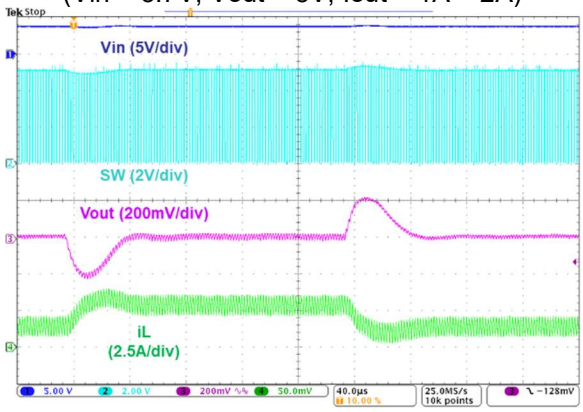
Time (400us/div)

Power Down
(Vin = 3.3V, Vout = 5V, Iout = 3A)



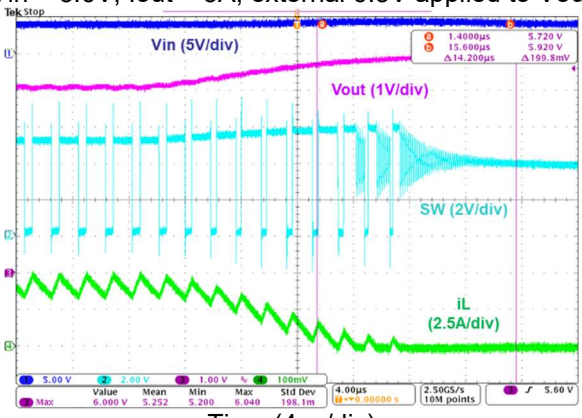
Time (4us/div)

Load Transient
(Vin = 3.7V, Vout = 5V, Iout = 1A ~ 2A)



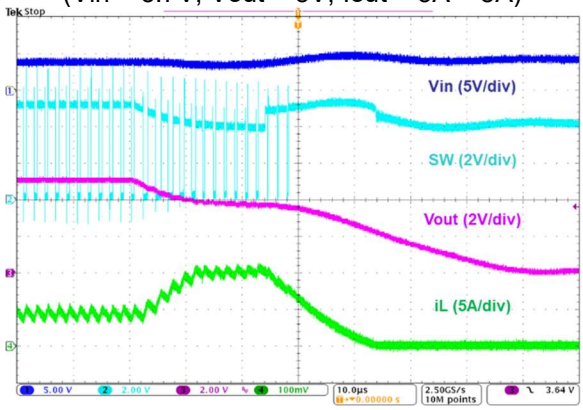
Time (40us/div)

Over Voltage Protection
(Vin = 3.6V, Iout = 3A, external 6.3V applied to Vout)



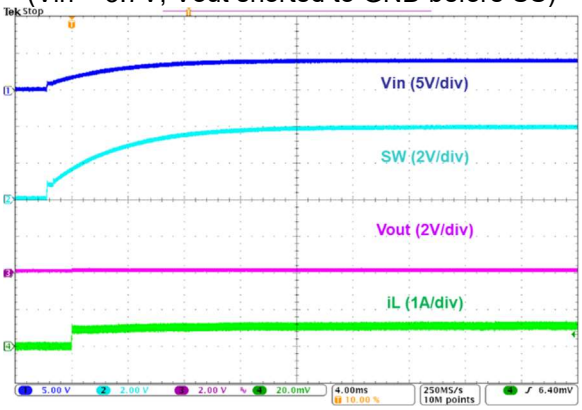
Time (4us/div)

Over Current Protection
(Vin = 3.7V, Vout = 5V, Iout = 3A ~ 8A)



Time (10us/div)

Short Circuit Protection
(Vin = 3.7V, Vout shorted to GND before SS)



Time (4ms/div)

Operation Information

The VIS2007 is a high efficiency synchronous boost converter. The device features fixed-frequency (600kHz) current-mode PWM control for excellent load and line regulation. Integrated low on-resistance power MOSFETs, combining with frequency stretching and power save mode (PSM) at light load, improve the efficiency over a wide load range. Internal soft-start and loop compensation simplifies the design process and minimizes the number of external components.

Enable and Disable

The device is enabled by setting EN pin high (>1.2V). When EN pin is pulled to ground, the device is disabled, switching is stopped and entire internal circuitry is turned off. The output is isolated from the input.

Linear Charge Mode

After the device is enabled, the internal reference and bias circuits are activated when the rising V_{IN} trips the under-voltage lockout threshold (V_{INUVLO_R}). At first, the PMOS rectifier turns on to charge the output capacitor linearly in linear charge mode. The device exits linear charge mode when the output is charged to 1.7V. In linear charge mode, the PMOS charging current is being regulated to avoid inrush current and limit the output current during short-circuit protection (SCP). This charging current is proportional to the output voltage, which is 0.6A when the output is 0V and ramps up as the output voltage increases. Once the output reaches 1.7V, the device starts switching and the output slowly ramps up to the targeted value in soft start.

Soft Start

In linear charge mode, the soft-start voltage follows the voltage on FB pin. As the device starts switching, the soft-start voltage is rising slowly by charging an internal capacitor with a current source. The reference voltage rises at the same rate of soft-start voltage. The soft-start ends when the soft-start voltage reaches 0.8V. The typical soft-start time is 2ms. Soft-start mechanism prevents high inrush current from the input power supply to the output capacitors.

PWM and PSM

The VIS2007 automatically enters power save mode (PSM) when the load decreases and resumes pulse width modulation (PWM) mode when the load increases. In the PWM mode, at the beginning of each cycle, the internal N-channel MOSFET switch is turned on, forcing the inductor current to rise. The current of this switch is measured and converted to a voltage by a current sense amplifier. That voltage is compared to the output voltage of the error amplifier. When the two voltages are equal, the PWM comparator turns off the N-channel MOSFET and forces the inductor current to flow into the output capacitor through the internal P-channel MOSFET, and the inductor current decreases. The peak inductor current is controlled by V_{COMP}, which in turn is controlled by the output voltage, thus the output voltage is regulated through the inductor current to satisfy the load. In the PSM, the device lowers the switching frequency and then switches to pulse skip mode if the load drops further.

Step-down Mode

In case that V_{OUT} is lower than V_{IN}+0.3V which usually happens during soft start and large load or line transients, the VIS2007 operates in a step-down mode with a lower peak current limit than that in step-up (boost) mode. In this step-down mode, the PWM operation is similar to that in the boost mode except that the gate of internal P-channel MOSFET is tied to VIN. One thing needs to pay more attention is that SW node voltage stress in step-down mode is about 1V higher than boost mode and more power dissipation from the device.

Current Limit

To avoid an accidental large peak current, an internal cycle-by-cycle current limit operation is adopted. The internally sensed inductor current is converted to a voltage and compared to the peak current limit. The internal N-channel

MOSFET switch is turned off immediately as soon as the inductor current exceeds the limit. If the load current is further increased and the output is pulled below the input voltage, the VIS2007 enters short circuit protection (SCP) mode.

Short Circuit Protection

Once short circuit protection (SCP) is triggered, the VIS2007 stops switching immediately and restarts after about 1ms as a new power-on cycle. The device continues this hiccup steady state until the overload condition is removed.

Output Disconnection

When the device is shut down, the VIS2007 disconnects V_{OUT} from V_{IN} by eliminating body diode conduction of the internal P-channel MOSFET switch. This prevents either V_{OUT} or VIN being discharged by each other when the VIS2007 is disabled.

Output Over-Voltage Protection

The VIS2007 provides output over-voltage protection. If the output voltage exceeds the over voltage protection (OVP) threshold of 5.7V, the device stops switching and both of the N-channel and P-channel MOSFET switches turn off. When the output voltage drops below the OVP voltage, the device resumes switching automatically. This function secures the circuits connected to the output from excessive overvoltage.

Low Battery Detector

The VIS2007 integrates a low-battery detector to monitor the input battery voltage and generate an error flag when that voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance because the voltage at LBI is above the threshold. It becomes actively low when the voltage at LBI goes below 500 mV.
The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold.

Thermal Shutdown

The VIS2007 has a built-in temperature monitor. If the chip temperature exceeds thermal shutdown threshold, the device goes into the thermal shutdown and switching is stopped. If the temperature drops below the thermal shutdown falling threshold, the converter resumes the normal operation.

Application Information

Following information provides a general component design reference in a typical application of the VIS2007.

Output Voltage Setting

Output voltage V_{OUT} is programmed by a resistor divider connected between V_{OUT} sense point and analog ground AGND, as depicted in Figure 2, having a value of

$$V_{OUT} = V_{FB} \cdot \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where V_{FB} is feedback voltage, which equals to an internal reference voltage 0.8V when the V_{OUT} is in regulation.

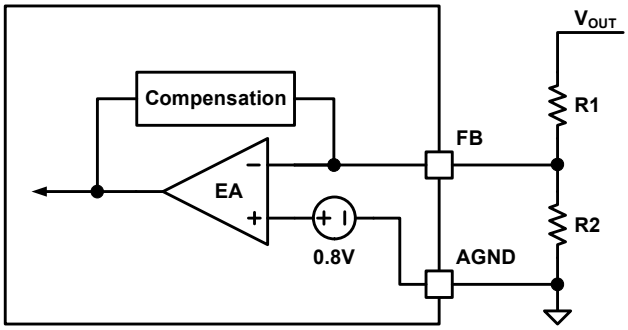


Figure 2. Output Voltage Setting

Usually the resistor R1 is predetermined in applications, having a typical value of 470kΩ. When there is a need, users may fine tune close-loop response by adjusting R1 value in a range from 100 kΩ to 1M Ω. The smaller R1 resistance, the higher close-loop bandwidth while probably lower stability margin. After R1 is selected, R2 value is given by

$$R2 = \frac{R1}{\frac{V_{OUT}}{V_{FB}} - 1} \quad (2)$$

Inductor Selection

A low-DCR SMD inductor is recommended for a high-efficiency and compact design. A general rule of thumb is to allow the peak-to-peak ripple current to be approximately 30-50% of the maximum input current, and the maximum peak inductor current in normal operation should not be over 75% of the current limit to maintain good output regulation.

In most applications, a 1.5uH inductor could be a good choice though users may select an alternative inductor in a range from 1uH to 4.7uH. For a given inductor L, the peak-to-peak ripple current in Continuous Conduction Mode (CCM) is

$$I_{pp} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{V_{OUT} \cdot F_S \cdot L} \quad (3)$$

where F_S is switching frequency in CCM.

To avoid overheating the inductor, the maximum DC current I_{IN_MAX} under the worst condition needs to be calculated by

$$I_{IN\_MAX} = \frac{V_{OUT} \cdot I_{OUT\_MAX}}{V_{IN\_MIN} \cdot \eta} \quad (4)$$

where V_{IN_MIN} is the minimum input voltage, I_{OUT_MAX} is the maximum load current, and η is the conversion efficiency.

To make sure the inductor does not saturate in a large load step transient, an additional rated saturation current margin should be added on top of the peak current in normal operation, that is

$$I_{L\_rated} = K_m \cdot \left(I_{IN\_MAX} + \frac{I_{pp}}{2}\right) \quad (5)$$

In equation (5), the coefficient K_m could be about 1.5.

Due to the cycle-by-cycle peak current protection of the VIS2007, with a built-in switching peak current limit of I_{LIM_SW}, the input DC current limit I_{IN_LIM} is also a function of the inductor peak-to-peak ripple current I_{pp}, we have

$$I_{IN\_LIM} = I_{LIM\_SW} - \frac{I_{pp}}{2} \quad (6)$$

And hence, an approximated corresponding output DC current limit I_{OUT_LIM} can be obtained as

$$I_{OUT\_LIM} = \frac{V_{IN} \cdot I_{IN\_LIM} \cdot \eta}{V_{OUT}} \quad (7)$$

Input Capacitor Selection

A 22uF or more ceramic capacitors are recommended to stabilize the input voltage, absorb hot plug voltage spike, and bypass the inductor ripple current with a low power loss.

Output Capacitor Selection

Low-ESR capacitors, such as X5R or better ceramic capacitors, are preferred to keep the output voltage ripple to a minimum and reduce voltage transient spikes. The output voltage ripple can be estimated as

$$V_{pp} \approx \frac{I_{OUT}}{\eta}\left(\frac{1-\frac{V_{IN}}{V_{OUT}}}{F_S \cdot C_{OUT}} + \frac{ESR \cdot V_{OUT}}{V_{IN}}\right) \quad (8)$$

where C_{OUT} is a total output capacitance value and ESR is an equivalent series resistance value, taking account of all the output capacitors in parallel.

Low Battery Detection

Low battery detection and indication can be done by applying a resistor divider from the input voltage V_{IN} to LBI pin and pull LBO pin up to V_{OUT} via a 100kΩ resistor, as shown in Figure 3. The programmed low battery voltage threshold is

$$V_{LB} = 0.5V \cdot \left(1 + \frac{R3}{R4}\right) \quad (9)$$

Note that LBI should not be left float. If the function is unnecessary in an application, users can simply connect LBI pin to V_{IN} or ground and leave LBO pin float.

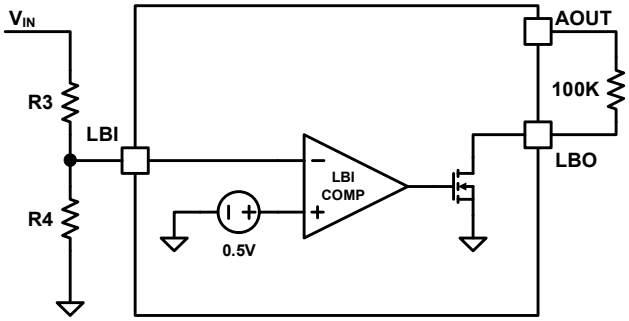


Figure 3. Low Battery Detection

PCB Layout Guideline

Following information provides a general board layout guideline in a typical application, taking the VIS2007 demo board as a reference.

Electrical Layout Considerations

Good electrical layout is a key to ensure proper operation, high efficiency, and noise reduction.

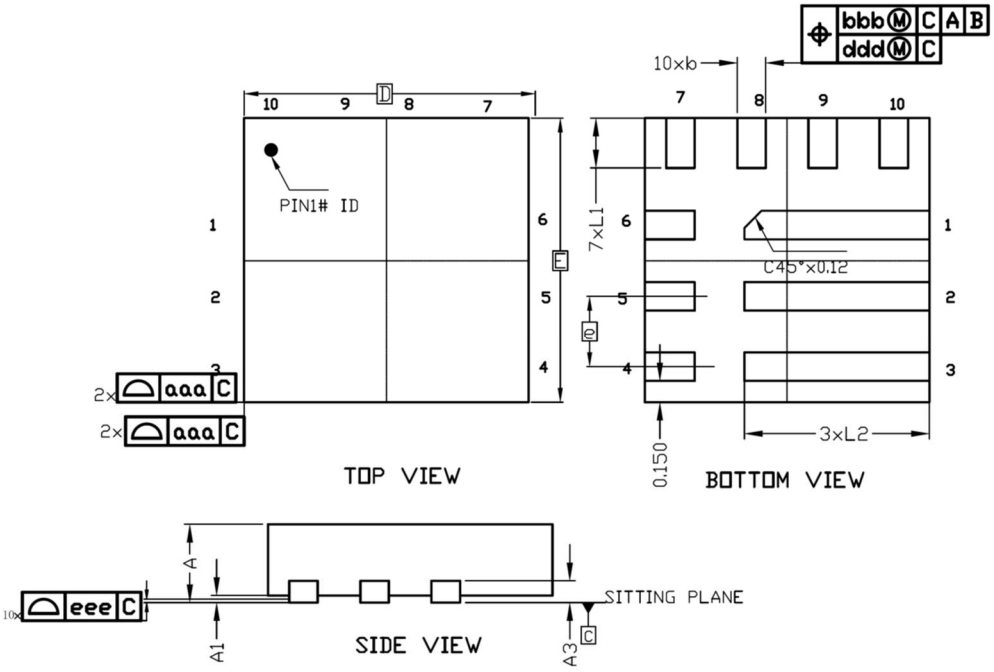
- **Power Paths:** Use wide and short traces or copper pours for power paths (such as V_{IN}, V_{OUT}, SW, and PGND) to reduce parasitic inductance and high-frequency loop area. It is appreciated for efficiency improvement as well.
- **Power Supply Decoupling:** The converter should be well decoupled by input capacitors. A 22uF or more MLCC capacitors are directly placed at VIN pin.
- **POUT Decoupling:** At least one or more low-ESL MLCC output capacitors must be placed very close to POUT pin, and the decoupling loop area should be as small as possible to reduce parasitic inductance, switching voltage spike, and noise emission.
- **AOUT Decoupling:** Place a 4.7uF or larger decoupling capacitor as close as possible to AOUT pin.
- **Switching Node:** SW node should be a copper pour, but compact because it is also a noise source.
- **Ground:** It would be good to have multiple layers of ground planes on PCB. Directly connect PGND pin and AGND pin to GND planes through vias close to the pins.
- **Voltage Sense:** Use a short trace and arrange a “quiet” path for the output voltage sense. Keep FB trace short to minimize its capacitance to ground. All feedback components must be kept close to FB pin to prevent noise injection on FB traces.

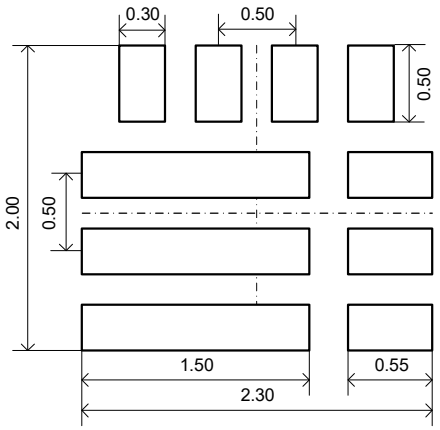
Thermal Layout Considerations

Good thermal layout helps high power dissipation from a small package with reduced temperature rise.

- All the pins of the device must be well soldered on the board.
- A four or more layers PCB board with solid ground planes is preferred for efficient heat dissipation.
- More vias are welcome to be around the device to connect more layers to reduce thermal impedance.
- Use large-area copper pours to help thermal conduction and radiation.
- Distribute heat sources to be not too close together.

Package Dimensions





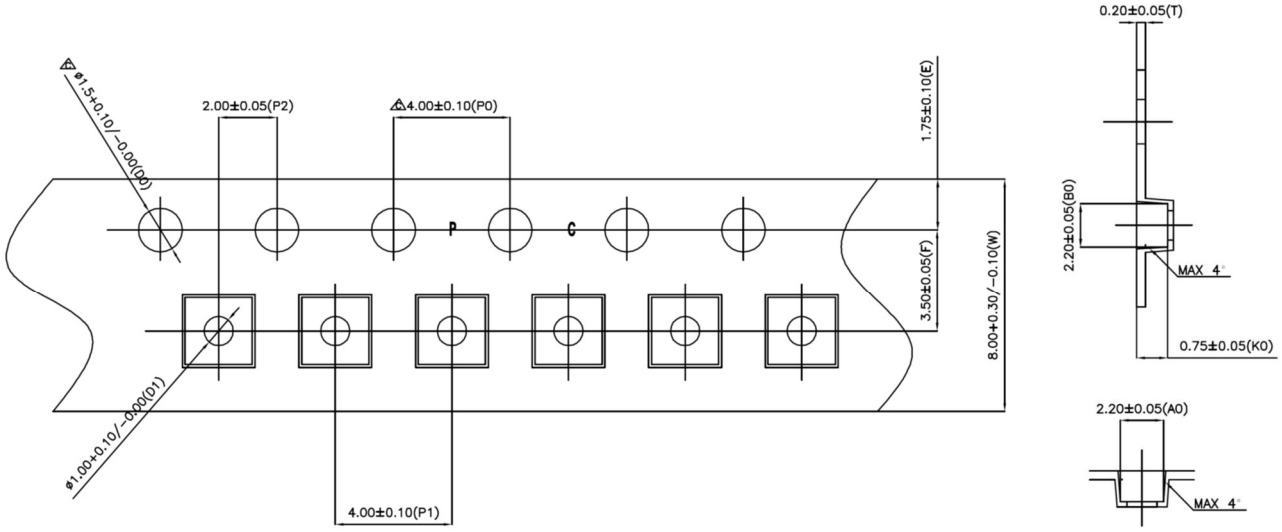
LAND PATTERN RECOMMENDATION

DIM / SYMBOL	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
A1	0	0.02	0.05
A3	–	0.152 REF	–
b	0.15	0.20	0.25
D		2.00BSC	
E		2.00BSC	
e		0.50BSC	
L1	0.30	0.35	0.40
L2	1.25	1.30	1.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

Notes:

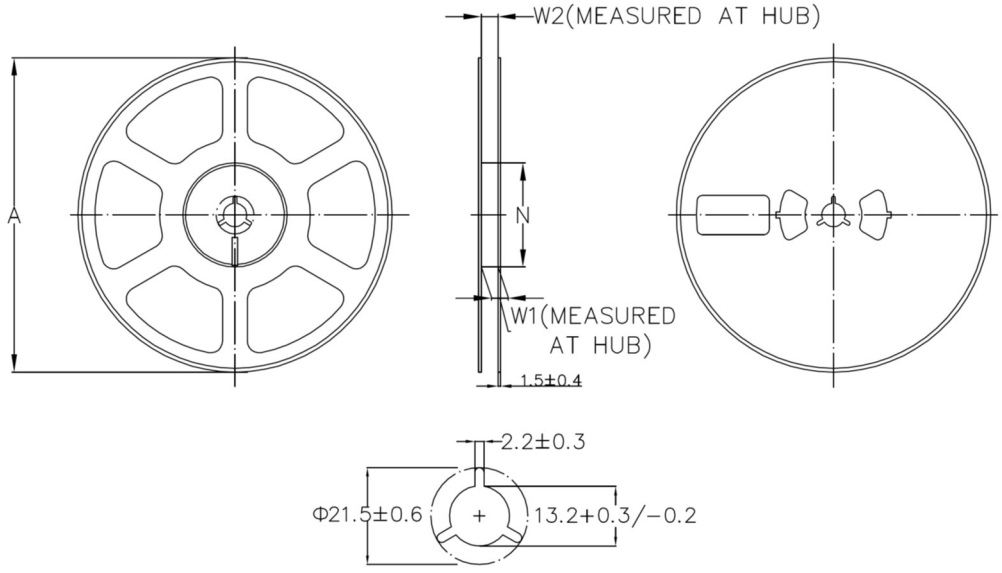
- Dimensioning and tolerancing confirm to ASME Y14.5M-1994.
- All dimensions are in millimeters, angles are in degrees.
- Unilateral coplanarity zone applies to the exposed heat sink slug as well as the terminals.
- Dimension b applies to metallized terminal and is measured between 0.15mm to 0.30mm from the terminal tip.
- Dimension b should not be measured in radius area.
- All specs take JEDEC MO-220 for reference.

Tape and Reel Information



Notes:

- 10 sprocket hole pitch cumulative tolerance ±0.2.
- Camber not to exceed 1mm in 250mm.
- Material: Polycarbonate.
- Ao and Bo measured on a plane 0.3mm above the bottom of the pocket.
- Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
- Pocket center and pocket hole center must be same position.
- Surface resistivity:10E+5~10E+9 OHMS/SQ.



Tape Width	A (±1.0)	N (±2.0)	W1 (+1.5/-0)	W2 (MAX)
8mm	178.0mm	54.0mm	8.4mm	14.4mm

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