Table of Contents

Features

- Performance
  - 50MHz ARM®Cortex®-M0 processor
- On-Chip Memory
  - 32KB Data
  - 128KB Program
  - 1Kb Efuse memory
  - On-chip Error Detection and Correction (EDAC) and Scrub Engine
- 56 General Purpose I/O (GPIO) pins
  - Configurable direction
  - Configurable weak pull-up/down resistors
  - Configurable as edge or level sensitive interrupt sources
- 24 General purpose counter/timers
  - Configurable interrupt sources
  - Can be triggered from 2 sources (GPIO or other counter/timers)
- 2 UARTS
  - Internal FIFO
  - Transmit or receive interrupt source
- 2 ½ Serial Peripheral Interface (SPI) ports
  - Internal FIFO
  - Transmit or receive interrupt source
  - Multiple chip select outputs
  - Two ports Master / Slave, one port Master only
- 2 I^2C ports
  - Internal FIFO
  - Master and Slave mode on both ports
  - Standard and Fast mode support
- System-level Triple Modular Redundancy (TMR) on all internal registers
- 3.3V I/O Supply; 1.5V Core Supply

Description

The VA10820 ARM®Cortex®-M0 microcontroller chips using ***HARDSIL®*** technology are designed for high reliability in extreme radiation environments. The VA10820 includes Error Detection And Correction (EDAC) logic on the internal memories. This EDAC is byte based for optimum performance and reliability. In addition, the VA10820 includes Triple Modular Redundancy (TMR) with voting on all internal flip-flop storage elements.

1 Functional Description

The VA10820 is optimized for radiation environments. It includes Error Detection And Correction (EDAC) logic on the internal memories. This EDAC is byte-based for optimum performance and reliability. In addition the VA10820 includes Triple Modular Redundancy (TMR) with voting on all internal flip-flop storage elements.

1.1 Related Documentation

The followed related documents will be helpful to fully understand this device:

- ARM® Documents (Available from http://infocenter.arm.com)
  - Cortex®-M0 Generic User Guide
  - Cortex®-M0 Technical Reference Manual
  - AMBA® 3 AHB-Lite Protocol Specification
  - AMBA® 3 APB Protocol Specification
- NXP Documents (Available from http://www.nxp.com)
  - I^2C-bus specification and user manual
- VORAGO Documents
  - VA10800/VA10820 Programmers Guide (Available at http://voragotech.com)

1.2 Feature Summary

- Processor Core
  - ARM®Cortex®-M0 processor
    - Up to 50 MHz
    - SysTick Counter
    - Single Cycle Multiply
  - ARM® Cortex®-M0 built-in Nested Vectored Interrupt Controller (NVIC)
    - 32 Interrupts
  - CoreSight™ compliant debug access via JTAG based Debug interface
    - 4 Breakpoint Comparators

        - 2 Data Watch Point Comparators
        - JTAG Debug Port
- Memory
    - 32kB Data Memory
    - 128kB Code Memory
        - Loaded from external Serial Peripheral Interface (SPI) based memory at startup
        - Configurable boot delay, boot speed, and boot checking
    - Byte-level Error Detection and Correction (EDAC) module
    - Scrub Engine
    - 128kB Code Memory
        - Loaded from external Serial Peripheral Interface (SPI) based memory at startup
        - Configurable boot delay, boot speed, and boot checking
- Peripherals
    - 2 UARTs
        - 16 word Transmit and Receive FIFOs
        - Fractional baud rate generation
            - Supports baud rates up to 115200 with system clocks above 2MHz
        - Supports 5, 6, 7, 8 and 9 bits
        - Supports Even, Odd, and None parity
        - Stop Bits 1 or 2
        - Supports Break generation and detection
        - Error detection
            - FIFO overflow
            - Framing error
            - Parity error
            - Break detection
        - Configurable Interrupt generation
            - FIFO level (fully configurable)
            - Receive Timeout
            - Error
    - 2 ½ SPI Ports
        - Supports all 4 modes of Motorola's SPI Specification

- Word/Frame size of 4 to 16 bits
- 16 word Transmit and Receive FIFOs
- Block mode support for larger Frame sizes
- Master mode rates up to 1/4 the system clock
- Slave mode rates up to 1/12 the system clock
- Configurable Interrupt generation
  - FIFO level (fully configurable)
  - FIFO Overflow
  - Receive Timeout
- 2 Ports Configurable as Master or Slave
- 1 Port is Master Only
  - Uses the SPI Boot ROM pins after startup

- I^2C
  - Standard I^2C-compliant bus interface
  - Dedicated open-drain pins supporting I^2C Fast mode
  - Configurable as Master or Slave
  - 16 word Transmit and Receive FIFOs
  - Configurable Interrupt generation
    - FIFO level (fully configurable)
  - Fast-Mode non-obstruct feature is not supported
- GPIO
  - 2 GPIO Ports, Up to 56 pins total
    - 32 bit A port
    - 24 bit B port
  - Configurable direction control of individual bits
  - Bit level mask register allows single instruction setting or clearing of any bits in one port.
  - Configurable interrupt detect on individual bits
    - Level or Edge sensitive
  - Configurable Pulse mode on individual bits
  - Configurable (0-3) cycle delay on individual bits
- IO Configuration
  - Manages GPIO/SPI/UART IO configurations:
    - Glitch filters
    - Pull-up/Pull-down

        - Signal inversion
        - Pseudo open-drain
    - Counters/Timers
        - 24 Counter/Timers
        - Advanced trigger modes
            - Start/Stop based on other Counter/Timers or GPIO signals
            - Multiple trigger sources
        - Configurable output event
            - One cycle zero detect
            - Active mode
            - Divide by 2
            - PWM compare
    - Interrupt Select
        - Reduced multiple interrupt source down to 1 of 32 supported by processor NVIC
        - Configurable source for alternate Interrupts
            - NMI
            - WatchDog Reset
            - Memory Error Reset
            - Processor Receive Event
    - System Configuration
        - Memory Control
            - Data memory clear on reset
            - Code memory reload on reset
            - Code memory write protect
            - Code/Data memory Scrub rate
            - Code/Data memory error injection for testing
            - Code/Data memory SBE/MBE counters
            - Code/Data memory SBE/MBE Interrupt control
            - EDAC Syndrome calculation support
        - Register Scrub rate control
        - GPIO Glitch Filter rate control
        - Peripheral Configuration
            - Enable/Disable/Reset individual peripherals
- JTAG

- 2 Serial Controllers on same pins
- M0 Debug Controller
  - Provides access to M0 Debug port
- VORAGO Controller
  - Provides standard boundary scan
  - Provides BIST access to memories
  - Provides EFUSE access
  - Provides Test mode access
    - Scan
    - IDDQ
    - I/O Parametric
    - Configuration of Boot sequence
    - Configuration of Memory Margin

- EFUSE
  - 32 Bit Unique ID Number Support
  - Custom part configuration information
    - SPI ROM interface – Delay, Speed, Size, Checking
  - Multiple reconfiguration support (limited to 30 times)

1.3 Power-Up Sequence

The VA10820 auto-detects the Power-Up condition and begins operations by loading the internal code memory from an external Serial Peripheral Interface (SPI) based memory. After loading the code memory, the processor follows a normal ARM® Cortex®-M0 start sequence. See the "VA10800/VA10820 Programmers Guide" for complete details of the Power-Up Sequence.

1.4 Power-Up and Reset Behavior of pins

This section describes the Power-Up and Reset behavior of the GPIO pins on the device.

- At Power-up, an internal SYNC_PORESET signal is asserted asynchronously (without a clock required). For all other reset events the internal SYNC_PORESET signal is asserted synchronously to the clock.
- The SYNC_PORESET signal directly asserts the internal HRESET signal. This signal synchronously resets the processor and peripherals.

- The IO interface unit places all the GPIO pins in the high-Z state while HRESET is active.
- The HRESET is de-asserted after loading the program code from external memory when the processor starts its boot sequence.
- Processor boot code can then configure the pins as needed by the peripheral control registers.

1.5 Other Resets

In addition to the Power-Up reset, the device can be reset from other events:

- EXTRESETn pin
- SYSRESETREQ from software
- Hardware events configured by IRQ Selector Peripheral or the System Controller Peripheral:
    - Processor Lockup
    - Watchdog Timer
    - Memory Errors (Single or Multi-bit errors from the EDAC memory controller)

Based on previous software configuration (in the RST_CNTL_ROM and RST_CNTRL_RAM registers), these resets may or may not re-initialize the memories similar to the Power-Up reset sequence.

See the "VA10800/VA10820 Programmers Guide" for configuration details.

1.6 Support for in system programming of the SPI ROM

To assist in programming the external SPI ROM, the EXTRESETn pin provides additional hardware functionality. While EXTRESETn is active (low), the ROM_SCK, ROM_CSn, and ROM_SO pins are placed in the high-Z state. External hardware can be connected to the pins in the state to access the external SPI ROM.

Note that these pins have dedicated a weak pull-up or pull-down resistors on them keep them is a known state during EXTRESTn. The ROM_CSn has a weak up-up resistor while ROM_SCK and ROM_SO have weak pull-down resistors.

The SPI ROM can also be accessed through the JTAG port using the SPI Encapsulation feature. See the "VA10800/VA10820 Programmers Guide" for details.

1.7 I2C pins

The VA10820 contains 2 sets of dedicated I^2C pins and related I^2C controllers. Each controller can act as both an I^2C master and an I^2C slave simultaneously. These interfaces are capable of operating up to 100 kbits/s in Standard-mode, and up to 400 kbits/s in Fast-mode.

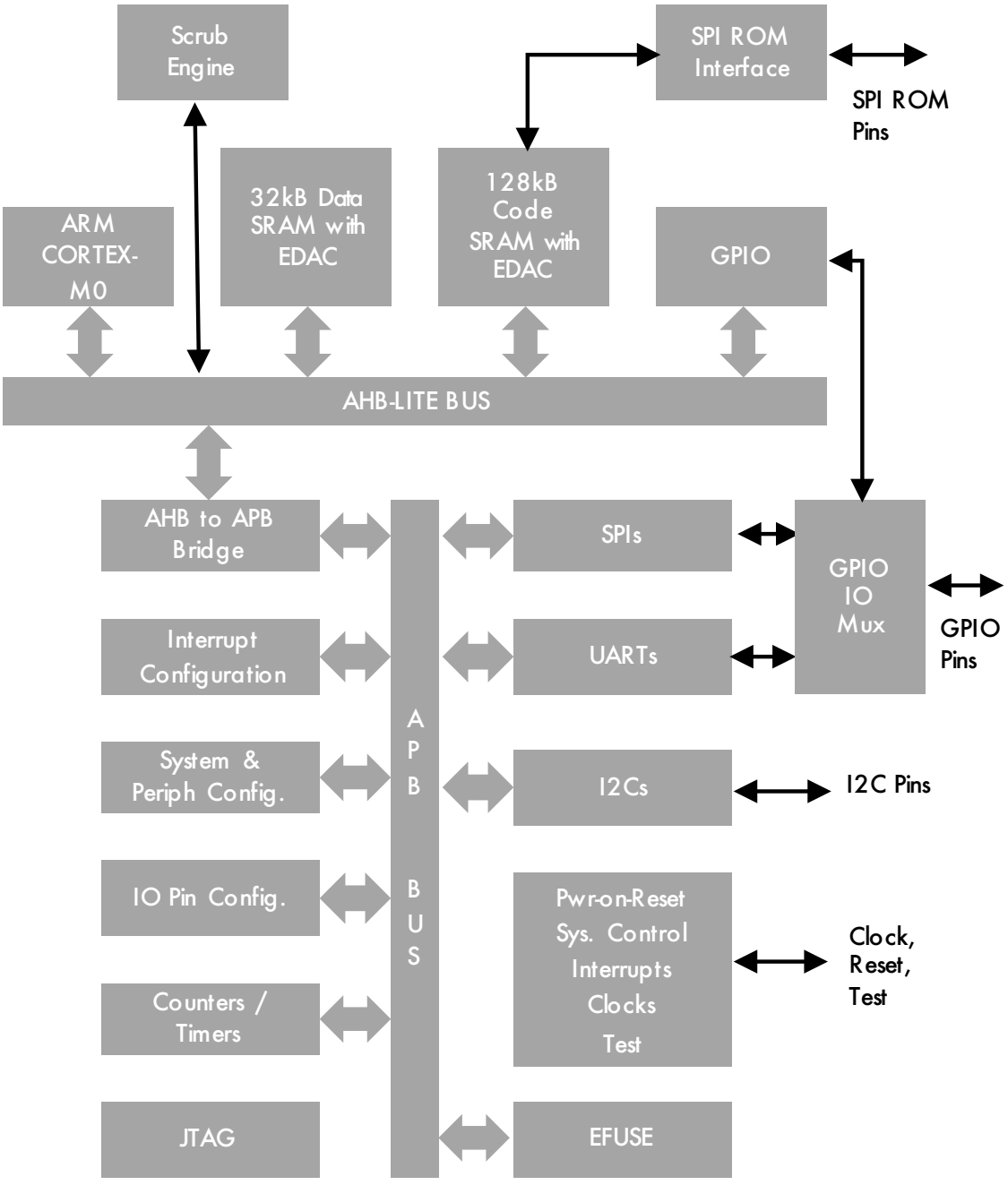
Note, that due to the ESD protection used in the ***HARDSIL®*** process, the device does not meet the non-obstruct feature of I^2C Fast-Mode when this device is powered off. If this non-obstruct feature is required in a system using this part, it will need to be implemented external to the device.

1.8 eFuse Writing

The EF_TIMING register is a 25-bit register used to configure eFuse Write timing. Normally the eFuse is timed from the nominal 1MHz clock. If it is configured (by RESET-CFG) to run from CLK, then these values shoul;d be adjusted accordingly.

Bit	Reset	Description
15:0	0x0009	eFuse Write pulse width (in nominal 1MHz clock periods) minus 1. Should be set to >10µS
20:16	0x00	eFuse Write gap width (in nominal 1MHz clock periods) minus 1. Should be set to >100nS
24:21	0x0	eFuse Read pulse width (in nominal 1MHz clock periods) minus 1. Should be set to >20nS

2 Block Diagram



3 Pin Descriptions

Pin Type	Description	Type	Internal Pull-up/down
	System Pins		
CLK	System Clock. All I/O pin timing is relative to the rising edge of the Clock.	CLOCK	None
EXTRESETn	External System Reset, active low. Resets the processor and all peripherals. This is internally synchronized before being used.	ASync In	None
	General Purpose I/O pins		
PORTA[31:0]	Software configurable General Purpose I/O pins. Software configurable for direction, interrupts sources, and counter/timer triggers. These pins are configurable as the UART and SPI pins as well.	Sync I/O	Software configurable
PORTB[23:0]	Software configurable General Purpose I/O pins. Software configurable for direction, interrupts sources, and counter/timer triggers. These pins are configurable as the UART and SPI pins as well.	Sync I/O	Software configurable
	SPI ROM pins		
ROM_SCK	SPI Clock to Boot ROM.	Sync Out[1]	Pull-down
ROM_CSn	SPI Chip Select to Boot ROM (Active Low).	Sync Out[1]	Pull-up
ROM_SO	SPI Data Out to Boot ROM.	Sync Out[1]	Pull-down
ROM_SI	SPI Data In from Boot ROM.	Sync In	None
	I2C Pins		
I2CA_SCL	I2CA Clock	ASync I/O	None
I2CA_SDA	I2CA Data	ASync I/O	None
I2CB_SCL	I2CB Clock	ASync I/O	None
I2CB_SDA	I2CB Data	ASync I/O	None
	JTAG pins		
TCK	Test Clock.	CLOCK	None
TMS	Test Mode Select.	Sync In	Pull-up
TRSTn	Test Reset, active low.	Sync In	Pull-up
TDI	Test Data In.	Sync In	Pull-up
TDO	Test Data Out.	Sync Out	None
	Other pins		

EFUSE_BURN_ENn	EFuse Burn Enable pin, active low. This pin should be tied to the 3.3V supply during normal operations.	In	Pull-up
DSTPOR	When high this signal disables the Power-On-Reset to the JTAG controllers for test purposes.	In	Pull-down
	Power/Ground/Analog pins		
VDD15	1.5V Core power	Power	
VSS	Ground	Ground	
VDD33	3.3V IO power	Power	

Notes:

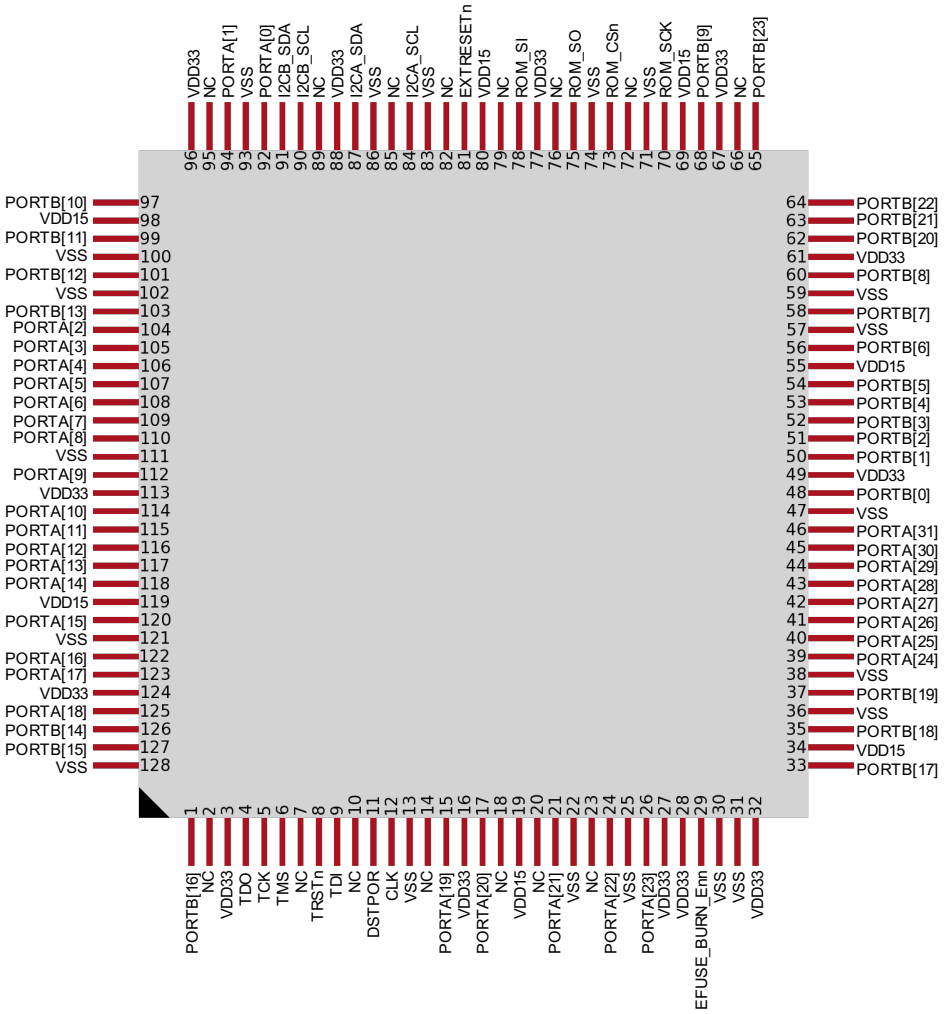
1. Pins ROM_SCK, ROM_CSn, and ROM_SO are normally enabled outputs. When EXTRESETn is active (low) these pins are placed in a high-Z mode with a pull-down on ROM_SCK and ROM_SO; and a pull-up on ROM_CSn. This can be used to assist board level hardware with access to SPI ROM for programming.

4 Package Options

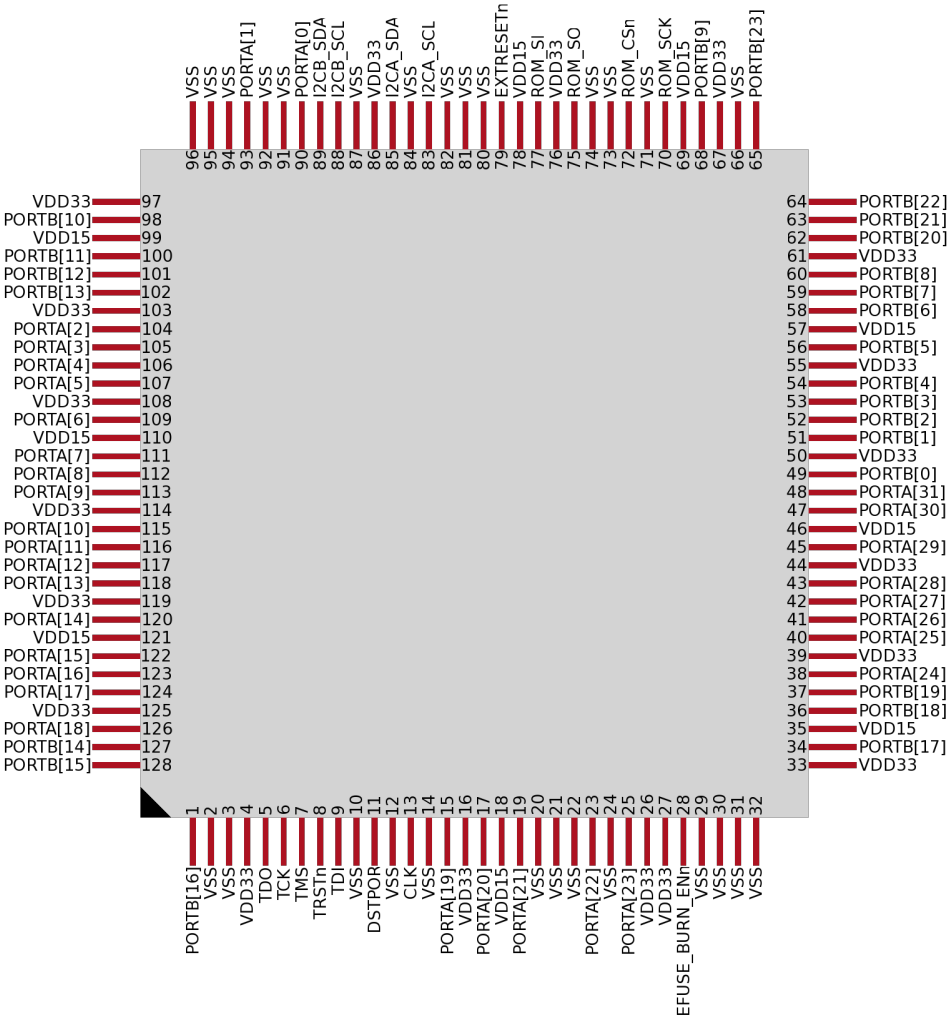
Note that the pinouts on the 128 plastic LQFP and the 128 ceramic LQFP are different as shown in Sections 4.1 and 4.2 below.

It is recommended to tie pins marked 'NC' (No connect) to VSS.

4.1 128 Pin Ceramic LQFP



4.2 128 Pin Plastic LQFP



5 Die Options

The VA10820 microcontroller is available in die form.

Die Size (Without Scribe or Partial Street): X = 7048 um, Y =6712 um

5.1 Table of Die Pad Coordinates from Center of Die in Microns

Pad #	Die Signal Name	X (um)	Y (um)
1	VDDIO_PAD_0	-2760	-3288
2	TDO	-2574	-3288
3	TCK	-2294	-3288
4	TMS	-2014	-3288
5	TRSTn	-1734	-3288
6	TDI	-1454	-3288
7	DSTPOR	-1174	-3288
8	CLK	-894	-3288
9	VSSIO_PAD_0	-614	-3288
10	PORTA[19]	-334	-3288
11	VDDIO_PAD_1	-54	-3288
12	PORTA[20]	226	-3288
13	VDD_PAD_0	506	-3288
14	PORTA[21]	786	-3288
15	VSS_PAD_0	1066	-3288
16	PORTA[22]	1346	-3288
17	VSSIO_PAD_1	1626	-3288
18	PORTA[23]	1906	-3288
19	EFUSE_AVDD_LCUT	2186	-3288
20	EFUSE_AVDD	2313	-3288
21	EFUSE_BURN_ENn	2473	-3288
22	EFUSE_AVSS	2633	-3288
23	EFUSE_AVSS_RCUT	2760	-3288
24	VDDIO_PAD_2	3456	-2870
25	PORTB[17]	3456	-2730
26	VDD_PAD_1	3456	-2590
27	PORTB[18]	3456	-2450
28	VSS_PAD_1	3456	-2310
29	PORTB[19]	3456	-2170
30	VSSIO_PAD_2	3456	-2030

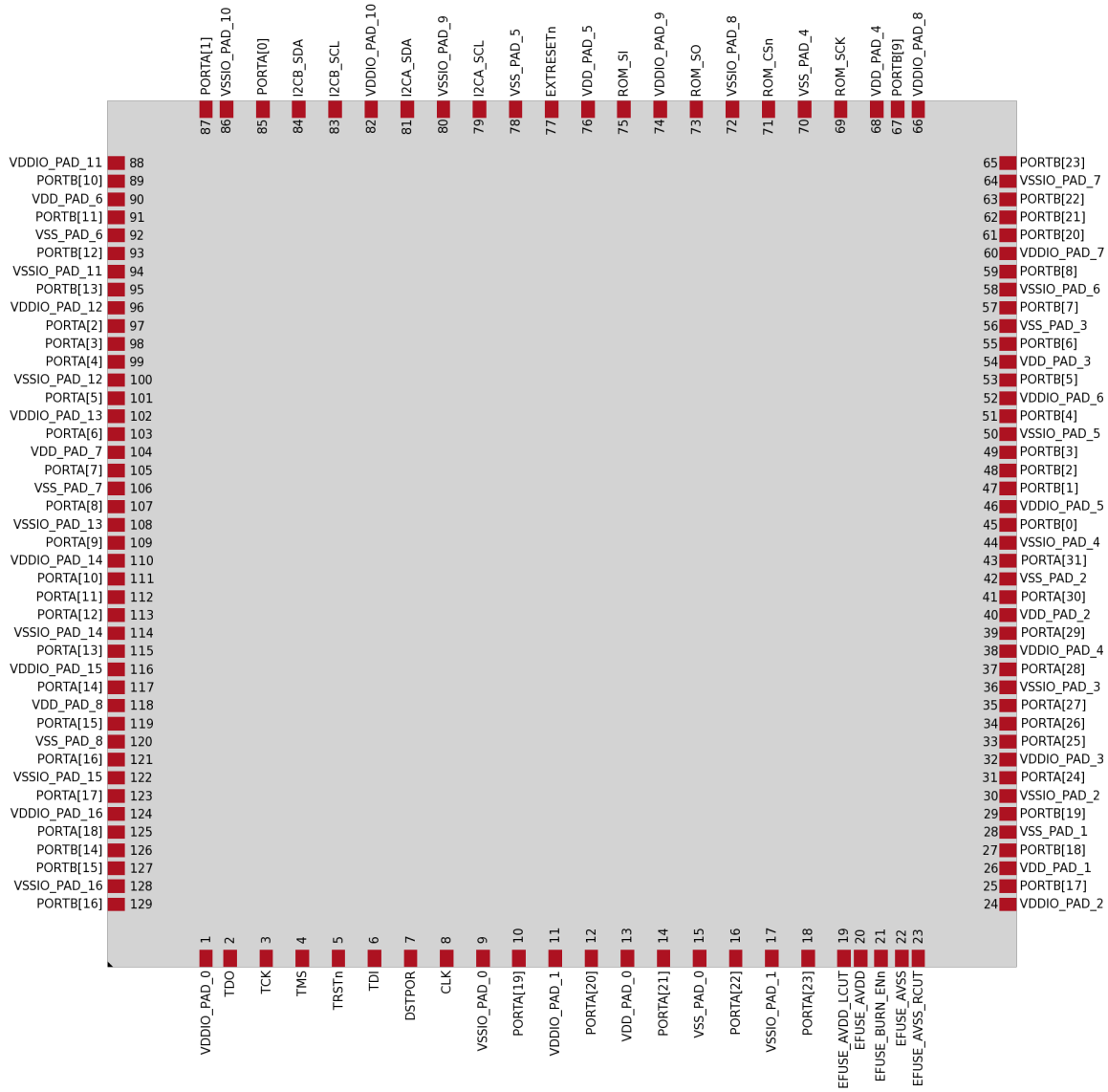
31	PORTA[24]	3456	-1890
32	VDDIO_PAD_3	3456	-1750
33	PORTA[25]	3456	-1610
34	PORTA[26]	3456	-1470
35	PORTA[27]	3456	-1330
36	VSSIO_PAD_3	3456	-1190
37	PORTA[28]	3456	-1050
38	VDDIO_PAD_4	3456	-910
39	PORTA[29]	3456	-770
40	VDD_PAD_2	3456	-630
41	PORTA[30]	3456	-490
42	VSS_PAD_2	3456	-350
43	PORTA[31]	3456	-210
44	VSSIO_PAD_4	3456	-70
45	PORTB[0]	3456	70
46	VDDIO_PAD_5	3456	210
47	PORTB[1]	3456	350
48	PORTB[2]	3456	490
49	PORTB[3]	3456	630
50	VSSIO_PAD_5	3456	770
51	PORTB[4]	3456	910
52	VDDIO_PAD_6	3456	1050
53	PORTB[5]	3456	1190
54	VDD_PAD_3	3456	1330
55	PORTB[6]	3456	1470
56	VSS_PAD_3	3456	1610
57	PORTB[7]	3456	1750
58	VSSIO_PAD_6	3456	1890
59	PORTB[8]	3456	2030
60	VDDIO_PAD_7	3456	2170
61	PORTB[20]	3456	2310
62	PORTB[21]	3456	2450
63	PORTB[22]	3456	2590
64	VSSIO_PAD_7	3456	2730
65	PORTB[23]	3456	2870
66	VDDIO_PAD_8	2760	3288
67	PORTB[9]	2600	3288
68	VDD_PAD_4	2440	3288
69	ROM_SCK	2160	3288

70	VSS_PAD_4	1880	3288
71	ROM_CSn	1600	3288
72	VSSIO_PAD_8	1320	3288
73	ROM_SO	1040	3288
74	VDDIO_PAD_9	760	3288
75	ROM_SI	480	3288
76	VDD_PAD_5	200	3288
77	EXTRESETn	-80	3288
78	VSS_PAD_5	-360	3288
79	I2CA_SCL	-640	3288
80	VSSIO_PAD_9	-920	3288
81	I2CA_SDA	-1200	3288
82	VDDIO_PAD_10	-1480	3288
83	I2CB_SCL	-1760	3288
84	I2CB_SDA	-2040	3288
85	PORTA[0]	-2320	3288
86	VSSIO_PAD_10	-2600	3288
87	PORTA[1]	-2760	3288
88	VDDIO_PAD_11	-3456	2870
89	PORTB[10]	-3456	2730
90	VDD_PAD_6	-3456	2590
91	PORTB[11]	-3456	2450
92	VSS_PAD_6	-3456	2310
93	PORTB[12]	-3456	2170
94	VSSIO_PAD_11	-3456	2030
95	PORTB[13]	-3456	1890
96	VDDIO_PAD_12	-3456	1750
97	PORTA[2]	-3456	1610
98	PORTA[3]	-3456	1470
99	PORTA[4]	-3456	1330
100	VSSIO_PAD_12	-3456	1190
101	PORTA[5]	-3456	1050
102	VDDIO_PAD_13	-3456	910
103	PORTA[6]	-3456	770
104	VDD_PAD_7	-3456	630
105	PORTA[7]	-3456	490
106	VSS_PAD_7	-3456	350
107	PORTA[8]	-3456	210
108	VSSIO_PAD_13	-3456	70

109	PORTA[9]	-3456	-70
110	VDDIO_PAD_14	-3456	-210
111	PORTA[10]	-3456	-350
112	PORTA[11]	-3456	-490
113	PORTA[12]	-3456	-630
114	VSSIO_PAD_14	-3456	-770
115	PORTA[13]	-3456	-910
116	VDDIO_PAD_15	-3456	-1050
117	PORTA[14]	-3456	-1190
118	VDD_PAD_8	-3456	-1330
119	PORTA[15]	-3456	-1470
120	VSS_PAD_8	-3456	-1610
121	PORTA[16]	-3456	-1750
122	VSSIO_PAD_15	-3456	-1890
123	PORTA[17]	-3456	-2030
124	VDDIO_PAD_16	-3456	-2170
125	PORTA[18]	-3456	-2310
126	PORTB[14]	-3456	-2450
127	PORTB[15]	-3456	-2590
128	VSSIO_PAD_16	-3456	-2730
129	PORTB[16]	-3456	-2870

5.2 Pad Layout with Marking in Upper Left Corner of Die

Note: Upper Left Corner Metal Fill Missing + Layer Markings



For Pad Naming VDDIO = VDD33, VDD = VDD15

6 Ratings Tables

6.1 Absolute Maximum Ratings

Symbol	Rating	Hi Rel	Unit
VVDD15	DC supply voltage(core)	-0.3 to 1.8	V
VVDD33	DC supply voltage (I/O)	-0.3 to 3.8	V
$V_{I/O}$	Voltage on any pin	-0.3 to 3.8	V
T_{CASE}	Operating Temperature	-55 to 125	˚C
T_{STG}	Storage Temperature	-55 to 125	˚C

6.2 Recommended Supply Operating Condition

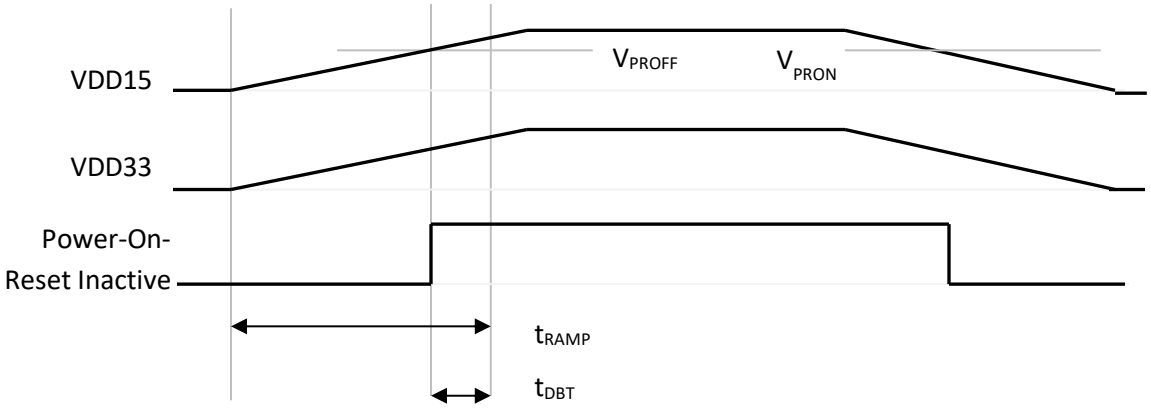
Grade	Temperature	VSS	VDD15	VDD33
Extreme	-55˚ to 125˚C	0V	1.5V +/-10%	3.3V +/-10%

6.3 Recommended Supply Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VVDD15	Core Supply	1.35	1.5	1.65	V
VVDD33	I/O Supply Voltage	3.0	3.3	3.6	V
VSS	Ground	0	0	0	V
V_{ramp1}	VDD15 voltage ramp time[1]	100			uS
V_{ramp2}	VDD33 voltage ramp time[1]	100			uS
V_{PROFF1}	VDD15 level at which the Power-On-Reset is released[2]	1.00	1.11	1.20	V
V_{PROFF2}	VDD33 level at which the Power-On-Reset is released[2]	2.2	2.4	2.7	V
V_{PRON1}	VDD15 level at which the Power-On-Reset is activated[3]	0.90	1.01	1.15	V
V_{PRON2}	VDD33level at which the Power-On-Reset is activated[3]	1.7	2.0	2.2	V
t_{DBT}	Default boot delay. The time from VDD15/VDD33 at V_{PROFF} until supplies reach operating range[2,4] and input clock is valid[6].		30[5]		ms

Notes:

1. Ramp time is the time from VDD15/VDD33 at 0V until it reaches the operating range. The Maximum value will depend on t_{DBT} (Boot Delay) and the Clock frequency (if clock is running during power the power up sequence).
2. V_{PROFF} is the voltage at which the internal Power-on-Reset is released when power is rising. The EFuse and boot delay logic both begin operating at this point and will operate correctly at this reduced voltage. The programmed boot delay needs to be specified so that t_{DBT} is sufficient for the VDD15 and VDD33 to have reached the operating range in the specified time, for the rest of the device to operate correctly.
3. V_{PRON} is the voltage at which the internal Power-on-Reset is activated when power is falling or during a VDD15 glitch.
4. t_{DBT} can be reconfigured through Efuse data using the JTAG port.
5. Time value is based on a 30000 clock cycles of the internal nominal 1MHz oscillator.
6. Clock CLK should be valid after the default boot delay time. Valid requires that the level be stable and any transitions meet the required min high and min low times (this implies it can be held in the off state).



6.4 Signal Pads Operating Conditions

6.4.1 Non- I2C Pads

This applies to pads except: I2CA_SCL, I2CA_SDA, I2CB_SCK, and I2CB_SDA.

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage		-0.3	0.8	V
V_{IH}	Input High Voltage		2	VDD33 +0.3	V
V_{hys} [1]	Hysteresis of Schmitt trigger		60	350	mV
I_{OL}	Low level sink current	V_{OL}=0.4V, VDD33= Min	8		mA
I_{OH}	High level source current	V_{OH}=2.4V, VDD33= Min	8		mA

6.4.2 Leakage Current non-I2C pads

Symbol	Parameter	Pins	Test Conditions	Temperature	Min.	Typ.	Max.
II	Input leakage current (Vin low)	Pins with configurable pull-up or pull-down (Port A, Port B)	Vin= 0V	-55 to 125	-1µA	<-1nA	-
		DSTPOR (internal pull-down)	Vin= 0V	-55 to 125	-1µA	-	1µA
		TMS, TRSTn, TDI, EFUSE_BURN_En (internal pull-up)	Vin= 0V	-55 to 125	-65µA	-50µA	-
		CLK, TCK, TDO, ROM_SI, EXTRESETn	Vin= 0V	-55 to 125	-1µA	<-1nA	-
	Input leakage current (Vin high)	Pins with configurable pull-up or pull-down (Port A, Port B)	Vin=VDD33	-55 to 125	-	<1nA	1µA
		DSTPOR (internal pull-down)	Vin=VDD33	-55 to 125	-	75µA	85µA
		TMS, TRSTn, TDI, EFUSE_BURN_En (internal pull-up)	Vin=VDD33	-55 to 125	-	<1nA	1µA
		CLK, TCK, TDO, ROM_SI, EXTRESETn	Vin=VDD33	-55 to 125	-	<1nA	1µA

Notes:

1. The following input buffers have Schmitt Trigger Inputs: TCK, TRSTn, CLK
2. TYP for -55˚ to 125˚C measured at 25˚C

6.4.3 VOL, VOH non-I2C pads

Symbol	Parameter	Test Conditions	Temperature	Min.	Typ.	Max.	Unit
VOL	Output voltage	Load I = 8mA,	-55 to 125	-	0.25	0.4	V
VOH	Output voltage	Load I = 8mA,	-55 to 125	2.4	2.5	-	V

Notes:

1. TYP for -55˚ to 125˚C measured at 25˚C

6.4.4 I2C pads

This applies to pads: I2CA_SCL, I2CA_SDA, I2CB_SCL, I2CB_SDA

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage		-0.3	1.09 (see note 1)	V
V_{IH}	Input High Voltage		2.1 (see note 2)	VDDIO +0.3	V
V_{hys}	Hysteresis of Schmitt trigger		182 (see note 3)	-	mV
I_{OL1}	Low level sink current	V_{OL}=0.4V, VDD33= Min	4	-	mA
I_{OL2}	Low level sink current	V_{OL}=0.6V, VDD33= Min	6	-	mA

Notes:

1. This value is 0.3 * VVDD33 VDD33(MAX)
2. This value is 0.7 * VVDD33 VDD33(MIN)
3. This value is 0.05 * VVDD33 VDD33(MAX)

6.4.5 Input Leakage Current and Output Voltage I2C Pads

Symbol	Parameter	Pins	Test Conditions	Temperature	Min.	Typ.	Max.
II	Input leakage current (High)	I2C Pins (Tri-state)	Vin= VDD33	-55 to 125	-	<-1nA	1µA
VOL	Output Voltage (Low)	I2C Pins	Load I = 4mA, VDD33=Min	-55 to 125	-	0.3V	0.42V
			Load I = 6mA, VDD33=Min	-55 to 125	-	0.42V	0.6V

Notes:

1. TYP for -55˚ to 125˚C measured at 25˚C

6.5 DC Current Consumption

Symbol	Condition	Typ[1]	WCPOW[2]	Supply	Unit
I_{Idd}	Max core current at 50MHz with maximum activity (see note 1)	105	135	VDD15	mA
	Max core current at 50MHz with minimum activity (see note 2)	20	25	VDD15	mA

Notes:

1. Maximum activity is with all internal counters running at maximum rate, all I^2C interfaces active in Fast-Mode and loopback, all SPI active in master mode at 16x clock divide rate, and all UARTs active in loopback mode at 1MHz Baud rate, processor running multiply operations.
2. Minimum activity is with all peripheral clocks disabled except 1 Timer/Counter to generate interrupts, and the M0 in sleep mode.

6.6 DC Standby Current Consumption

Symbol	Parameter	Temperature	Min.	Typ.	Max.
ISB	I Standby Core	-55 to 125	-	0.17mA	3mA
	I standby IO	-55 to 125	-	0.47mA	1.25mA

Notes:

1. TYP for -55˚ to 125˚C measured at 25˚C

6.7 Internal Weak Pull-up/Pull-down

	Typ Value	Units
Pull-up	33	Kohms
Pull-down	33	Kohms

Notes:

1. Pins with dedicated Pull-ups: TMS, TRSTn, TDI, ROM_CSn, EFUSE_BURN_ENn
2. Pins with dedicated Pull-downs: ROM_SCK, ROM_SO
3. Pins with software configurable Pulls: PORTA[31:0], PORTB[23:0]

6.8 Post Total Ionizing Dose (TID) Current Consumption

These tables indicate the leakage current measured immediately following irradiation of 300K Rad (Si) at a Dose Rate of 84 rad(Si)/S, measured with all I/O in Tri-State or pull-down mode.

6.8.1 Post-TID Leakage Current non-I2C Pads

Symbol	Parameter	Pins	Test Conditions	Temperature	Min.	Typ.	Max.
II	Input leakage current (Vin high)	Pins with configurable pull-up or pull-down	Vin=VDD33	-55 to 125	-	50uA	100uA
		DSTPOR (internal pull-down)	Vin=VDD33	-55 to 125	-	125uA	185uA
		TMS, TRSTn, TDI, EFUSE_BURN_En (internal pull-up)	Vin=VDD33	-55 to 125	-	50uA	100uA
		Tri-State Pins	Vin=VDD33	-55 to 125	-	50uA	100uA

Notes:

1. Input leakage current (Vin low) unchanged from Table 6.4.2
2. Typ. measured at 25˚C at 50% duty cycle during irradiation

6.8.2 Post-TID Leakage Current I2C Pads

Symbol	Parameter	Pins	Test Conditions	Temperature	Min.	Typ.	Max.
II	Input leakage current (High)	I2C Pins (Tri-state)	Vin= VDD33	-55 to 125	-	50uA	100uA

Notes:

1. Typ. measured at 25˚C at 50% duty cycle during irradiation

6.8.3 Post-TID Standby Current Consumption

Symbol	Parameter	Temperature	Min.	Typ.	Max.
ISB	I Standby Core	-55 to 125	-	0.35mA	3.2mA
	I standby IO	-55 to 125	-	11.5mA	15mA

Notes:

1. Typ. measured at 25˚C at 50% duty cycle during irradiation

6.9 128 pin QFP Pin Capacitance

Symbol	Parameter	Conditions	Max	Unit
C_{IN}[1]	Input Capacitance	Vin = 3.3 V	6	pF
$C_{I/O}$[2]	I/O Capacitance	Vout = 3.3 V	10	pF

Notes:

1. Input Only pins: CLK, ROM_SI, TCK, TMS, TDI, EXTRESETn
2. Bidirectional pins: PORTA[31:0], PORTB[23:0], I2C*

7 AC Electrical Characteristics

7.1 AC Timing Conditions

VVDD15$_{VDD15}$	1.5V +/- 10%
VVDD33$_{VDD33}$	3.3V +/- 10%
Input Swing Levels	0 to 3.3V
Input Rise/Fall Times	1-4 ns[1]
Input Timing Reference Levels	1.65V
Output Timing Reference Levels	1.65V
AC Test Load	20pf

Notes:

1. Rise/Fall times are measured from 20% to 80% of VDDIO

7.1.1 Output delay derating for loads

The following table shows the effect of various output loads on the output data valid timing:

Load	t_{DV}(Min[1])	t_{DV}(Typ[1])	t_{DV}(Max[1])	Units
5pf	A-0.7	B-0.6	C-1.0	ns
20pf	A[2]	B[2]	C[2]	ns
35pf	A+0.8	B+0.6	C+0.8	ns

Notes:

1. Delay Value over normal operating conditions:
   a. Best case military (-55˚C, VVDD15+10%,, VVDD33+10%, fast/fast process)
   b. Typical (25˚C, VDD, typical/typical process)
   c. Worst case military (125˚C, VVDD15-10%, VVDD33-10%, slow/slow process)
2. A, B, and C represent the reference delay values for a given IO signals (at 20pf Load)

7.2 Internal Nominal 1 MHz Oscillator

The internal nominal 1 MHz oscillator is used for Power-Up delay timing.

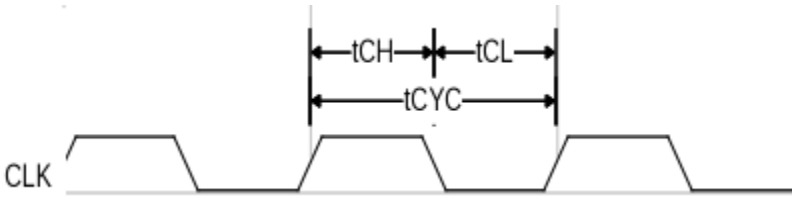
Parameter	Description	Min	Typ	Max	Unit
t_{FREQ}	Clock frequency	1.0	1.2	1.7	MHz

7.3 Clock Signal

Parameter	Description	Time	Unit
t_{CYC}	Clock cycle time (min)[1]	20	ns
t_{CH}	Clock high (min) [1]	8	ns
t_{CL}	Clock low (min) [1]	8	ns

Notes:

1. t_{CH} + t_{CL} must equal t_{CYC}, so only one of these can be at the minimum value.

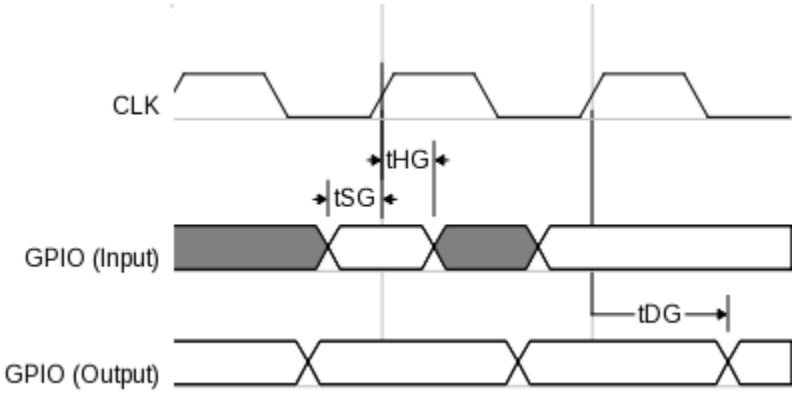


7.4 GPIO PORTA/PORTB

Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit
t_{DG}	GPIO output valid after CLK rise	4.5	11	18	ns
t_{SG}[2,3]	GPIO input setup before CLK rise	3.0	-	-	ns
t_{HG}[2,3]	GPIO input hold after CLK rise	6.5	-	-	ns

Notes:

1. Over normal operating conditions:
   a. Best case military (-55˚C, VVDD15+10%, VVDD33+10%, fast/fast process)
   b. Typical (25˚C, VDD, typical/typical process)
   c. Worst case military (125˚C, VVDD15-10%, VVDD33-10%, slow/slow process)
2. Setup and Hold times only apply when GPIO pin synchronization is disabled.
3. These times are across all configuration options of these pins (GPIO, SPI, or UART).



7.5 I2C pins

The I²C bus requires an external pull-up resistor or current-source on the bus, which needs to be sized to the desired load based on the I²C specification.

The timing of the I²C pins is designed to meet the I²C specification for Standard and Fast modes.

I²C pin timing in Master mode is based on an internal ICLK and default values in the I²C TMCONFIG register. ICLK must have a minimum period of 500ns in Standard mode and 100ns in Fast mode.

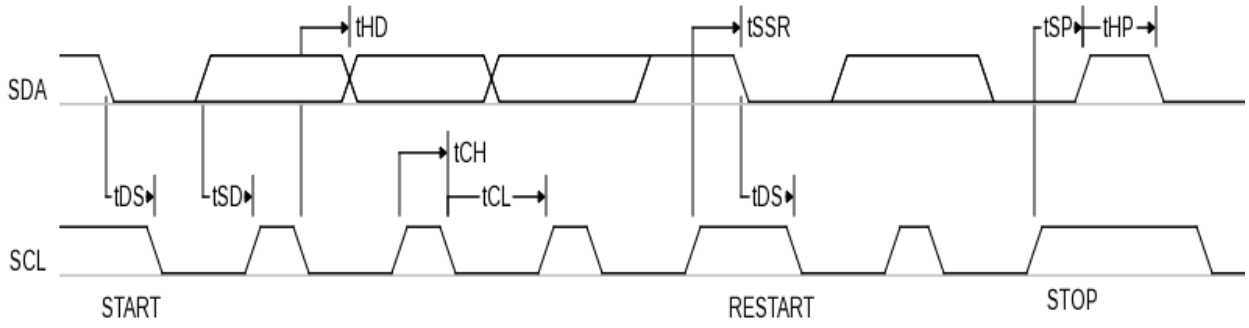
Parameter	Description[2]	Condition[3]	Standard-Mode[1,4]		Fast-Mode[1,5]	
			Cycles	µs	Cycles	µs
t_{DS}	START Delay from SDA to SCL	Start of SDA to Start of SCL	9	4.5	9	0.9
t_{SD}	Setup of SDA to SCL rise	Start of SDA to Start of SCL	8	4.0	12	1.2
t_{HD}	Hold of SDA after SCL fall	Start of SCL to Start of SDA	2	1.0	4	0.4
t_{CH}	High time of SCL	Start of SCL to Start of SCL	10	5.0	9	0.9
t_{CL}	Low time of SCL	Start of SCL to Start of SCL	10	5.0	16	1.6
t_{SSR}	Setup SCL to SDA for RESTART	Start of SCL to Start of SDA	12	6.0	9	0.9
t_{SP}	Setup of SCL to SDA for STOP	Start of SCL to Start of SDA	10	5.0	9	0.9
t_{HP}	Hold of SDA after STOP	Start of SDA to Start of SDA	12	6.0	16	1.6

Notes:

1. I²C pin timing in Master mode is based on an internal ICLK and default values in the I²C TMCONFIG register. ICLK must have a minimum period of 500ns in Standard mode and 100ns in Fast mode.
2. Timing is for the internal state machine change, which reflects the start of a signal change. This will typically include the rise/fall time of some signals. The fall times are based on the C_{LOAD} on the I²C output buffer. The rise times are based on the C_{LOAD} and the external pull-up on the I²C output buffer. It is assumes that for the C_{LOAD} given load and pull-up that the rise and fall times are within the I²C specification values (Rise

being 1.0µs for Standard mode, and 0.3µs for Fast mode; Fall being 0.3µs for either mode).

3. The condition specifies which starting edges are involved in this measurement.
4. Cycles are cycles of the ICLK in Standard mode. Time in ns is for ICLK of 500ns in Standard mode.
5. Cycles are cycles of the ICLK in Fast mode. Time in ns is for ICLK of 100ns in Fast Mode.



7.6 I2C Pin Timing

Parameter	Description	Condition	Min	Max	Units
t_F	Fall time of SDA or SCL	From 70% to 30% of VDD33 For valid values of C_{LOAD}	15	300	ns
$t_{R\text{-}STD}$[1]	Rise time of SDA or SCL Standard mode	From 30% to 70% of VDD33 For valid values of C_{LOAD}		1000	ns
$t_{R\text{-}FAST}$[1]	Rise time of SDA or SCL Fast mode	From 30% to 70% of VDD33 For valid values of C_{LOAD}	20	300	ns
C_{LOAD}	Capacitance load on SDA or SCL			400	pF
t_{SP}	Pulse width of input noise spike that is suppressed by input filter		50		ns

Notes:

1. I^2C pin rise time is determined by external pull-up and not the device. Values listed are the I^2C specification values for reference purposes.

7.7 SPI ROM

This section describes the SPI boot ROM pins, which are used during the boot process and are available as the SPI-C port to the processor.

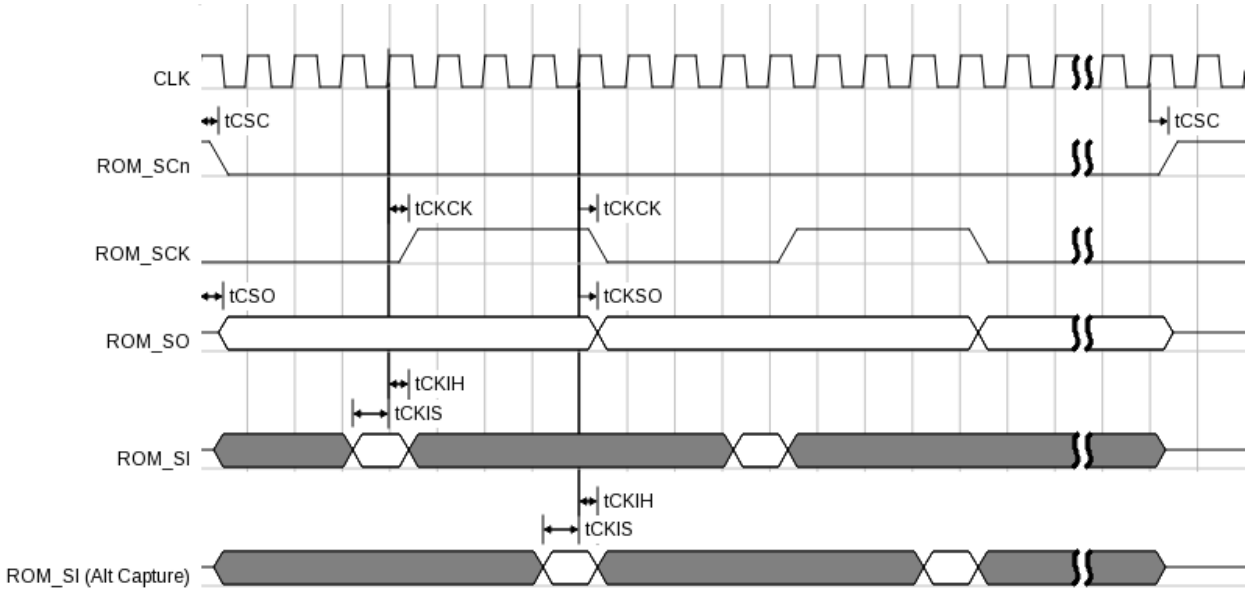
Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit
t_{CSC}	ROM_CSn valid after CLK rise	4	15	17	ns
t_{CKCK}	ROM_SCK valid after CLK rise	4	15	17	ns
t_{CSO}[2]	ROM_SO valid after CLK rise when ROM_CSn changes	4	15	17	ns
t_{CKSO}[2]	ROM_SO valid after CLK rise	4	15	17	ns
t_{CKIS}[3]	ROM_SI setup before CLK rise	0	-	-	ns
t_{CKIH}[3]	ROM_SI hold after CLK rise	7.5	-	-	ns

Notes:

1. Over normal operating conditions:
   a. Best case military (-55˚C, VVDD15+10%, VVDD33+10%, fast/fast process)
   b. Typical (25˚C, VDD, typical/typical process)
   c. Worst case military (125˚C, VVDD15-10%, VVDD33-10%, slow/slow process)

2. ROM_SO changes on the cycles that ROM_SCK falls.
3. The ROM_SI signal is captured on the rising edge of CLK on the cycles that ROM_SCK will be rising at the output. ROM_SI can be configured to be captured on the cycles that ROM_SCK will be falling at the output; this mode allows a longer time for the external ROM to respond, which can result in a faster data rate. This late capture is non-standard SPI, but will work properly since the ROM_SI value is will be capture internally before ROM_SCK is generated out of the chip.

When used during the SPI boot process, the ROM_SCK clock is generated from the CLK clock by dividing it down. The EFuse can be used to program this as divide by 2, 6, 12, or 52. The default is to divide by 6. See the BOOT_CFG section of the "VA10800/VA10820 Programmers Guide".

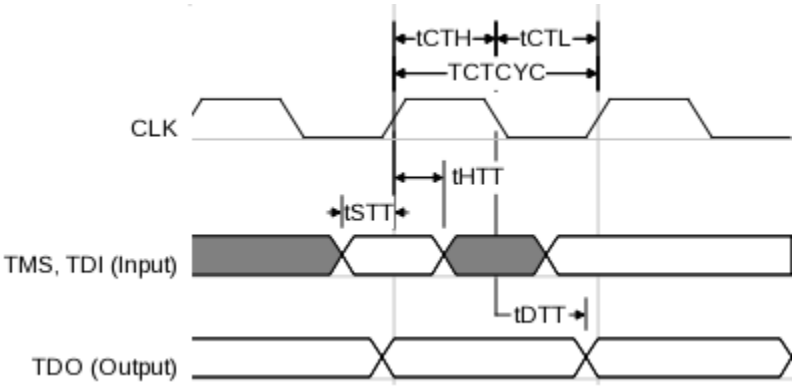


7.8 JTAG

Parameter	Description	Min[1]	Typ[1]	Max[1]	Unit
t_{CTCYC}	TCK cycle time (min)[2]	60	-	-	ns
t_{CTH}	TCK high (min)[2]	20	-	-	ns
t_{CTL}	TCK low (min)[2]	20	-	-	ns
T_{DTT}	TDO output changed from TCK fall[3]	3.0	9	14	ns
T_{STT}	TMS/TDI setup time to TCK rise	2.0	-	-	ns
T_{HTT}	TMS/TDI hold time to TCK rise	6.0	-	-	ns

Notes:

1. Over normal operating condition:
   a. Best case military (-55˚C, VVDD15+10%, VVDD33+10%, fast/fast process)
   b. Typical (25˚C, VDD, typical/typical process)
   c. Worst case military (125˚C, VVDD15-10%, VVDD33-10%, slow/slow process)
2. t_{CTH} + t_{CTL} must equal t_{CTCYC}, so only one of these can be at the minimum value.
3. Includes both change in value or change in enable.



8 Radiation Hardened Performance

Parameter	Description	Min	Typ	Max	Unit
TID	Total Ionizing Dose	300K	-	-	rad (Si)
SER	Soft Error Rate (EDAC disabled)	-	-	1.3e7	errors / bit / day*
SER	Soft Error Rate (EDAC enabled)	-	-	1e-15	errors / bit / day*
LET	Linear Energy Transfer (latch-up immunity)	110	-	-	MeV-cm2 / mg
SEFI	Single Event Functional Interrupt			1e-9	upsets / device /day

*Geosynchronous orbit solar min. with 100 mils of Al shielding

With EDAC enabled, the Scrub Engine should also be enabled and running at an appropriate frequency to prevent accumulation of errors in the memory in order to achieve consistently low SER over time.

9 Thermal Characteristics

Package Type	Specification	Symbol	Max	Nominal	Min	Units
Plastic QFP	Junction temperature	Tj	130.5			°C
	Case temperature	Tc	125		-55	°C
	Thermal resistance (junction to case), 2-layer PCB	θjc		15.9		°C/W
	Thermal resistance (junction to case), 4-layer PCB	θjc		14.6		°C/W
	Thermal resistance (junction to ambient), 2-layer PCB	θja		21.4		°C/W
	Thermal resistance (junction to ambient), 4-layer PCB	θja	-	20.4		°C/W
Ceramic QFP	Junction temperature	Tj	126.2			°C
	Case temperature	Tc	125		-55	°C
	Thermal resistance (junction to case)	θjc		3.2		°C/W
	Thermal resistance (junction to ambient)	θja		30		°C/W

10 Electrostatic Discharge (ESD) Protection Charcteristics

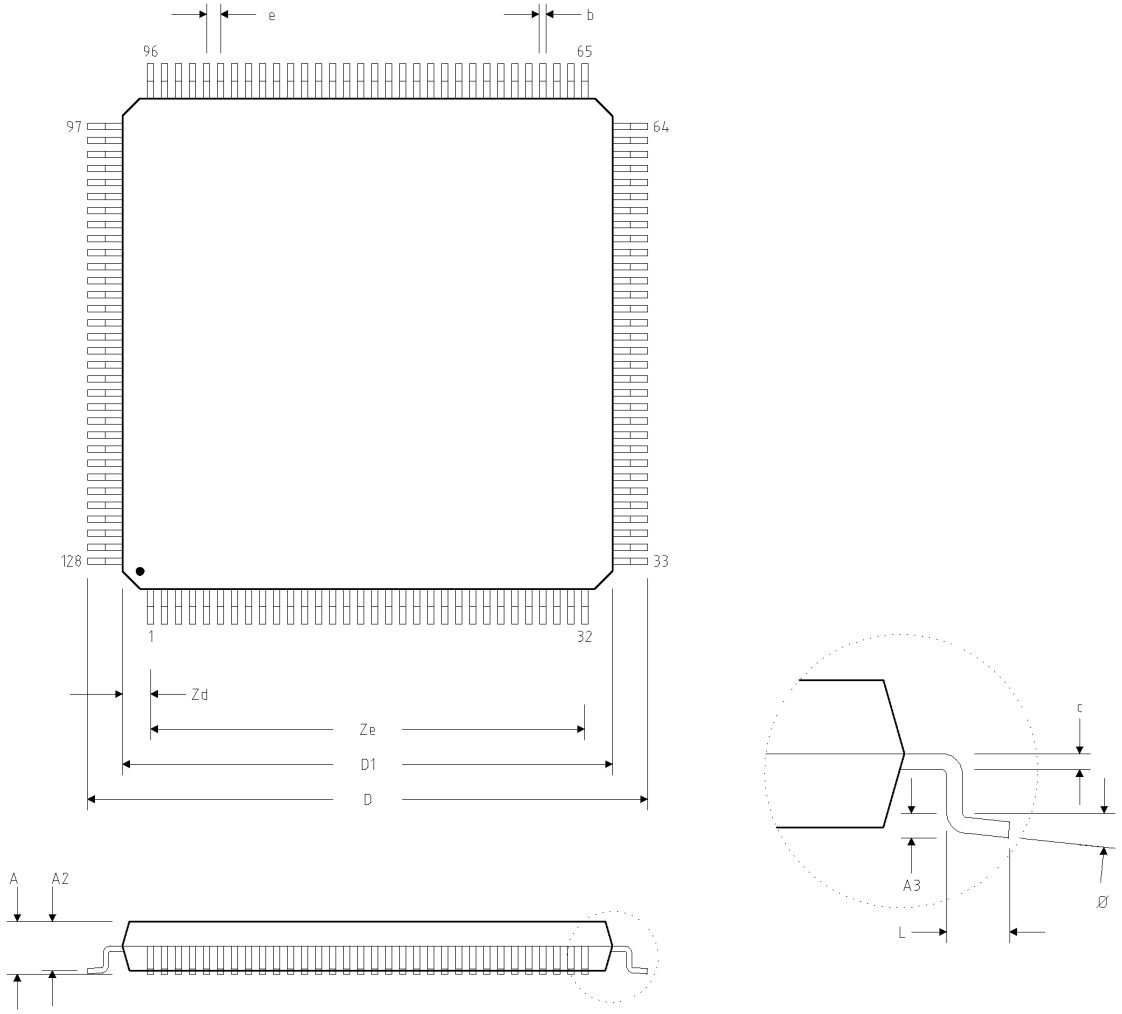
VORAGO has performed ESD testing to meet qualification levels shown in the table below. The silicon die has ESD protection implemented on every pin including the JTAG interface.

Parameter	Description	Value	Units	Specification
HBM	Human Body Model	4000	V	JS-001-2014
CDM	Charged Device Model	500	V	JS-002-2014

11 Package Mechanical Information

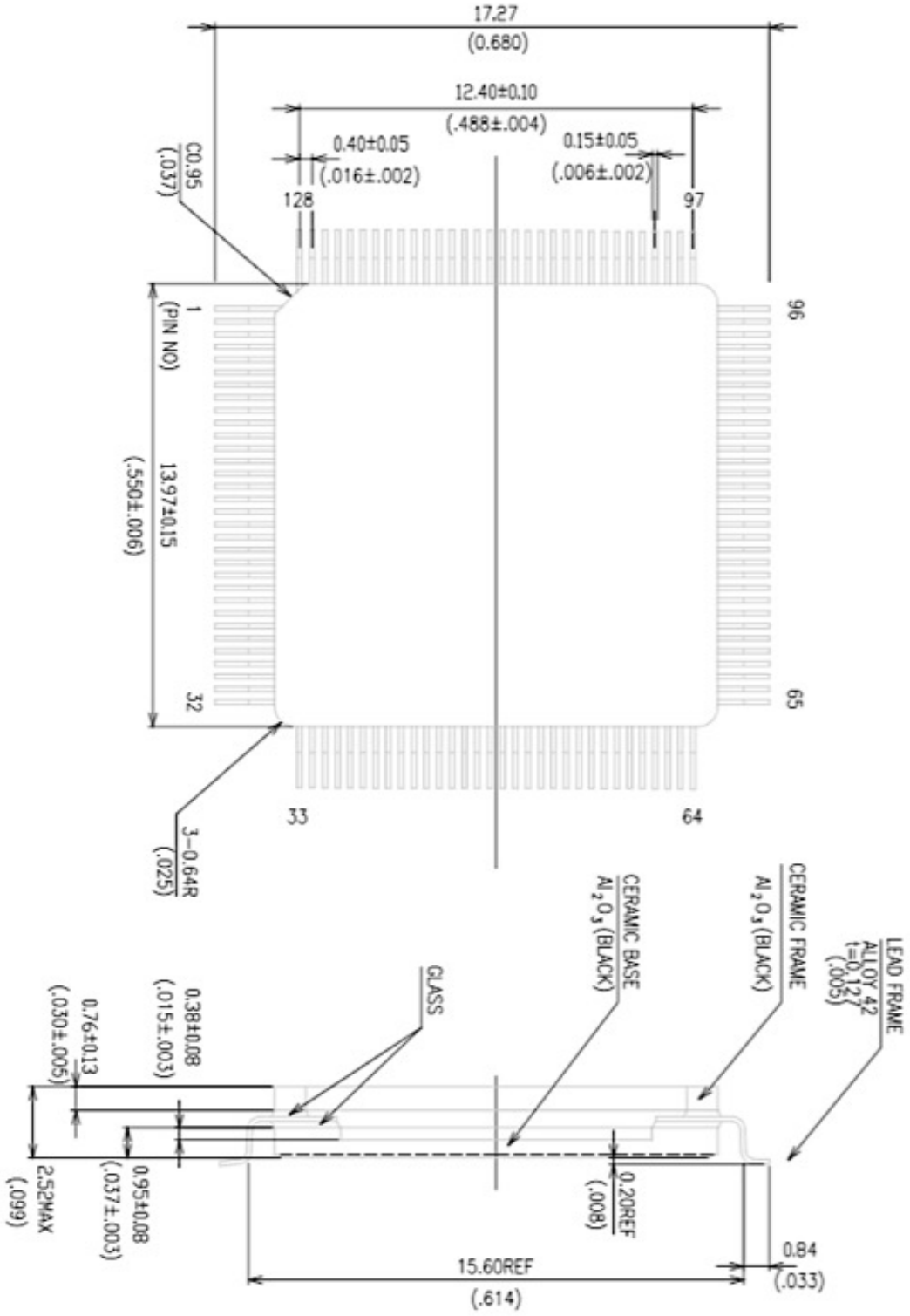
11.1128 Pin Plastic LQFP Nominal Package Dimensions (mm)

Lead Count	Body Size	Body Thickness	Lead Pitch	Lead Form	Standoff	Foot Length	Tip-to-Tip	JEDEC
128	14x14	1.40	0.40	1.00	0.10	0.60	16.0	MS-026



UNIT	A	A2	A3	b	c	D	D1	e	L	Zd	Ze	Ø
mm	1.60	1.45 1.35	0.25	0.23 0.13	0.20 0.09	16.00	14.00	0.40	0.75 0.45	0.80	12.40	0°-7°

11.2 128 Pin Ceramic LQFP Nominal Package Dimensions (mm)



12 Ordering Information

Part Number	Environment	Package
VA10820-CQ128F0ECA	Radiation hardened	Ceramic 128 LQFP
VA10820-PQ128F0PCA	Radiation hardened	Plastic 128 LQFP
VA10820-D0000F0PCA	Radiation hardened	Die

12.1 Part Marking

The marking on the ceramic version of the device follows the format shown:

Line 1: Company Name	VORAGO
Line 2: Part Number:	VA10800-CQ128XX
Line 3: Assembly Trace Code:	YYWW**R**RXXX-W##
Line 4: ARM Product Trademark	ARM® Cortex® - M0

To identify the revision number of the silicon, see the fifth digit on Line 3. This is highlighted in the table in bold and underlined.

13 Development kit Ordering Information

Part Number	Features
REB1-VA10820	Supported by Keil™ MDK-ARM Microcontroller Software kit BSP includes example software for peripherals Segger J-Link OB

14 Errata

VOR-ER1001: Hard fault can occur during debug activity		
Description	**Workaround**	**Comment**
When a debug communication occurs at the same time as the CPU is performing a read or write access to an APB based peripheral register, it is possible that a hard fault interrupt is incorrectly generated. **This error will not occur in normal user mode when a debugger is not attached.**	Implement an interrupt service routine that unpacks the hard fault stack frame and jumps to the address specified by the program counter at the time when the hard fault occurred. This interrupt service routine is included in the BSP available to download at *www.voragotech.com/products/reb1*	The silicon fix has been applied to the latest revision of silicon – these fixed versions are given in the latest part number table shown in section 10 'Ordering Information'.
VOR-ER1002: Errant eFuse read at POR		
Description	**Workaround**	**Comment**
Under certain Power-On ramp rate conditions, the eFuse information may not be correctly read. This can lead to incorrect timing configurations for the memory at high temperatures.	To ensure the eFuse information is read correctly, implement a firmware check on the integrity of the EF_CONFIG register. It should read 0x81400701. If it does not read this value, firmware should reset the device. This will cause the eFuse information to be re-read with the power supplies at valid voltage levels (System reset request (SYSRESETREQ bit in the AIRCR register) will issue a system reset request).	VORAGO Technologies does not plan to implement a design change to address this errata.

15 Revision History

Date	Version	Page Locations	Description
3/4/2016	0.1	1-33	Initial Release Revision of VA10820-only Datasheet
4/1/2016	0.2	31	Added Section 8 'Radiation Hardened Performance'
4/20/2016	1.0	20-26, 37	Updated electrical specifications and address
5/25/2016	1.1	1, 12, 38	Added Contents table (page 1) Changed description of DSTPOR signal in table (page 12). Added Errata Section 12 (page 38).
6/30/16	1.2	13	Updated ceramic 128 LQFP package pinout
9/27/16	1.3	11	Clarified pull-down on DSTPOR
10/17/16	1.4	25	Updated Table 6.5 (DC Current Consumption)
10/31/16	1.5	39	Updated ordering information to reflect part number changes.
11/8/16	1.6	10	Added section 1.8 on eFuse timing register settings. Updated Errata table.
12/22/16	1.7	25	Added post-TID current consumption Section 6.8
1/17/17	1.8	37	Added part marking section 10.1 and minor typo fixes
3/20/17	1.9	37	Corrected ceramic 128 QFP part number in Table 10
3/28/17	2.0	15, 38-40	Added plastic LQFP pinout, mechanical package drawing and new orderable part number for plastic package option
7/7/17	2.1	37	Fixed typos. Added SEFI spec.
10/24/17	2.2	13, 21, 24, 25, 26, 30, 32	Fixed various typos
3/5/18	2.3	39-41	New (simpler) diagram for Plastic QFP package. Updated diagram for Ceramic QFP clarifying trimmed lead dimensions. Added ESD Section.
4/18/18	2.4	38	Added Thermal characteristics table
6/18/18	2.5	13-36	Fixed various typos
8/13/18	2.6	41	Updated ceramic package drawing

The use of this product is subject to the manufacturer's standard terms and conditions available on the manufacturer's website:
https://www.voragotech.com/sites/default/files/Vorago%20Standard%20Terms%20and%20Conditions%20of%20Sale%204_18_2016.pdf

VORAGO Technologies
1501 S MoPac Expressway, Suite #350
Austin, TX 78744
www.voragotech.com
Email: info@voragotech.com
Phone: (512) 633-7992

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for ARM Microcontrollers - MCU ***category:***

Click to view products by Vorago ***manufacturer:***

Other Similar products are found below :

R7FS3A77C2A01CLK#AC1 CP8363AT MB96F119RBPMC-GSE1 MB9BF122LPMC1-G-JNE2 MB9BF122LPMC-G-JNE2 MB9BF128SAPMC-GE2 MB9BF218TBGL-GE1 MB9BF529TBGL-GE1 26-21/R6C-AT1V2B/CT 5962-8506403MQA MB9AF342MAPMC-G-JNE2 MB96F001YBPMC1-GSE1 MB9BF121KPMC-G-JNE2 VA10800-D000003PCA CP8547AT CY9AF156NPMC-G-JNE2 MB9BF104NAPMC-G-JNE1 CY8C4724FNI-S402T ADUCM410BCBZ-RL7 GD32f303RGT6 NHS3152UK/A1Z MK26FN2M0CAC18R EFM32TG230F32-D-QFN64 EFM32TG232F32-D-QFP64 EFM32TG825F32-D-BGA48 MB9AFB44NBBGL-GE1 MB9BF304RBPMC-G-JNE2 MB9BF416RPMC-G-JNE2 MB9AF155MABGL-GE1 MB9BF306RBPMC-G-JNE2 MB9BF618TBGL-GE1 MK20DX64VFT5 MK51DX128CMC7 LPC1754FBD80 STM32F030K6T6TR STM32L073VBT6 AT91SAM7L64-CU ATSAM3N0AA-MU ATSAM3N0CA-CU ATSAM3SD8BA-MU ATSAM4LC2BA-UUR ATSAM4LC4BA-MU ADuC7023BCPZ62I-R7 ATSAM4LS4CA-CFU XMC1302Q040X0200ABXUMA1 ADUCM3027BCPZ-R7 ADUCM3027BCPZ-RL ADUCM3029BCPZ-R7 GD32F450IGH6 GD32F450IIH6