

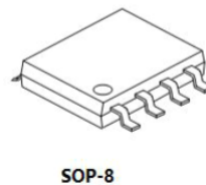
DESCRIPTION

The WD2001 is a monolithic high voltage and high current Darlington transistor arrays. It consists of three NPN darlington pairs that features high-voltage outputs with common-cathode clamp diode for switching inductive loads. The collector-current rating of a single darlington pair is 500mA. The darlington pairs may be paralleled for higher current capability. Applications include relay drivers, hammer drivers, lampdrivers, display drivers(LED gas discharge), line drivers, and logic buffers. The WD2001 has a 2.7k series base resistor for operation directly with TTL or 5V CMOS devices.

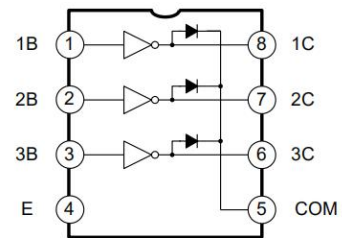
FEATURES

- 500mA rated collector current(Single output)
- High-voltage outputs: 50V
- Inputs compatible with various types of logic.

PACKA



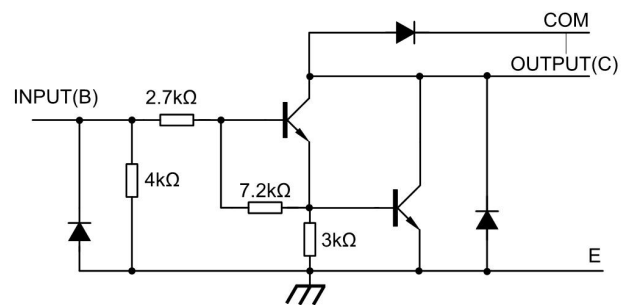
LOGIC DIAGRAM



APPLICATION

- Relay drivers
- Lamp drivers
- Display drivers
- LED gas discharge
- Line drivers
- Logic buffers
- Hammer drivers

SCHEMATIC(EACH DARLINGTON PAIR)



ORDERING INFORMATION

DEVICE	MARKING	PACKAGE
WD2001	WD2001	SOP-8-225-1.27

ABSOLUTE MAXIMUM RATINGS($T_a=25^{\circ}\text{C}$)

Characteristic	Symbol	Value	Unit	
Collector-Emitter Voltage(pin6-8)	V_{CE}	50	V	
COM Voltage(pin5)	V_{com}	50	V	
Input Voltage(pin1-3)	V_I	12	V	
Peak Collector Current	I_{CP}	500	mA	
Total Emitter-terminal	I_{OK}	500	mA	
Maximum peak current of total emitter	I_{ET}	-1	A	
Packaging Thermal Impedance ^{(1) (2) (3)}	DIP-8	I_{ET}	160	°C/W
	SOP-8	θ_{JA}	100	
Junction Temperature ⁽²⁾	T_J	150		
Welding Temperature		260	°C	
Storage Temperature	T_{stg}	-65 ~ +150	°C	

Note: (1) Calculation of Maximum Power Consumption Relation: $P_D=(T_J-T_A)/\theta_{JA}$

(2) T_J Junction temperature indicating circuit operation, T_A Indicates the ambient temperature at which the circuit operates.

(3) Calculating Method of Packaging Thermal Resistance JESD51-7

RECOMMENDED WORKING CONDITIONS($T_a=25^{\circ}\text{C}$)

Characteristic	Symbol	Test Conditions	Min.	Max.	Unit
Output current	I_{OUT}	Continuous output, $T_A=+85^{\circ}\text{C}$		100	mA/ch
Input voltage	V_{IN}		0	12	V
Input voltage(Output ON)	$V_{IN(ON)}$	$I_{out}=400\text{mA}$, $hFE=800$	2.8	12	V
Input voltage(Output OFF)	$V_{IN(OFF)}$		0	0.7	V
Clamp diode reverse voltage	V_R			50	V
Forward Current of Clamp Diode	I_F			350	mA
Operating temperature	T_A		-40	+85	°C
Junction Temperature	T_J		-20	125	°C
Dissipative Power Consumption	SOP8	P_D	$T_A=+25^{\circ}\text{C}$	0.625	W
			$T_A=+85^{\circ}\text{C}$	0.25	
	DIP8	P_D	$T_A=+25^{\circ}\text{C}$	1	
			$T_A=+85^{\circ}\text{C}$	0.4	

Note: 1、 T_A Indicates the ambient temperature at which the circuit operates.

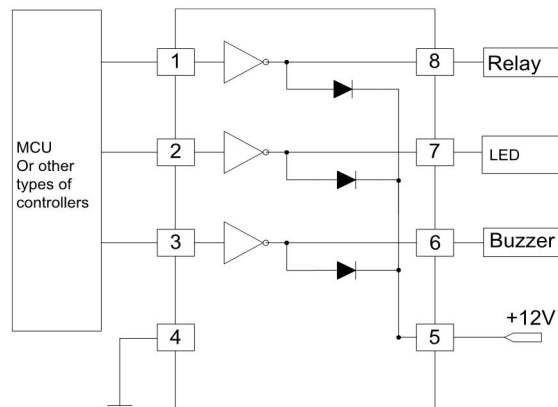
2、Calculation Method of Circuit Power Consumption: $P_D=V_{CE(ON)1} \times I_{C1} + V_{CE(ON)2} \times I_{C2} + V_{CE(ON)3} \times I_{C3} + V_{IN1} \times I_{IN1} + V_{IN2} \times I_{IN2} + V_{IN3} \times I_{IN3}$;

3、In Note 2, $V_{CE(ON)n}$ denotes the conduction voltage drop of the corresponding channel, where $n = 1,2,3$; I_{Cn} denotes the average load current of the corresponding channel, where $n = 1,2,3$; V_{INn} denotes the average value of the signal input high level of the corresponding channel, where $n = 1,2,3$; I_{INn} denotes the average value of the signal input current of the corresponding channel, where $n = 1,2,3$.

ELECTRICAL CHARACTERISTICS (Ta=25°C)

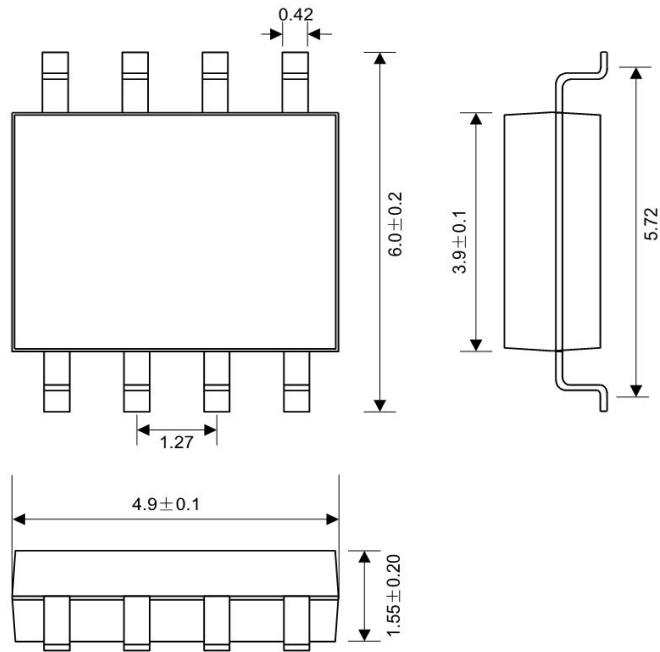
Characteristic	Symbol	Test Conditions	Min	Typ	Max	Units
On-state Input Voltage	$V_{I(ON)}$	$V_{CE}=2V, I_C=200mA$		1.9	2.4	V
		$V_{CE}=2V, I_C=250mA$		2.0	2.7	
		$V_{CE}=2V, I_C=300mA$		2.1	3	
Collector-Emitter Saturation Voltage	$V_{CE(SAT)}$	$V_I=2.4V, I_C=30mA$		0.78		V
		$V_I=2.4V, I_C=60mA$		0.82		
		$V_I=2.4V, I_C=120mA$		0.9		
		$V_I=2.4V, I_C=240mA$		1.1		
		$V_I=2.4V, I_C=3500mA$		1.25		
Input Current	I_I	$V_I=5V, I_C=200mA$		2.7	4	mA
Clamp Forward Voltage	V_F	$I_F=200mA$		1.4	1.6	V
Collector Cutoff Current	I_{CEX}	$V_{CE}=50V, I_I=0$			50	μA
Collector Breakdown Voltage	V_{CE}	$V_{CE}=50V, I_I=0$	50			V
Clamp Reverse Current	I_R	$V_R=50V$			50	μA
Clamp reverse Breakdown voltage	I_R	$V_R=50V$	50			V
Propagation delay time, low-to-high-level output	t_{PLH}	$V_L=12V, R_L=45\Omega$		0.15	1	μs
Propagation delay time, high-to-low-level output	t_{PHL}	$V_L=12V, R_L=45\Omega$		0.15	1	μs

TYPICAL APPLICATION CIRCUIT



PACKAGE DIMENSIONS

SOP-8-225-1.27(unit: mm)



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