

APPROVAL SHEET

MULTILAYER CERAMIC CAPACITORS

Capacitor Arrays Series (10V to 100V)

4 x 0402, 4 x 0603 Sizes

NP0, X7R & Y5V Dielectrics

Halogen Free & RoHS Compliance

*Contents in this sheet are subject to change without prior notice.

Multilayer Ceramic Capacitors

1. INTRODUCTION

WTC middle and high voltage series MLCC is designed by a special internal electrode pattern, which can reduce voltage concentrations by distributing voltage gradients throughout the entire capacitor. This special design also affords increased capacitance values in a given case size and voltage rating.

WTC capacitor arrays are developed to offer designers the opportunity to lower placement costs increase assembly line output through lower component count per board.

2. FEATURES

- a. High density mounting due to mounting space saving.
- b. Mounting cost saving.
- c. Increased throughput.

3. APPLICATIONS

- a. For use as a bypass for digital and analog signal line noise
- b. Computer motherboards and peripherals.
- c. The other common electronic circuits.

4. HOW TO ORDER

<u>Y</u>	<u>4C</u>	<u>3</u>	<u>B</u>	<u>103</u>	<u>K</u>	<u>500</u>	<u>C</u>	<u>I</u>
Series	Cap. Nr.	Termination pitch	Dielectric	Capacitance	Tolerance	Rated voltage	Termination	Packaging
Y=Capacitor array	4C=4xCap	3=0.03" pitch* 2=0.02" pitch*	N=NP0 (COG) B=X7R F=Y5V	Two significant digits followed by no. of zeros. And R is in place of decimal point. eg.: 103=10x10 ³ =10,000pF =10nF	J=±5% K=±10% M=±20% Z=-20/+80%	Two significant digits followed by no. of zeros. And R is in place of decimal point. eg.: 100=10 VDC 160=16 VDC 250=25 VDC 500=50 VDC 101=100 VDC	C=Cu/Ni/Sn	T=7" reeled
Y4C3: 4x0603 (0612) Y4C2: 4x0402 (0508)								

*Size/ Inch (mm) : 4x0402=0508 (1220), 4x0603=0612 (1632)

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5. EXTERNAL DIMENSIONS

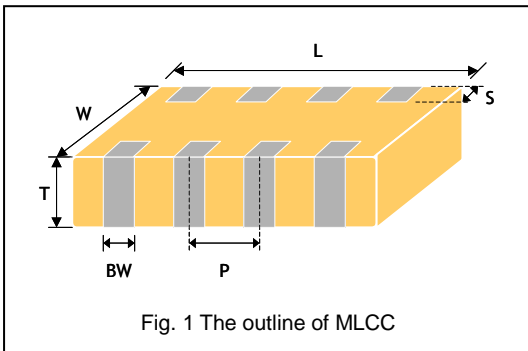


Fig. 1 The outline of MLCC

Size Inch (mm)	L (mm)	W (mm)	T (mm)/Symbol	S (mm)	BW (mm)	P (mm)
4x0402 0508 (1220)	2.00±0.15	1.25±0.15	0.85±0.10 T	0.20±0.10	0.25±0.10	0.50±0.10
4x0603 0612 (1632)	3.20±0.15	1.60±0.15	0.80±0.10 B	0.30±0.20	0.40±0.15	0.80±0.15

Reflow soldering process only.

6. GENERAL ELECTRICAL DATA

	NP0		X7R		Y5V
Size	4x0402	4x0603	4x0402	4x0603	4x0603
Inch (mm)	0508 (1220)	0612 (1632)	0508 (1220)	0612 (1632)	0612 (1632)
Capacitance*	10pF to 270pF	10pF to 470pF	1000pF to 100nF	150pF to 100nF	10nF to 100nF
Capacitance tolerance**	J (±5%), K (±10%)		K (±10%), M (±20%)		Z (-20/+80%)
Rated voltage (WVDC)	25, 50V, 100V		10V, 16V, 25V, 50V	16V, 25V, 50V	16V, 50V
Q/Tan δ*	Cap<30pF: Q≥400+20C Cap≥30pF: Q≥1000		Ur=50V, ≤2.5% Ur=25V&16V, ≤3.5% Ur=10V, ≤5.0%		Ur=50V, ≤5% Ur=16V, ≤7%
Insulation resistance at Ur	≥10GΩ		≥10GΩ or RxC≥500ΩxF whichever is less		
Operating temperature	-55 to +125°C				-25 to +85°C
Capacitance characteristic	±30ppm		±15%		+30/-80%
Termination	Ni/Sn (lead-free termination)				

* Measured at 30~70% related humidity.

NP0: Apply 1.0±0.2Vrms, 1.0MHz±10% at the conditions of 25°C ambient temperature.

X7R: Apply 1.0±0.2Vrms, 1.0kHz±10%, at the conditions of 25°C ambient temperature.

Y5V: Apply 1.0±0.2Vrms, 1.0kHz±10%, at the conditions of 20°C ambient temperature.

** Preconditioning for Class II MLCC: Perform a heat treatment at 150±10°C for 1 hour, then leave in a mbient condition for 24±2 hours before measurement.

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7. CAPACITANCE RANGE

SIZE Inch (mm)	4 x 0402 0508 (1220)								4x0603 0612 (1632)							
	NP0			X7R					NP0			X7R			Y5V	
	25	50	100	10	16	25	50	25	50	100	16	25	50	16	50	
Capacitance	10pF (100)	T	T	T					B	B	B					
	15pF (150)	T	T	T					B	B	B					
	22pF (220)	T	T	T					B	B	B					
	33pF (330)	T	T	T					B	B	B					
	47pF (470)	T	T	T					B	B	B					
	68pF (680)	T	T	T					B	B	B					
	100pF (101)	T	T	T					B	B	B					
	120pF (121)	T	T	T					B	B	B					
	150pF (151)	T	T	T					B	B	B		B	B		
	180pF (181)	T	T	T					B	B	B		B	B		
	220pF (221)	T	T	T					B	B	B		B	B		
	270pF (271)	T	T	T					B	B	B		B	B		
	330pF (331)								B	B	B		B	B		
	470pF (471)								B	B	B		B	B		
	6,80pF (681)												B	B		
	1,000pF (102)				T	T	T	T					B	B		
	1,500pF (152)				T	T	T	T					B	B		
	2,200pF (222)				T	T	T	T					B	B		
	3,300pF (332)				T	T	T	T					B	B		
	4,700pF (472)				T	T	T	T					B	B		
	6,800pF (682)				T	T	T	T					B	B		
	0.010μF (103)				T	T	T	T					B	B	B	
	0.015μF (153)				T	T	T	T				B	B	B	B	
	0.022μF (223)				T	T	T	T				B	B	B	B	
	0.033μF (333)				T	T	T	T				B			B	
0.047μF (473)				T	T	T	T				B			B		
0.068μF (683)				T	T	T	T				B			B		
0.10μF (104)				T	T	T	T				B		B	B		

1. The letter in cell is expressed the symbol of product thickness.

8. PACKAGING DIMENSION AND QUANTITY

SIZE Inch (mm)	Thickness/Symbol (mm)		Paper tape	
			7" reel	13" reel
4x0402 0508 (1220)	0.85±0.10	T	4k	-
4x0603 0612 (1632)	0.80±0.10	B	4k	-

Unit: pieces

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9. RELIABILITY TEST CONDITIONS AND REQUIREMENTS

No.	Item	Test Condition	Requirements																
1.	Visual and Mechanical		<ul style="list-style-type: none"> No remarkable defect. Dimensions to conform to individual specification sheet. 																
2.	Capacitance	Class I: (NP0)	Shall not exceed the limits given in the detailed spec.																
3.	Q/ D.F. (Dissipation Factor)	1.0±0.2Vrms, 1MHz±10% Class II: (X7R, Y5V) 1.0±0.2Vrms, 1kHz±10% *Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .	NP0: Cap≥30pF, Q≥1000; Cap<30pF, Q≥400+20C X7R: Ur=50V, ≤2.5%; Ur=25V&16V, ≤3.5%; Ur=10V, ≤5.0% Y5V: Ur=50V, ≤5%; Ur=16V, ≤7%																
4.	Dielectric Strength	<ul style="list-style-type: none"> To apply 250% rated voltage. Duration: 1 to 5 sec. Charge and discharge current less than 50mA. 	No evidence of damage or flash over during test.																
5.	Insulation Resistance	To apply rated voltage for max. 120 sec. *Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .	≥10GΩ or RxC≥500Ω-F whichever is smaller.																
6.	Temperature Coefficient	With no electrical load. <table border="1"> <thead> <tr> <th>T.C.</th> <th>Operating Temp</th> </tr> </thead> <tbody> <tr> <td>NP0</td> <td>-55~125°C at 25°C</td> </tr> <tr> <td>X7R</td> <td>-55~125°C at 25°C</td> </tr> <tr> <td>Y5V</td> <td>-25~85°C at 20°C</td> </tr> </tbody> </table> *Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .	T.C.	Operating Temp	NP0	-55~125°C at 25°C	X7R	-55~125°C at 25°C	Y5V	-25~85°C at 20°C	<table border="1"> <thead> <tr> <th>T.C.</th> <th>Capacitance Change</th> </tr> </thead> <tbody> <tr> <td>NP0</td> <td>Within ±30ppm/°C</td> </tr> <tr> <td>X7R</td> <td>Within ±15%</td> </tr> <tr> <td>Y5V</td> <td>Within +30%/-80%</td> </tr> </tbody> </table>	T.C.	Capacitance Change	NP0	Within ±30ppm/°C	X7R	Within ±15%	Y5V	Within +30%/-80%
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7.	Adhesive Strength of Termination	<ul style="list-style-type: none"> * Pressurizing force : 5N (≤0603) and 10N (>0603) * Test time: 10±1 sec. 	No remarkable damage or removal of the terminations.																
8.	Vibration Resistance	<ul style="list-style-type: none"> * Vibration frequency: 10~55 Hz/min. * Total amplitude: 1.5mm * Test time: 6 hrs. (Two hrs each in three mutually perpendicular directions.) *Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp . *Cap./DF(Q) Measurement to be made after de-aging at 150°C for 1hr then set for 24±2 hrs at room temp. 	<ul style="list-style-type: none"> No remarkable damage. Cap change and Q/D.F.: To meet initial spec. 																
9.	Solderability	<ul style="list-style-type: none"> * Solder temperature: 235±5°C * Dipping time: 2±0.5 sec. 	95% min. coverage of all metalized area.																
10.	Bending Test	<ul style="list-style-type: none"> * The middle part of substrate shall be pressurized by means of the pressurizing rod at a rate of about 1 mm per second until the deflection becomes 1 mm and then the pressure shall be maintained for 5±1 sec. *Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp . *Measurement to be made after keeping at room temp. for 24±2 hrs. 	<ul style="list-style-type: none"> No remarkable damage. Cap change : NP0: within ±5.0% or ±0.5pF whichever is larger. X7R: within ±12.5% Y5V: within ±30% (This capacitance change means the change of capacitance under specified flexure of substrate from the capacitance measured before the test.) 																
11.	Resistance to Soldering Heat	<ul style="list-style-type: none"> * Solder temperature: 260±5°C * Dipping time: 10±1 sec * Preheating: 120 to 150°C for 1 minute before immerse the capacitor in a eutectic solder. *Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp . *Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr then set for 24±2 hrs at room temp. 	<ul style="list-style-type: none"> No remarkable damage. Cap change: NP0: within ±2.5% or ±0.25pF whichever is larger. X7R: within ±7.5% Y5V: within ±20% Q/D.F., I.R. and dielectric strength: To meet initial requirements. 25% max. leaching on each edge. 																

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No.	Item	Test Condition	Requirements															
12.	Temperature Cycle	<p>* Conduct the five cycles according to the temperatures and time.</p> <table border="1"> <thead> <tr> <th>Step</th> <th>Temp. (°C)</th> <th>Time (min.)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Min. operating temp. +0/-3</td> <td>30±3</td> </tr> <tr> <td>2</td> <td>Room temp.</td> <td>2~3</td> </tr> <tr> <td>3</td> <td>Max. operating temp. +3/-0</td> <td>30±3</td> </tr> <tr> <td>4</td> <td>Room temp.</td> <td>2~3</td> </tr> </tbody> </table> <p>* Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .</p>	Step	Temp. (°C)	Time (min.)	1	Min. operating temp. +0/-3	30±3	2	Room temp.	2~3	3	Max. operating temp. +3/-0	30±3	4	Room temp.	2~3	<p>No remarkable damage.</p> <p>Cap change :</p> <p>NP0: within ±2.5% or ±0.25pF whichever is larger.</p> <p>X7R: within ±7.5%</p> <p>Y5V: within ±20%</p> <p>* Q/D.F., I.R. and dielectric strength: To meet initial requirements.</p>
Step	Temp. (°C)	Time (min.)																
1	Min. operating temp. +0/-3	30±3																
2	Room temp.	2~3																
3	Max. operating temp. +3/-0	30±3																
4	Room temp.	2~3																
13.	Humidity (Damp Heat) Steady State	<p>* Test temp.: 40±2°C</p> <p>* Humidity: 90~95% RH</p> <p>* Test time: 500+24/-0hrs.</p> <p>* Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .</p>	<p>* No remarkable damage.</p> <p>* Cap change: NP0: within ±5.0% or ±0.5pF whichever is larger.</p> <p>X7R: within ±12.5%</p> <p>Y5V: within ±30%</p> <p>* Q/D.F. value:</p> <p>NP0: Cap≥30pF, Q≥350; 10pF≤Cap<30pF, Q≥275+2.5C Cap<10pF; Q≥200+10C</p> <p>X7R: Ur=50V, ≤3%; Ur=25V&16V, ≤5%; Ur=10V, ≤7.5%</p> <p>Y5V: Ur=50V, ≤7.5%; Ur=16V, ≤10%</p> <p>I.R.: ≥1GΩ or RxC≥50Ω-F whichever is smaller.</p>															
14.	Humidity (Damp Heat) Load	<p>* Test temp.: 40±2°C</p> <p>* Humidity: 90~95%RH</p> <p>* Test time: 500+24/-0 hrs.</p> <p>* To apply voltage : rated voltage.</p> <p>* Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .</p>	<p>* No remarkable damage.</p> <p>* Cap change: NP0: within ±7.5% or ±0.75pF whichever is larger.</p> <p>X7R: within ±12.5%</p> <p>Y5V: within ±30%</p> <p>* Q/D.F. value:</p> <p>NP0: Cap≥30pF, Q≥200; Cap<30pF, Q≥100+10/3C</p> <p>X7R: Ur=50V, ≤3%; Ur=25V&16V, ≤5%; Ur=10V, ≤7.5%</p> <p>Y5V: Ur=50V, ≤7.5%; Ur=16V, ≤10%</p> <p>I.R.: ≥500MΩ or RxC≥25Ω-F whichever is smaller.</p>															
15.	High Temperature Load (Endurance)	<p>* Test temp.: NP0, X7R: 125±3°C Y5V: 85±3°C</p> <p>* To apply voltage: 200% of rated voltage.</p> <p>* Test time: 1000+24/-0 hrs.</p> <p>* Before initial measurement (Class II only): To apply de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .</p> <p>* Cap. / DF(Q) / I.R. Measurement to be made after de-aging at 150°C for 1hr then set for 24±2 hrs at room temp .</p>	<p>* No remarkable damage.</p> <p>* Cap change: NP0: within ±3.0% or ±0.3pF whichever is larger.</p> <p>X7R: within ±12.5%</p> <p>Y5V: within ±30%</p> <p>* Q/D.F. value:</p> <p>NP0: Cap≥30pF, Q≥350 10pF≤Cap<30pF, Q≥275+2.5C Cap<10pF, Q≥200+10C</p> <p>X7R: Ur=50V, ≤3%; Ur=25V&16V, ≤5%; Ur=10V, ≤7.5%</p> <p>Y5V: Ur=50V, ≤7.5%; Ur=16V, ≤10%</p> <p>I.R.: ≥1GΩ or RxC≥50Ω-F whichever is smaller.</p>															

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APPENDIXES

▣ Tape & reel dimensions

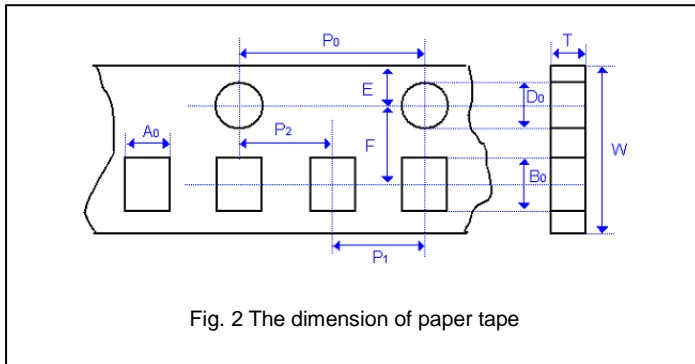


Fig. 2 The dimension of paper tape

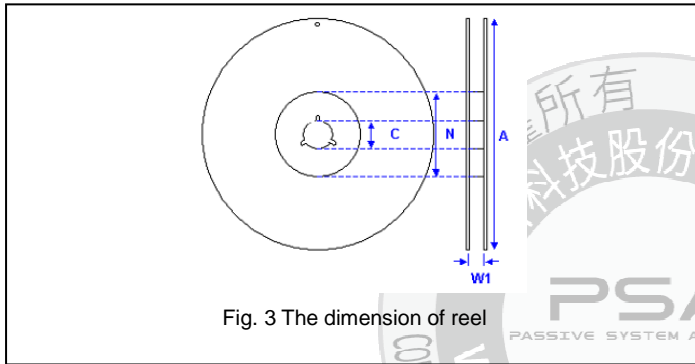
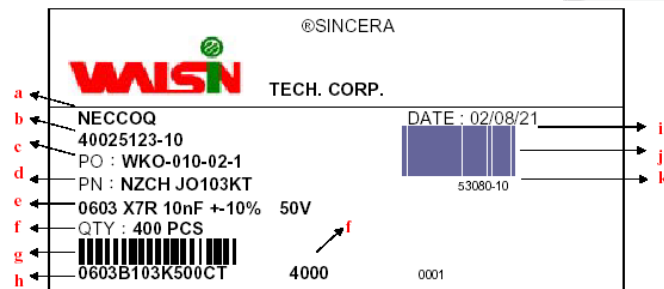


Fig. 3 The dimension of reel

SIZE Inch (mm)	4x0402 0508 (1220)	4x0603 0612 (1632)
Thickness	T	B
A ₀	1.50 +/-0.20	1.90 +/-0.50
B ₀	2.30 +/-0.20	3.50 +/-0.50
T	≤ 1.20	≤ 1.20
K ₀	-	-
W	8.00 +/-0.10	8.00 +/-0.10
P ₀	4.00 +/-0.10	4.00 +/-0.10
10xP ₀	40.00 +/-0.20	40.00 +/-0.20
P ₁	4.00 +/-0.10	4.00 +/-0.10
P ₂	2.00 +/-0.05	2.00 +/-0.05
D ₀	1.55 +/-0.05	1.55 +/-0.05
D ₁	-	-
E	1.75 +/-0.05	1.75 +/-0.05
F	3.50 +/-0.05	3.50 +/-0.05

Reel size	7"
C	13.0+0.5/-0.2
W ₁	8.4+1.5/-0
A	178.0±1.0
N	60.0+1.0/-0

▣ Description of customer label



- a. Customer name
- b. WTC order series and item number
- c. Customer P/O
- d. Customer P/N
- e. Description of product
- f. Quantity
- g. Bar code including quantity & WTC P/N or customer
- h. WTC P/N
- i. Shipping date
- j. Order bar code including series and item numbers
- k. Serial number of label

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Constructions

No.	Name	NP0, X7R, Y5V
①	Ceramic material	BaTiO ₃ based
②	Inner electrode	Ni
③	Termination	Inner layer
④		Middle layer
⑤		Outer layer
		Sn (Matt)

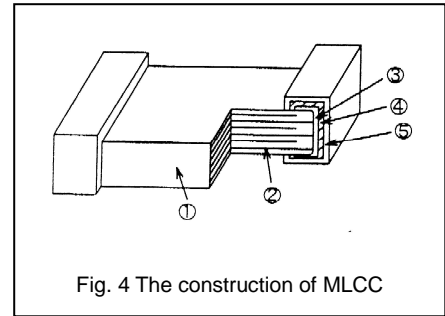


Fig. 4 The construction of MLCC

Storage and handling conditions

- (1) To store products at 5 to 40°C ambient temperature and 20 to 70% related humidity conditions.
- (2) The product is recommended to be used within one year after shipment. Check solderability in case of shelf life extension is needed.

Cautions:

- a. The corrosive gas reacts on the terminal electrodes of capacitors, and results in the poor solderability. Do not store the capacitors in the ambience of corrosive gas (e.g., hydrogen sulfide, sulfur dioxide, chlorine, ammonia gas etc.)
- b. In corrosive atmosphere, solderability might be degraded, and silver migration might occur to cause low reliability.
- c. Due to the dewing by rapid humidity change, or the photochemical change of the terminal electrode by direct sunlight, the solderability and electrical performance may deteriorate. Do not store capacitors under direct sunlight or dewing condition. To store products on the shelf and avoid exposure to moisture.

Recommended soldering conditions

The lead-free termination MLCCs are not only to be used on SMT against lead-free solder paste, but also suitable against lead-containing solder paste. If the optimized solder joint is requested, increasing soldering time, temperature and concentration of N₂ within oven are recommended.

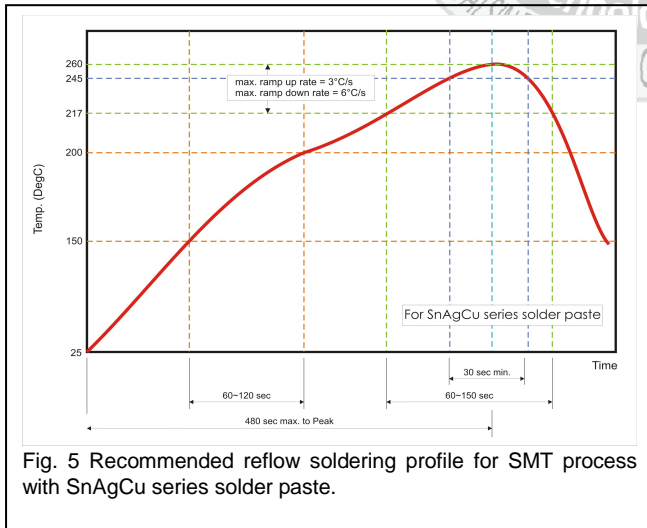


Fig. 5 Recommended reflow soldering profile for SMT process with SnAgCu series solder paste.

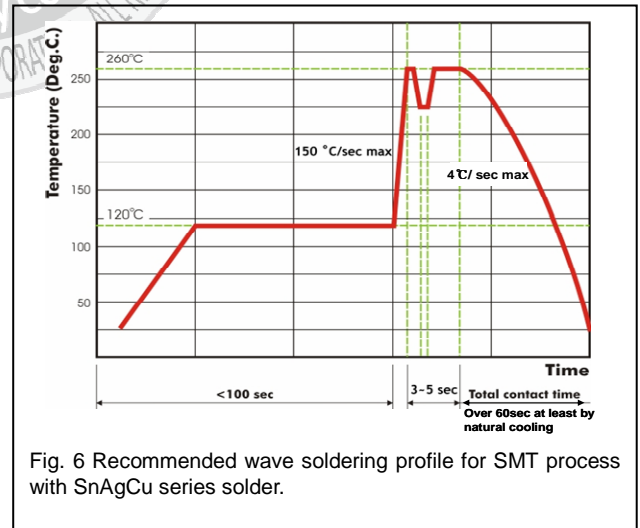


Fig. 6 Recommended wave soldering profile for SMT process with SnAgCu series solder.

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[CA064C103M5RACTU](#) [CA064C223K5RAC7800](#) [CA064C330K5GACTU](#) [CA064C472K5RACTU](#) [LG224Z224MAT2S1](#) [20108D1X103K5E](#)
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[CA0612KRX7R9BB102](#) [CA064C103K5RACTU](#) [CA064C104K4RACTU](#) [C1632C223M5RAC3020](#) [CA0612JRNPO9BN470](#)
[CA0612KRNPO9BN181](#) [CA064C101K5GACTU](#) [CA064C102K5RACTU](#) [20115D1C271K5P](#) [W3A45A151KAT2A](#)
[CKCL22JB1H102M085AA](#) [W3A41C471KAT2A](#) [CKCL22C0G1H221K085AK](#) [CKCM25C0G2A220K060AK](#) [CKCL22CH1H151K085AA](#)
[W3A41A470JAT2A](#)