1.02inch e-Paper

Specifications

Customer	**Standard**
Description	**1.02” E-PAPER DISPLAY**
Model Name	**1.02inch e-Paper**
Date	**2019/12/18**
Revision	**1.0**

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Revision History

Rev.	Issued Date	Revised Contents
1.0	May.28.2019	Preliminary
1.1	Feb.17.2020	Updating

1. General Description

1.1 Over View

The 1.02” active area contains 128×80 pixels, and has1-bit white/black full display capabilities. An integrated circuit contains gate buffer,source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM,and border are supplied with each panel.

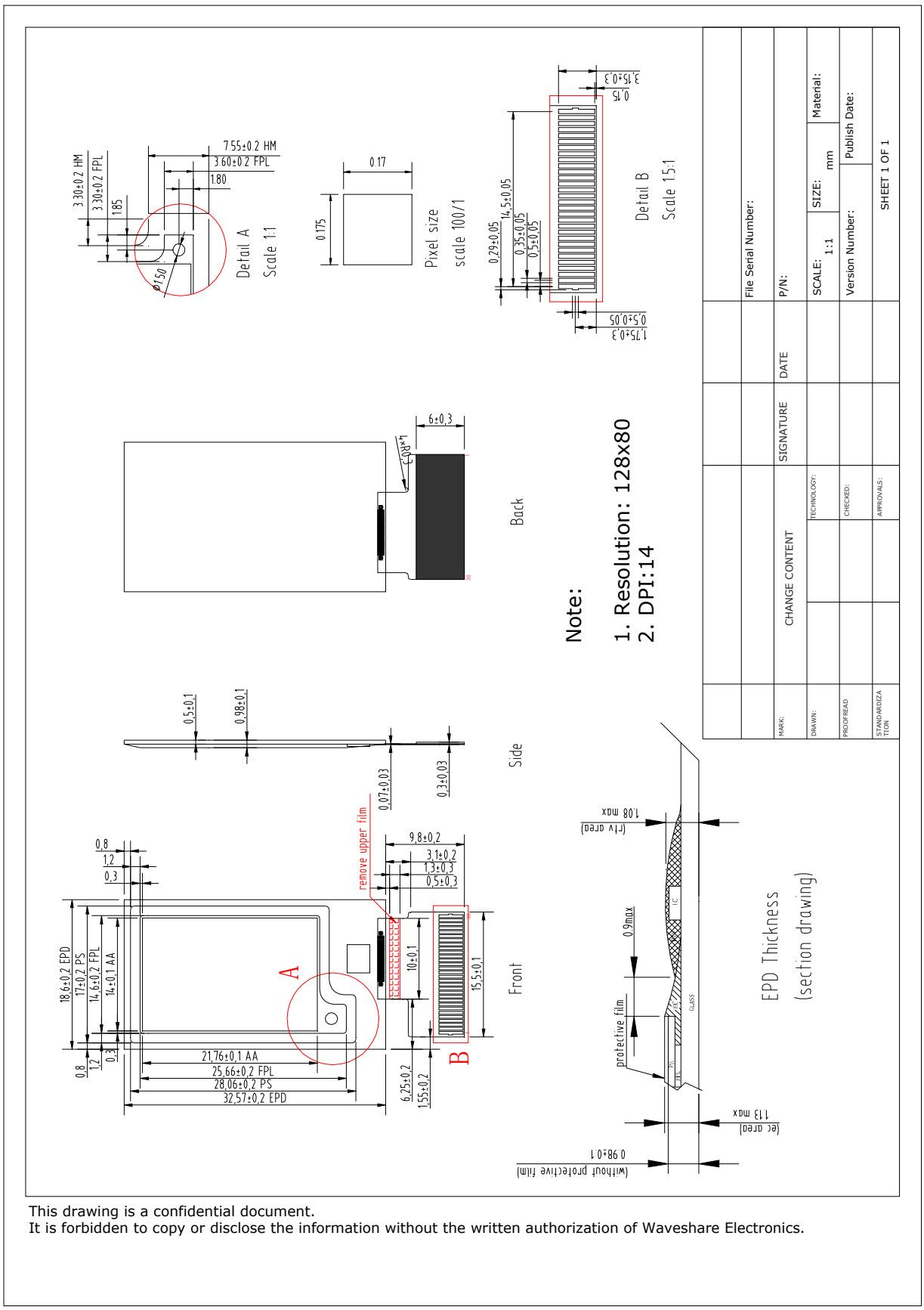
1.2 Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I^2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness TBD um

1.3 Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	1.02	Inch	
Display Resolution	128(H)×80(V)	Pixel	Dpi: 145
Active Area	21.76(H)×14(V)	mm	
Pixel Pitch	0.175×0.17	mm	
Pixel Configuration	Square		
Outline Dimension	32.57(H)×18.6(V) ×0.98(D)	mm	
Weight	1.34±0.05	g	

1.4 Mechanical Drawing of EPD module



1.5 Input/Output Terminals

1.5-1) Pin out List

Pin #	Type	Single	Description	Remark
1	PWR	VPP	OTP Program power	
2	PWR	GND	Digital ground	
3	PWR	VDD	Digital power	
4	I/O	SDA	Serial communication data input/output	
5	I	SCL	Serial communication clock input	
6	I	CS#	Serial communication chip Select	Note 1.5-1
7	I	D/C#	Data /Command control pin	Note 1.5-2
8	I	RES#	Global reset pin	Note 1.5-3
9	O	BUSY	Driver busy flag	Note 1.5-4
10	I	BS1	Bus selection	Note 1.5-5
11	PWR	VDDD	Digital power input	
12	I/O	VDL	Negative source driver voltage	
13	I/O	VDH	Positive source driver voltage	
14	PWR	VGH	Positive gate driver voltage	
15	PWR	VGL	Negative gate driver voltage	
16	PWR	C6N	Capacitor connecting pins on the positive/negative side	
17	PWR	C6P	Capacitor connecting pins on the positive/negative side	
18	PWR	C5N	Capacitor connecting pins on the positive/negative side	
19	PWR	C5P	Capacitor connecting pins on the positive/negative side	
20	PWR	C4N	Capacitor connecting pins on the positive/negative side	
21	PWR	C4P	Capacitor connecting pins on the positive/negative side	
22	PWR	C3N	Capacitor connecting pins on the positive/negative side	
23	PWR	C3P	Capacitor connecting pins on the positive/negative side	
24	PWR	C2N	Capacitor connecting pins on the positive/negative side	
25	PWR	C2P	Capacitor connecting pins on the positive/negative side	
26	PWR	C1N	Capacitor connecting pins on the positive/negative side	

27	PWR	C1P	Capacitor connecting pins on the positive/negative side	
28	PWR	VCOML	Negative pumping voltage for internal use	
29	PWR	VCOMH	Positive pumping voltage for internal use	
30	O	VCOM	VCOM output	

Note 1.5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 1.5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 1.5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 1.5-4: This pin (BUSY) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

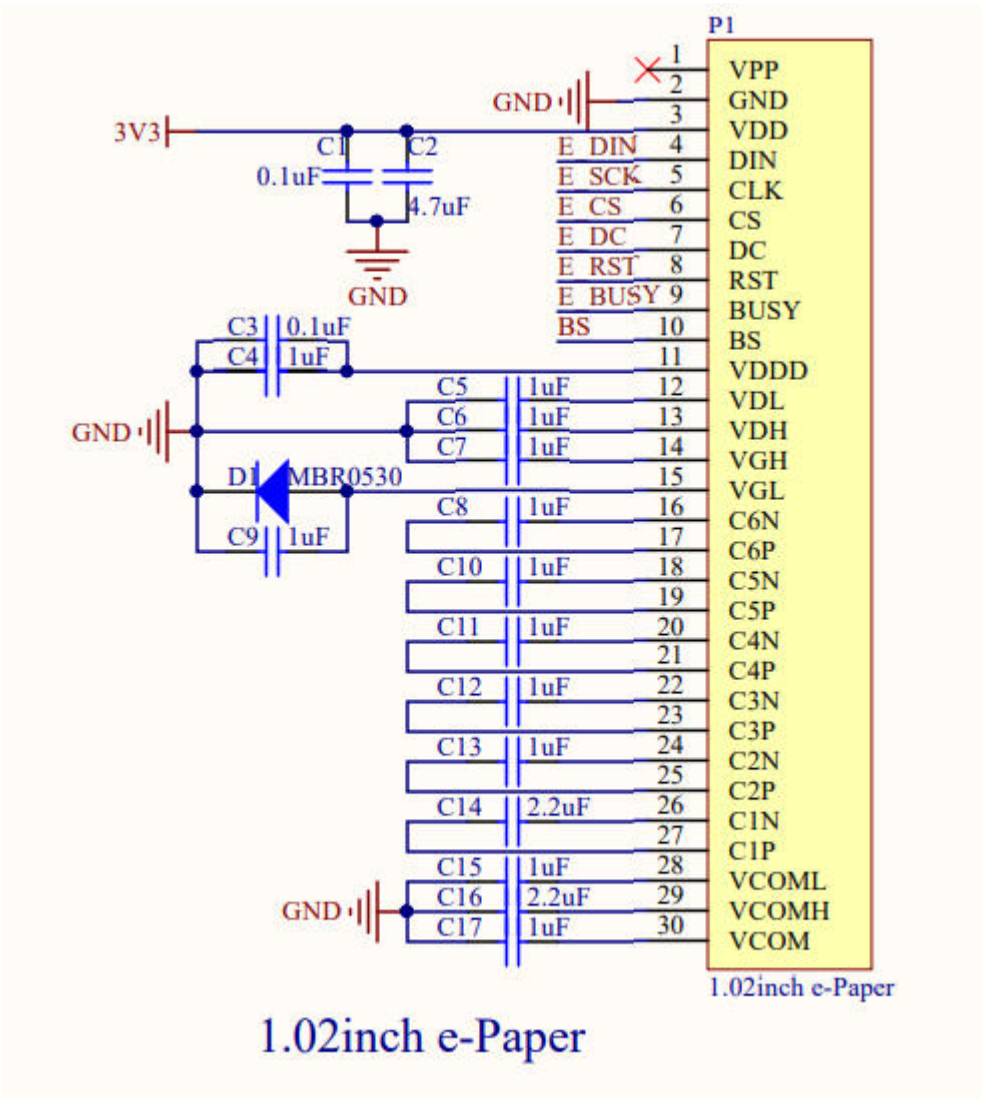
- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 1.5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

1.6 Reference Circuit



2. Environmental

2.1 Handling, Safety and Environmental Requirements

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

Data sheet status	
Product specification	The data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and dose not form part of the specification.	

Product Environmental certification
RoHS

2.2 Reliability test

	TEST	CONDITION	METHOD	REMARK
1	High-Temperature Operation	T =40℃, RH=35% for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
2	Low-Temperature Operation	T = 0℃ for 240 hrs	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Ab.	When experiment finished, the EPD must meet electrical and optical performance standards.
3	High-Temperature Storage	T = +60℃, RH=35% for 168 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the high temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Bp.	When experiment finished, the EPD must meet electrical and optical performance standards.
4	Low-Temperature Storage	T = -25℃ for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the low temperature environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-2Ab	When experiment finished, the EPD must meet electrical and optical performance standards.
5	High Temperature, High-Humidity Operation	T=+40℃, RH=80% for 240 hrs update everyday to return temperature	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-3CA.	When experiment finished, the EPD must meet electrical and optical performance standards.
6	High Temperature, High-Humidity Storage	T=+50℃, RH=80% for 240 hrs Test in white pattern	When the experimental cycle finished, the EPD samples will be taken out from the environmental chamber and set aside for a few minutes. As EPDs return to room temperature, testers will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-3CA.	When experiment finished, the EPD must meet electrical performance standards.

7	Temperature Cycle	[-25℃ 30mins]→ [+60℃,RH=35% 30mins], 50cycles Test in white pattern	1. Samples are put in the Temp & Humid. Environmental Chamber. Temperature cycle starts with -25℃, storage period 30 minutes. After 30 minutes, it needs 30min to let temperature rise to 70℃. After 30min, temperature will be adjusted to 70℃, RH=35% and storage period is 30 minutes. After 30 minutes, it needs 30min to let temperature rise to -25℃. One temperature cycle (2hrs) is complete. 2. Temperature cycle repeats 70 times. 3. When 70 cycles finished, the samples will be taken out from experiment chamber and set aside a few minutes. As EPDs return to room temperature, tests will observe the appearance, and test electrical and optical performance based on standard # IEC 60068-2-14NB.	When experiment finished, the EPD Must meet electrical and optical performance standards.
8	UV exposure Resistance	765 W/m^2 for 168 hrs,40℃	Standard # IEC 60068-2-5 Sa	
9	Electrostatic discharge	Machine model:+/- 250V, 0Ω, 200pF	Standard # IEC61000-4-2	
10	Package Vibration	1.04G,Frequency : 10~500Hz Direction : X,Y,Z Duration:1hours in each direction	Full packed for shipment	
11	Package Drop Impact	Drop from height of 122 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment	

Actual EMC level to be measured on customer application.

Note:

(1) The protective film must be removed before temperature test.

(2) In order to make sure the display module can provide the best display quality, the update should be made after putting the display module in stable temperature environment for 4 hours at 25℃.

3. Electrical Characteristics

3.1 Absolute maximum rating

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	V_{CI}	-0.3 to +6.0	V
Logic Input Voltage	V_{IN}	-0.3 to VCI +2.4	V
Operating Temp. range	T_{OPR}	0 to +50	℃
Storage Temp. range	T_{STG}	-25 to +70	℃
Humidity range	-	40~70	%RH

***Note: Avoid direct sunlight.**

3.2 Panel DC Characteristics

The following specifications apply for: VSS = 0V, VCI = 3.3V, TA = 25℃

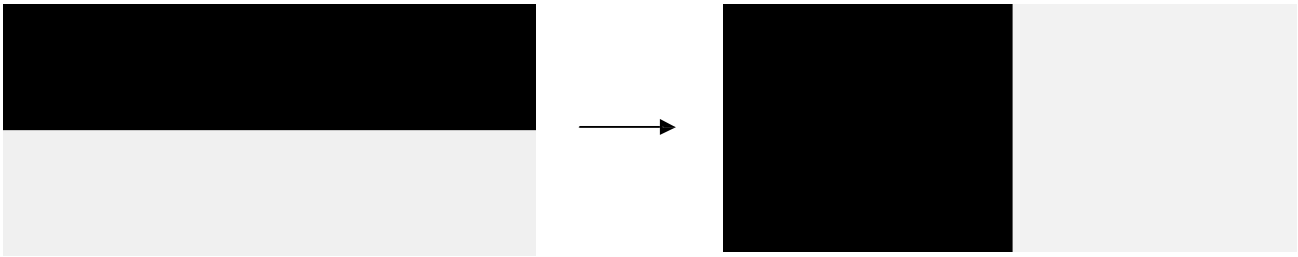
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Single ground	V_{SS}	-	-	0	-	V
Logic Supply Voltage	VCI	-	2.3	3.3	3.6	V
High level input voltage	VIH	Digital input pins	0.7VCI	-	VCI	V
Low level input voltage	VIL	Digital input pins	0	-	0.3VCI	V
High level output voltage	VOH	Digital input pins , IOH= 400uA	VCI-0.4	-	-	V
Low level output voltage	VOL	Digital input pins , IOL= -400uA	0	-	0.4	V
Image update current	I_{UPDATE}	-	1	1.5	2	mA
Standby panel current	Istandby	-	-	-	5	uA
Power panel（update）	P_{UPDATE}	-	-	5	7.5	mW
Standby power panel	P_{STBY}	-	-	-	0.0165	mW
Operating temperature	-	-	0	-	50	℃
Storage temperature	-	-	-25	-	70	℃
Image update Time at 25 ℃	-	-	-	3	5	Sec
Deep sleep mode current	I_{VCI}	DC/DC off No clock No input load Ram data not retain	-	0.2	-	uA
Sleep mode current	I_{VCI}	DC/DC off No clock No input load Ram data retain	-	20	-	uA

- The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.(Note 3-1)
- The standby power is the consumed power when the panel controller is in standby mode.

- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Waveshare.
- Vcom is recommended to be set in the range of assigned value ± 0.1V.

Note 3-1

The Typical power consumption



3.3 Panel AC Characteristics

3.3-1) Oscillator frequency

The following specifications apply for : VSS = 0V, VCI = 3.3V, TA = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator frequency	Fosc	VCI=2.3 to 3.6V	-	1.625	-	MHz

3.3-2) MCU Interface

3.3-2-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDA	SCL	CS#	D/C#	RES#
SPI3	SDA	SCL	CS#	L	RES#

Table 3-1: MCU interface assignment under different bus interface mode

Note 3-2: L is connected to VSS

Note 3-3: H is connected to VCI

3.3-2-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C#, CS#. In SPI mode, D0 acts as SCL, D1 acts as SDA.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 3-2: Control pins of 4-wire Serial Peripheral interface

Note 3-4: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

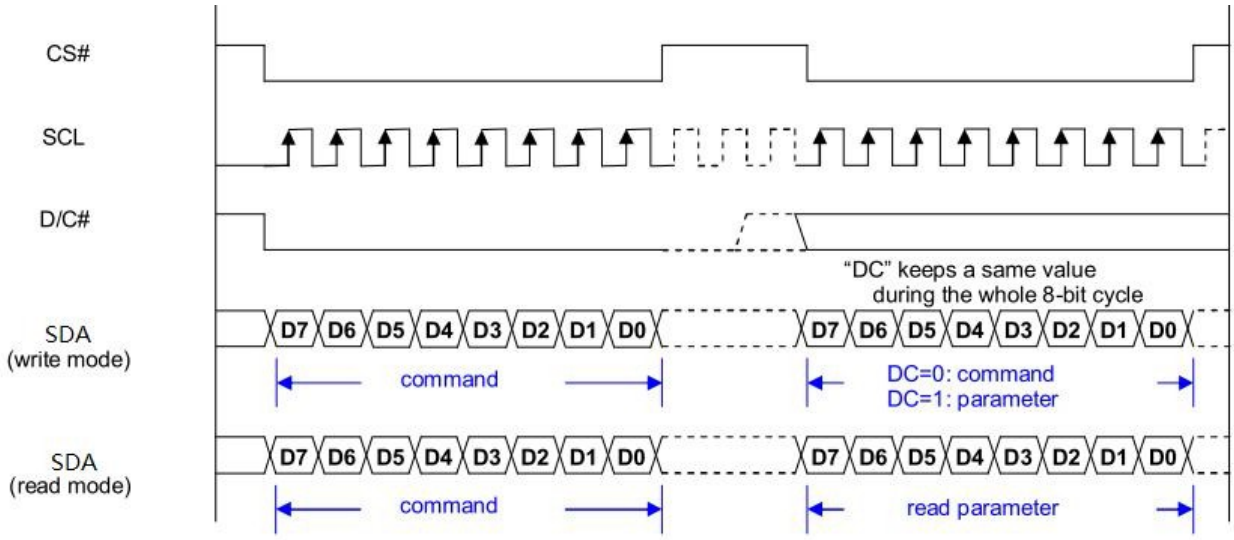


Figure 3-1: Write procedure in 4-wire Serial Peripheral Interface mode

3.3-2-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#.

In 3-wire SPI mode, D0 acts as SCL, D1 acts as SDA, The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Table 3-3: Control pins of 3-wire Serial Peripheral Interface

Note 3-5: ↑stands for rising edge of signal

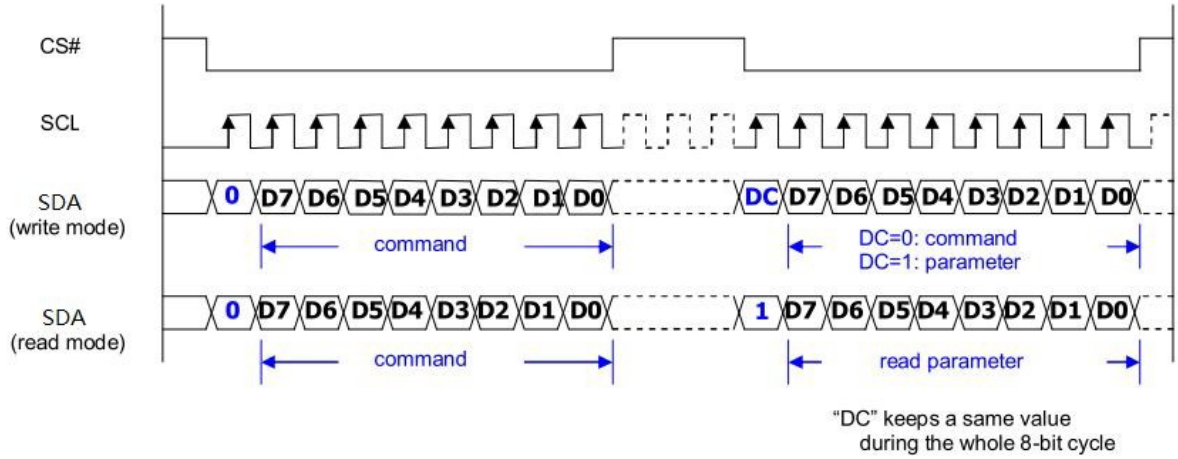
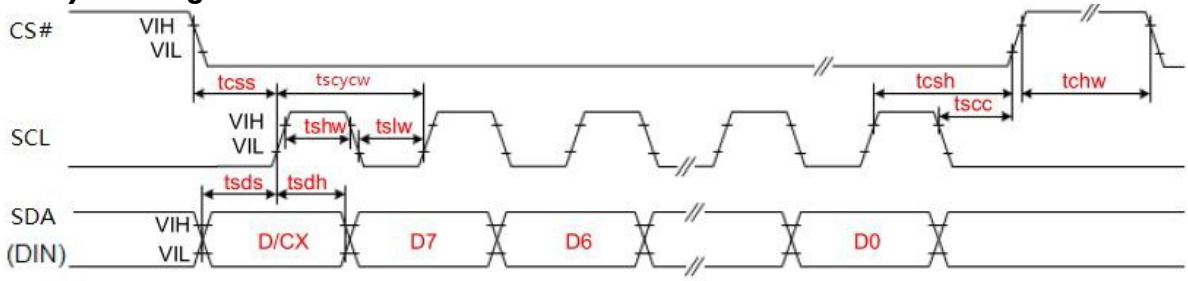
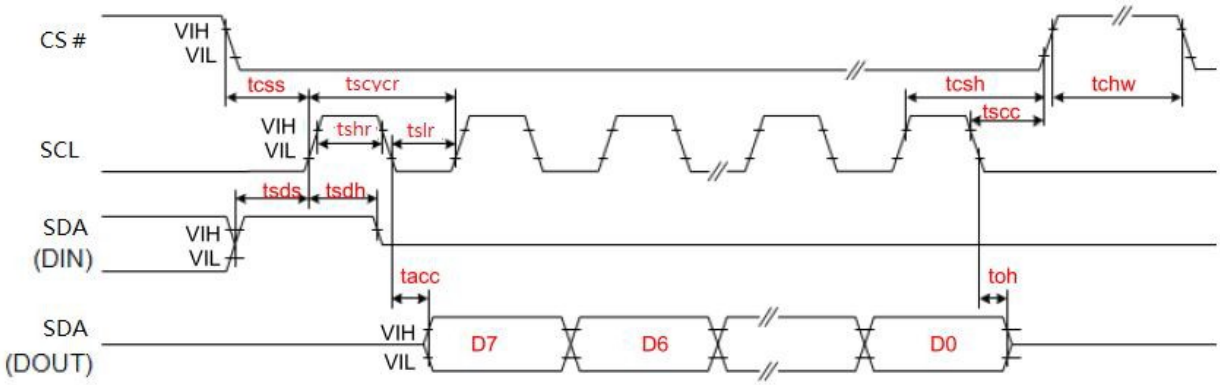


Figure 3-2: Write procedure in 3-wire Serial Peripheral Interface mode

3.3-3) Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw	SCL	Serial clock cycle (write)	100	-	-	ns
tshw		SCL “H” pulse width (write)	35	-	-	ns
tslw		SCL“L” pulse width (write)	35	-	-	ns
tscycr		Serial clock cycle (Read)	150	-	-	ns
tshr		SCL “H” pulse width (Read)	60	-	-	ns
tslr		SCL “L” pulse width (Read)	60	-	-	ns
tsds	SDA (DIN) (DOUT)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc		Access time	-	-	10	ns
toh		Output disable time	15	-	-	ns

3.4 Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	5	7.5	mW	-
Power consumption in standby mode	-	25℃	-	0.0165	mW	-

4. Typical Operating Sequence

TBD

5. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data

D7~D0: -: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	PSR	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	-	#	#	#	#	RES[1:0],REG ,UD, SHL,SHD_N,RST_N	0Fh
2	PWR	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	-	-	-	-	#	#	VDS_EN,VDG_EN	03h
		0	1	-	-	-	-	-	#	#	#	VGHL_LVL[2:0]	00h
		0	1	-	-	#	#	#	#	#	#	VDH_LVL[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDL_LVL[5:0]	26h
3	POF	0	0	0	0	0	0	0	0	1	0		02h
4	PFS	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_ VDS_OFF[1:0]	00h
5	PON	0	0	0	0	0	0	0	1	0	0		04h
6	PMES	0	0	0	0	0	0	0	1	0	1		05h
7	CPSET	0	0	0	0	0	0	0	1	1	0		06h
		0	0	-	-	#	#	#	#	#	#	CPINT[1:0],CPS[1:0],CPFRQ[1:0]	3Fh
8	DSLP	0	0	0	0	0	0	0	1	1	1		07h
		0	0	#	#	#	#	#	#	#	#	Check code=A5H	A5h
9	DTM1	0	0	0	0	0	1	0	0	0	0		10h
		0	1	#	#	#	#	#	#	#	#	Pixel[1:8]	00h
		0	1	..	..	..	..	..	..	..	..	..	...
		0	1	#	#	#	#	#	#	#	#	Pixel [n-7:n]	00h
10	DSP	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	-	-	-	-	-	-	-	Data_flag	00h
11	DRF	0	0	0	0	0	1	0	0	1	0		12h
12	DTM2	0	0	0	0	0	1	0	0	1	1		13h
		0	1	#	#	#	#	#	#	#	#	Pixel[1:8]	00h
		0	1	..	..	..	..	..	..	..	..	..	00h
		0	1	#	#	#	#	#	#	#	#	Pixel [n-7:n]	00h
13	AUTO	0	0	0	0	0	1	0	1	1	1		17h
		0	0	#	#	#	#	#	#	#	#	Check code = A5H/A7H	00h
14	LUTW(43-byte command, structure of bytes 2~7 repeated 7 times)	0	1	0	0	1	0	0	0	1	1		23h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
15	LUTB (43-byte command, sturcture of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	0		24h
16	LUTOPT	0	0	0	0	1	0	1	0	1	0		2Ah
		0	0	#	#	#	#	#	#	#	#	EOPT,STAGE_XON[6:0]	00h
		0	0	-	-	-	#	-	-	#	#	SEL2030,SEL05[1:0]	00h
17	PLL	0	0	0	0	1	1	0	0	0	0		30h
		0	1	-	-	#	#	#	#	#	#	FR[5:0]	13h
18	TSC	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	TS[7:0]	00h
19	TSE	0	0	0	1	0	0	0	0	0	1		41h
		0	1	0	-	-	-	#	#	#	#	TO[3:0]	00h
20	PBC	0	0	0	1	0	0	0	1	0	0		44h
		1	1	#	#	#	#	#	#	#	#	PSTA	00h
21	CDI	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	-	#	#	#	VBD[1:0],DDX[1:0],CDI[2:0]	D2h
22	LPD	0	0	0	1	0	1	0	0	0	1		51h
		1	1	-	-	-	-	-	-	-	#	LPD	01h
23	TCON	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h
24	TRES	0	0	0	1	1	0	0	0	0	1		61h
		0	1	-	#	#	#	#	0	0	0	HRES[6:3]	00h
		0	1	#	#	#	#	#	#	#	#	VRES[7:0]	00h
25	GSST	0	0	0	1	1	0	0	1	0	1		65h
		0	0	-	#	#	#	#	#	#	#	HST[6:3]	00h
		0	0	#	#	#	#	#	#	#	#	VST[7:0]	00h
26	REV	0	0	0	1	1	1	0	0	0	0		70h
		1	1	#	#	#	#	#	#	#	#	LUT_REV0[7:0]	FFh
		1	1	#	#	#	#	#	#	#	#	LUT_REV1[7:0]	FFh
27	FLG	0	0	0	1	1	1	0	0	0	1		71h
		1	1	#	#	-	-	#	#	#	#	CPOK,PTL_flag,data_flag,PON,POF,BUSY_N	02h
28	CRC	1	1	0	1	1	1	0	0	1	0		72h
		1	1	#	#	#	#	#	#	#	#	CRC_MSB[7:0]	FFh
		1	1	#	#	#	#	#	#	#	#	CRC_LSB[7:0]	FFh

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
29	AMV	0	0	1	0	0	0	0	0	0	0		80h
		1	1	-	-	#	#	#	#	#	#	AMVT[1:0],XON,AMVS, AMV,AMVE	10h
30	VV	0	0	1	0	0	0	0	0	0	1		81h
		1	1	-	-	#	#	#	#	#	#	VV[5:0]	00h
31	VDCS	0	0	1	0	0	0	0	0	1	0		82h
		1	1	-	-	#	#	#	#	#	#	VDCS[5:0]	00h
32	PTL	0	0	1	0	0	1	0	0	0	0		90h
		0	1	-	#	#	#	#	0	0	0	HRST[6:3]	00h
		0	1	-	#	#	#	#	1	1	1	HRED[6:3]	07h
		0	1	#	#	#	#	#	#	#	#	VRST[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	VRED [7:0]	00h
		0	1	-	-	-	-	-	-	-	#	PT_SCAN	01h
33	PIN	0	0	1	0	0	1	0	0	0	1		91h
34	POUT	0	0	1	0	0	1	0	0	1	0		92h
35	PGM	0	0	1	0	1	0	0	0	0	0		A0h
36	APG	0	0	1	0	1	0	0	0	0	1		A1h
37	ROTP	0	0	1	0	1	0	0	0	1	0		A2h
		1	1	#	#	#	#	#	#	#	#	Dummy	-
		1	1	#	#	#	#	#	#	#	#	Data of Address = 0	-
		1	1	..	..	..	..	..	..	..	..	..	-
		1	1	#	#	#	#	#	#	#	#	Data of address = n	-
38	CCSET	0	0	1	1	1	0	0	0	0	0		E0h
		0	1	-	-	-	-	-	-	#	#	TSFIX,CCEN	00h
39	PWS	0	0	1	1	1	0	0	0	1	1		E3h
		0	1	#	#	#	#	#	#	#	#	BD_W[3:0],SD_W[3:0]	33h
40	LVSEL	0	0	1	1	1	0	0	1	0	0		E4h
		0	1	-	-	-	-	-	-	#	#	LVD_SEL[1:0]	03h
41	TSSET	0	0	1	1	1	0	0	1	0	1		E5h
		0	1	#	#	#	#	#	#	#	#	TS_SET[7:0]	00h

(1) PSR (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Panel Setting Registers	0	0	0	0	0	0	0	0	0	0
	0	1	RES1	RES0	REG	-	UD	SHL	SHD_N	RST_N

RES[1:0]: Display Resolution setting (source x gate)

00b: 80×160 (source×gate) (Default)

01b: 80×128 (source×gate)

10b: 64×128 (source×gate)

11b: 64×96 (source×gate)

REG_EN: LUT selecti

0: HW LUT. (Default)

1: LUT from registers.

UD: Gate Scan Direction

0: Scan down. First line to last line: Gn-1 → Gn-2 → Gn-3 → ... → G0

1: Scan up. (default) First line to last line: G0 → G1 → G2 → ... → Gn-1

SHL: Source Shift direction

0: Shift left First data to last data: Sn-1 → Sn-2 → Sn-3 → ... → S0

1: Shift right. (default) First data to last data: S0 → S1→ S2 → ... → Sn-1

SHD_N: Charge pump Switch

0: Charge pump OFF.

1: Charge pump ON (Default)

When SHD_N becomes LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF, and Sourcw/Gate/border/ VCOM will be released to floating.

RST_N: Soft Reset

0: Reset. Charge pump OFF, Register data are set to their default values, all drivers will be reset, and all functions will be disabled.
Source/Gate/Border/VCOM will be released to floating.

1: No effect. (Default)

(2) PWR (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Setting	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN
	0	1	-	-	-	-	-	VGHL_LVL[2:0]		
	0	1	-	-	VDH_LVL[5:0]					
	0	1	-	-	VDL_LVL[5:0]					

VDS_EN: Source power selection

0: External source power from VDH/VDL pins

1: Internal voltage generation circuit for both VDH/VDL (Default)

VDG_EN: Gate power selection

0: External gate power from VGH/VGL pins

1: Internal voltage generation circuit for both VGH/VGL (Default)

VGHL_LVL[2:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL voltage level
000(Default)	VGH=16V,VGL= -16V
001	VGH=15V,VGL= -15V
010	VGH=14V,VGL= -14V
011	VGH=13V,VGL= -13V
100	VGH=12V,VGL= -12V
101	VGH=11V,VGL= -11V
others	VGH=11V,VGL= -11V

VDH_LVL[5:0]: Internal VDH power selection.(Default value: 100110b)

VDH	VDH_V	VDH	VDH_V
000000	2.4V	...	...
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

VDL_LVL[5:0]: Internal VDL power selection. (Default value: 100110b)

VDL	VDL_V	VDL	VDL_V
000000	-2.4V	...	...
000001	-2.6V	100110	-10.0V
000010	-2.8V	100111	-10.2V
000011	-3.0V	101000	-10.4V
000100	-3.2V	101001	-10.6V
000101	-3.4V	101010	-10.8V
000110	-3.6V	101011	-11.0V
000111	-3.8V	(others)	-11.0V

(3) POF (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
power OFF	0	0	0	0	0	0	0	0	1	0

After the Power OFF command, the driver will be powered OFF. Refer to the POWER MANAGEMENT section for the sequence. This command will turn off booster, controller, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD turned OFF or Deep Sleep Mode. Source/Gate/Border/VCOM will be released to floating.

(4) PFS (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-

T_VDS_OFF[1:0]: Source to gate power off interval time.

00b: 1frame (Default) 01b: 2 frames 10b: 3frames 11b:4 frame

(5) PON (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power ON	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON. Refer to the POWER MANAGEMENT section for the sequence.

This command will turn on booster, controller, regulators, and temperature sensor will be activated for one-time sensing before enabling booster. When all voltages are ready, the BUSY_N signal will return to high.

(6) PMES (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power ON measure	0	0	0	0	0	0	0	1	0	1

This command enables the internal bandgap, which will be cleared by the next POF.

(7) CPSET (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Charge pump setting	0	0	0	0	0	0	0	1	1	0
	0	0	-	-	CPINT[1:0]		CPS[1:0]		CPFRQ[1:0]	

CPINT[1:0]: Charge pump time internal

00b: 20mS 01b: 30mS 10b: 40mS 11b: 50mS (Default)

CPS[1:0]: Charge pump driving strength

00b: Strength 1 01b: Strength 2 10b: Strength 3 11b: Strength 4 (Default)

CPFRQ[1:0]: Charge pump frequency setting

00b: 1 KHz 01b: 2 KHz 10b: 4 KHz 11b: 8 KHz (Default)

(8) DSLP (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	1	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip will enter Deep Sleep Mode to save power. Deep Sleep Mode will return to Standby Mode by hardware reset. The only one parameter is a check code, the command will be executed if check code = 0xA5.

(9) DTM1 (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	..	..	..	..	..	..	Pixel(n-1)	Pixel(n)

This command starts transmitting “OLD” data and write them into SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) DSP (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Data stop	0	0	0	0	0	1	0	0	0	1
	1	1	Data_flag	-	-	-	-	-	-	-

Check the completeness of data. If data is complete, start to refresh display.

Data_flag: Data flag of receiving user data.

0: Driver didn't receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After "Data Start" (R10h) or "Data Stop" (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY_N signal will become "0".

(11) DRF (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Data refresh	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT. After Display Refresh command, BUSY signal will become "0" and the refreshing of panel starts.

The waiting interval form BUSY_N falling to the first FLG command must be longer than 200uS.

(12) DTM2 (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Data transmission 2	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	..	..	..	..	..	..	Pixel(n-1)	Pixel(n)

This command starts transmitting "NEW" data and write them into SRAM.

(13) Auto (R17H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Auto sequence	0	0	0	0	0	1	0	1	1	1
	0	1	Check code = A5h/A7h							

The command can enable the internal sequence to execute several commands continuously. The successive execution can minimize idle time to aviod unnecessary power consumption and reduce the complexity of the host's control procedure. The sequence contains several operations, including PON, DRF, POF, and DSLP.

AUTO(0x17) + Code(0xA5) = (PON DRF POF)

AUTO(0x17) + Code(0xA7) = (PON DRF POF DSLP)

(14) LUTW (R23H)

This command stores white Look-up Table with 7 groups of data.

(15) LUTB (R24H)

This command builds Look-up Table for Black.

(16) LUOPT (R2AH)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
LUT Option	0	0	0	0	1	0	1	0	1	0
	0	1	EOPT							
	0	1	-	-	-	SEL2030	-	-	SEL05[1:0]	

This command sets XON and the options of LUT.

EOPT: LUT sequence option

STAGE_XON[6:0]:

All Gate ON (Each bit controls one stage, STAGE_XON [0] for stage-1, STAGE_XON [1] for stage-2 …..)

000 0000b: no All-Gate-ON

000 0001b: Stage-1 All-Gate-ON

000 0011b: Stage-1 and Stage-2 All-Gate-ON

: :

SEL05[1:0]: Selection of 0℃ ~ 5℃ LUT

00: 10s 01b: 13.2s 1xb: 15s

SEL2030: Selection of 20℃ ~ 30℃ LUT

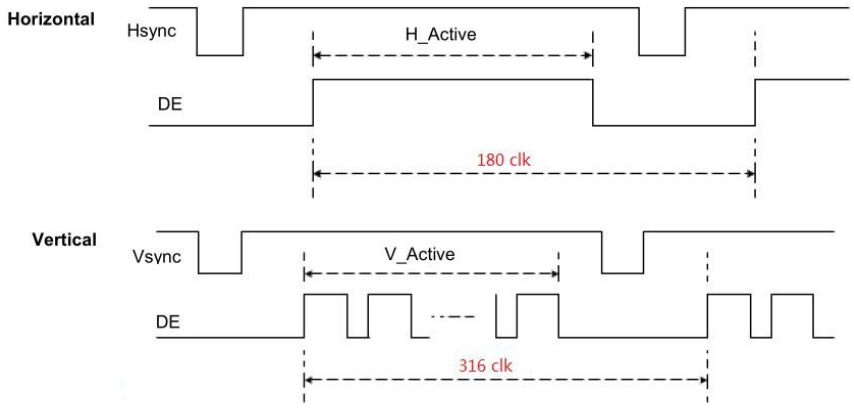
0: 4.8s 1: 8s

(17) PLL (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	FR[5:0]					

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

FR[5:0]	Frame Rate	FR[5:0]	Frame Rate	FR[5:0]	Frame Rate	FR[5:0]	Frame Rate
000000	2.5Hz	001100	32.5Hz	011000	62.5 Hz	100100	92.5 Hz
000001	5.0 Hz	001101	35 Hz	011001	65 Hz	100101	95 Hz
000010	7.5 Hz	001110	37.5 Hz	011010	67.5 Hz	100110	97.5Hz
000011	10.0 Hz	001111	40 Hz	011011	70Hz	100111	100Hz (Default)
000100	12.5 Hz	010000	42.5 Hz	011100	72.5 Hz	others	100 Hz
000101	15 Hz	010001	45 Hz	011101	75 Hz		
000110	17.5Hz	010010	47.5Hz	011110	77.5 Hz		
000111	20 Hz	010011	50 Hz	011111	80 Hz		
001000	22.5 Hz	010100	52.5Hz	100000	82.5 Hz		
001001	25 Hz	010101	55 Hz	100001	85 Hz		
001010	27.5 Hz	010110	57.5Hz	100010	87.5Hz		
001011	30 Hz	010111	60 Hz	100011	90 Hz		



(18) TSC (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature Sensing Command	0	0	0	1	0	0	0	0	0	0
	0	1	TS[7:0]							

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

TS[7:0]/ D[10:3]	Temperature (℃)	TS[7:0]/ D[10:3]	Temperature (℃)	TS[7:0]/ D[10:3]	Temperature (℃)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32
1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40
1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

(19) TSE(R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature sensor Selection	0	0	0	1	0	0	0	0	0	1
	0	1	0	-	-	-	TO[3:0]			

This command selects temperature option.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation	TO[3:0]	Calculation
0000 b	0	1000	-8
0001	1	1001	-7
0010	2	1010	-6
...	...	...	...
0110	6	1110	-2
0111	7	1111	-1

(20) PBC (R44H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Temperature sensor selection	0	0	0	1	0	0	0	0	1	0
	1	1	0	-	-	--	-	-	-	PSTA

This command is used to enable panel check, and to disable after reading result.

PSTA: 0: Panel check fail (panel broken) 1: Panel check pass

(21) CDI(R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Vcom and Data interval setting	0	0	0	1	0	1	0	0	0	0
	0	1	VBD[1:0]		DDX[1:0]		-	CDI[2:0]		

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]:Border data selection

DDX[1:0]:Data polarity

DDX[1:0]	Data (New,OLD)	LUT	DDX[1:0]	Data (New,OLD)	LUT	DDX[0]	VBD[1:0]	LUT
00	00	LUTW	10	00	GND	0	00	VCOM
	01			01	LUTW		01	LUTW
	10	LUTB		10	LUTB		10	LUTB
	11			11	GND		11	Floating
01 (default)	00	LUTB	11	00	GND	1(Default)	00	Floating
	01			01	LUTB		01	LUTB
	10	LUTW		10	LUTW		10	LUTW
	11			11	GND		11(default)	VCOM

CDI[2:0]: VCOM to Data Interval. Interval time setting between VCOM and driver data. Default: 5 Hsync.

CDI[2:0]	Interval
000	7 hsync
001	6 hsync
010	5 hsync (default)
011	4 hsync
100	3 hsync
101	2 hsync
110	2 hsync
111	2 hsync

(22) LPD(R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
LPD	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Interval Low Power Detection Flag

0: Low power input (VDD < 2.5V, selection by LVD_SEL[1:0] in command LVSEL)

1: Normal status (default)

(23) TCON (R60H)

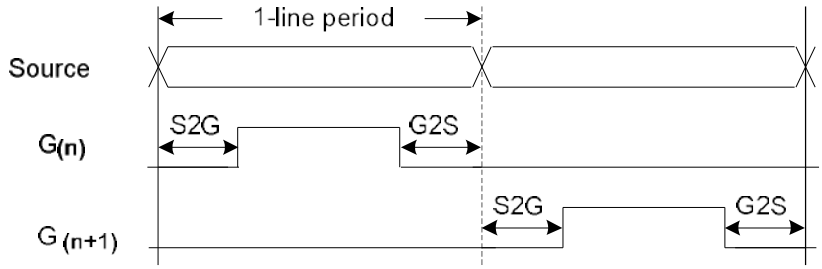
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
TCON	0	0	0	1	1	0	0	0	0	0
	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000b	4		...	...
0001	8		1011	48
0010	12(Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Unit= 2 uS.



(24) Resolution Setting (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	-	HRES[6:3]				0	0	0
	0	1	VRES[7:0]							

HRES[6:3]: Horizontal Resolution (HRES[2:0] is forced to '0')

VRES[7:0]: Vertical Resolution

Active channel calculation (assuming HST[6:0]=0, VST[7:0]=0):

Source: First active source = S0

Last active source = HRES[6:3]*8 - 1

Gate: First active gate = G0

Last active gate = VRES[7:0] - 1

Example: For 64(source) x 128(gate), assuming HST[7:0]=0, VST[8:0]=0, then

Source: First active source = S0

Last active source = S63 (Because HRES[6:3]*8 – 1 = 8*8 - 1 = 63)

Gate: First active gate = G0

Last active gate = G127 (Because VRES[7:0] -1 = 128 - 1= 127)

(25) GSST (R65H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Gate/Source start position	0	0	0	1	1	0	0	1	0	1
	0	1	-	HST[6:3]				0	0	0
	0	1	VST[7:0]							

This command defines resolution start gate/source position.

HST[7:3]: Horizontal Display Start Position (Source)

VST[7:0]: Vertical Display Start Position (Gate)

Example: For 64(Source) x 128(Gate), assuming HST[6:3] = 1 and VST[7:0] = 16, then

Source: First active source = S8 (Because HST[6:0] = HST[6:3]*8 = 1*8 = 8)
Last active source = S71 (Because HST[6:0]+HRES[8:0]–1 = 8+64-1 = 71)
Gate: First active gate = G16 (Because VST[7:0] = 16)
Last active gate = G143 (Because VST[7:0]+VRES[7:0]–1=16+128-1=143)

(26) REV (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read IC revision	0	0	0	1	1	1	0	0	0	0
	1	1	CHIP_REV0[7:0]							
	1	1	CHIP_REV1[7:0]							

This command reads the version of the IC.

(27) FLG (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	CPOK	PTL_flag	-	-	data_ flag	PON	POF	BUSY_N

This command reads the IC status.

CPOK: Charge pump status

PTL_FLAG: Partial display status (high: partial mode)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY_N: Driver busy status (low active)

(28) CRC (R72H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
CRC	1	0	0	1	1	1	0	0	1	0
	1	1	CRC_MSB[7:0]							
	1	1	CRC_LSB[7:0]							

This command reads Cyclic redundancy check(CRC) result.

The calculation only incudes image data (DTM1 & DTM2), and don't containt DTM1(R10h) & DTM2(R13h).

Polynomial = x16+ x12 + x5 + 1, initial vaulte: 16'hFFFF

The result will be reset after this command.

CRC_MSB[7:0]: Most significant bits of CRC result

CRC_LSB[7:0]: Lease significant bits of CRC result

(29) AMV (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

This command reads the IC status.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s 01b: 5s (Default)

10b: 8s 11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)

1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)

1: Get Vcom value in analog signal. (External analog to digital converter)

AMVE: Auto Measure Vcom Enable (/Disable)

0: No effect

1: Trigger auto Vcom sensing.

(30) VV (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
VV	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the Vcom value.

VV[5:0]: Vcom Value Output

VV[5:0]	Vcom value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(31) VDCS (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Vcom DC setting	0	0	1	0	0	0	0	0	1	0
	1	1	-	-	VDCS[5:0]					

This command sets VCOM_DC value

VDCS[5:0]: VCOM_DC Setting

VDCS[5:0]	Vcom value
00 0000b	-0.10 V (default)
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V
others	-3.00 V

(32) PTL (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
PTL	0	0	1	0	0	1	0	0	0	0
	1	1	-	HRST[6:3]				0	0	0
	0	1	-	HRED[6:3]				1	1	1
	1	1	VRST[7:0]							
	0	1	VRED[7:0]							
	1	1	-	-	-	-	-	-	-	PT_SCAN

This command sets partial window.

HRST[6:3]: Horizontal start channel bank. (value 0h~9h)

HRED[6:3]: Horizontal end channel bank. (value 0h~9h).

HRED must be greater than HRST.

VRST[7:0]: Vertical start line. (value 00h~9Fh)

VRED[7:0]: Vertical end line. (value 00h~9Fh). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (default)

(33) PIN (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	0	1

This command makes the display enter partial mode.

(34) POUT (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial OUT	0	0	1	0	0	1	0	0	1	0

This command makes the display exit partial mode and enter normal mode.

(35) Program Mode(PGM) (RA0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enter Program Mode	0	0	1	0	1	0	0	0	0	0

After this command is issued, the chip would enter the program mode.

After the programming procedure completed, a hardware reset is necessary for leaving program mode.

(36) Active Program (APG) (RA1H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Active Program OTP	0	0	1	0	1	0	0	0	0	1

After this command is transmitted, the programming state machine would be activated.

The BUSY_N flag would fall to 0 until the programming is completed.

(37) Read OTP Data (ROTP) (RA2H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read OTP data for check	0	0	1	0	1	0	0	0	1	0
	1	1	Dummy							
	1	1	The data of address 0x000 in the OTP							
	1	1	The data of address 0x001 in the OTP							
	1	1	..							
	1	1	The data of address (n-1) in the OTP							
	1	1	The data of address (n) in the OTP							

The command is used for reading the content of OTP for checking the data of programming.

The value of (n) is depending on the amount of programmed data, tha max address = 0x7FF.

(38) Cascade setting (CCSET) (RE0H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set cascade option	0	0	1	0	1	0	0	0	1	0
	0	1	-	-	-	-	-	-	TSFIX	CCEN

CCEN: Output clock enable/disable.

0: Output 0V at CL pin. (default)

1: Output clock at CL pin for slave chip.

TSFIX: Let the value of slave's temperature is same as the master's.

0: Temperature value is defined by internal temperature sensor / external LM75. (default)

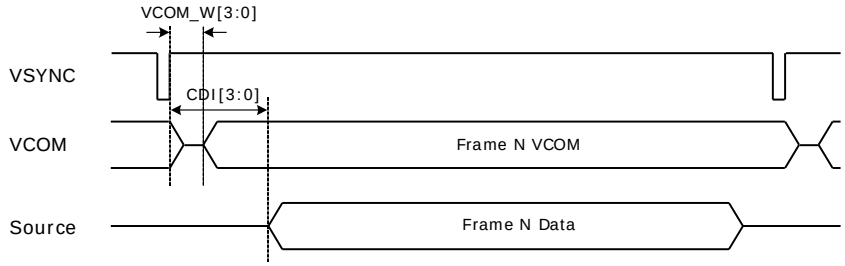
1: Temperature value is defined by TS_SET[7:0] registers.

(39) Power Saving (PWS) (RE3H)

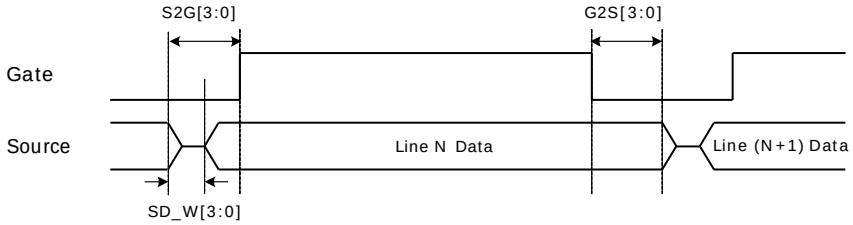
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Saving for	0	0	1	1	1	0	0	0	1	1
Vcom &Source	0	1	VCOM_W[3:0]				SD_W[3:0]			

This command is set for saving power during refreshing period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 2 uS)



(40) LPD voltage select (LVSEL) (RE4H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Select LPD voltage	0	0	1	1	1	0	0	1	0	0
	0	1	-	-	-	-	-	-	LVD_SEL[1:0]	

LPD_SEL[1:0]: Low Power Voltage selection

LVD_SEL[1:0]	LPD voltage threshold
00	＜2.2V
01	＜2.3V
10	＜2.4V
11	＜2.5V (default)

(41) Force temperature (TSSET) (RE5H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Force temperature value for cascade	0	0	1	1	1	0	0	1	0	1
	0	1	TS_SET[7:0]							

This command is used for cascade to fix the temperature value of master and slave chip.

6. Optical characteristics

6.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYPE	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 6-1
Gn	2Grey Level	-	-	DS＋(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	indoor	8		-	-	-
Panel's life		0℃~50℃		1000000 times or 5 years			Note 6-2

WS : White state, DS : Dark state

Gray state from Dark to White : DS、WS

m : 2

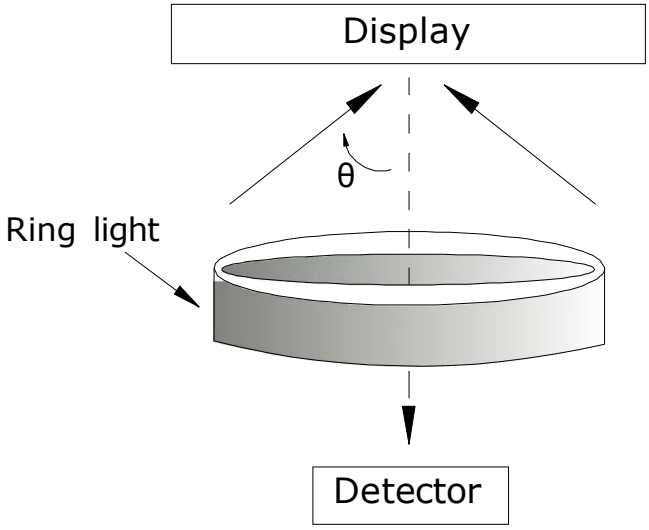
Note 6-1: Luminance meter: Eye – One Pro Spectrophotometer

Note 6-2: Panel life will not guaranteed when work in temperature below 0 degree or above 50 degree. Each update interval time should be minimum at 180 seconds.

6.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (R1) and the reflectance in a dark area (Rd)() : R1: white reflectance Rd: dark reflectance

CR = R1/Rd

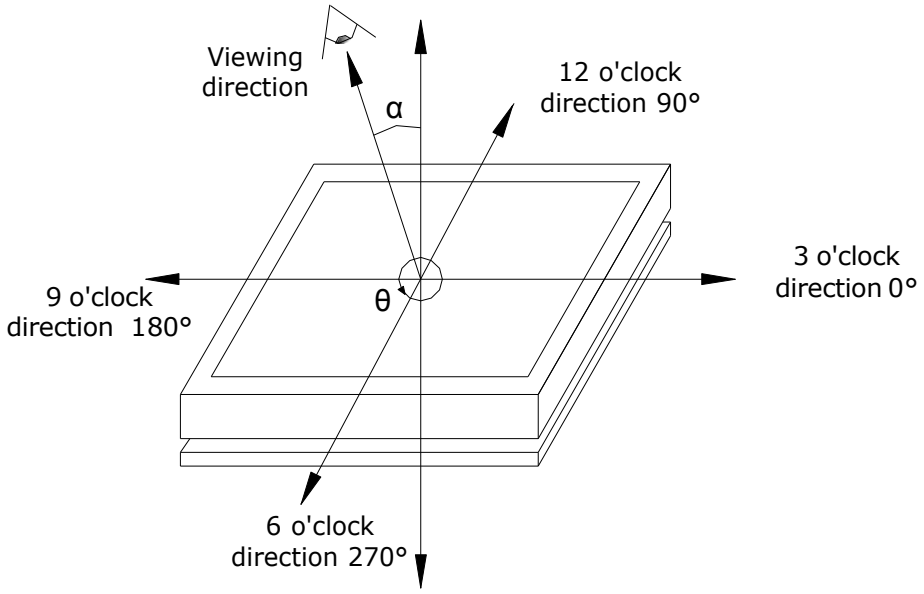


6.3 Reflection Ratio

The reflection ratio is expressed as :

R = Reflectance Factor $_{white\ board}$ x (L_{center} / $L_{white\ board}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1) . $L_{white\ board}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



6.4 Bi-stability

The Bi-stability standard as follows:

Bi-stability	Result		
24 hours Luminance drift		AVG	MAX
	White state △L*	-	3
	Black state △L*	-	3

7. Point and line standard

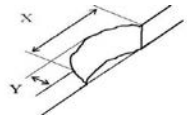
Shipment Inspection Standard

Part-A：Active area　　Part-B：Border area

Equipment：Electrical test fixture, Point gauge

Outline dimension：

32.57(H)×18.6(V) ×0.3(D)　　Unit：mm

<table>
<tr><td rowspan="2">Environment</td><td>Temperature</td><td>Humidity</td><td>Illuminance</td><td>Distance</td><td>Time</td><td>Angle</td></tr>
<tr><td>23±2℃</td><td>55± 5%RH</td><td>1200～ 1500Lux</td><td>300 mm</td><td>35 Sec</td><td></td></tr>
<tr><td>Name</td><td>Causes</td><td colspan="3">Spot size</td><td>Part-A</td><td>Part-B</td></tr>
<tr><td rowspan="3">Spot</td><td rowspan="3">B/W spot in glass or protection sheet, foreign mat. Pin hole</td><td colspan="3">D ≤ 0.15mm</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td colspan="3">0.15mm ＜ D ≤ 0.25mm</td><td>2</td></tr>
<tr><td colspan="3">0.25mm ＜ D</td><td>0</td></tr>
<tr><td rowspan="4">Scratch or line defect</td><td rowspan="4">Scratch on glass or Scratch on FPL or Particle is Protection sheet.</td><td>Length</td><td colspan="2">Width</td><td>Part-A</td><td rowspan="4">Ignore</td></tr>
<tr><td>L ≤0.5mm</td><td colspan="2">W≤0.06 mm</td><td>Ignore</td></tr>
<tr><td>0.5 mm<L≤1.0mm</td><td colspan="2">0.06 mm<W≤0.1mm</td><td>2</td></tr>
<tr><td>1.0 mm < L</td><td colspan="2">0.1mm < W</td><td>0</td></tr>
<tr><td rowspan="3">Air bubble</td><td rowspan="3">Air bubble</td><td colspan="3">D1, D2 ≤ 0.15 mm</td><td>Ignore</td><td rowspan="3">Ignore</td></tr>
<tr><td colspan="3">0.15 mm < D1,D2 ≤ 0.3mm</td><td>2</td></tr>
<tr><td colspan="3">0.3mm < D1, D2</td><td>0</td></tr>
<tr><td rowspan="2">Side Fragment</td><td colspan="6">  </td></tr>
<tr><td colspan="6">X≤3mm，Y≤1mm & display is ok, Ignore</td></tr>
</table>

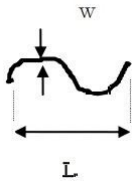
Remarks: Spot define: That only can be seen under WS or DS defects.

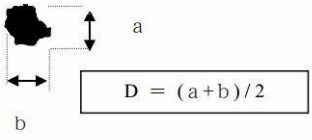
Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded. Here is definition of the “Spot” and “Scratch or line defect”.

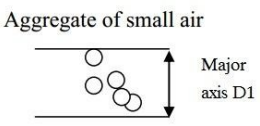
Spot: W > 1/4L　　Scratch or line defect: W ≤1/4L

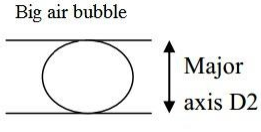
Definition for L/W and D (major axis)

FPC bonding area pad doesn’t allowed visual inspection.



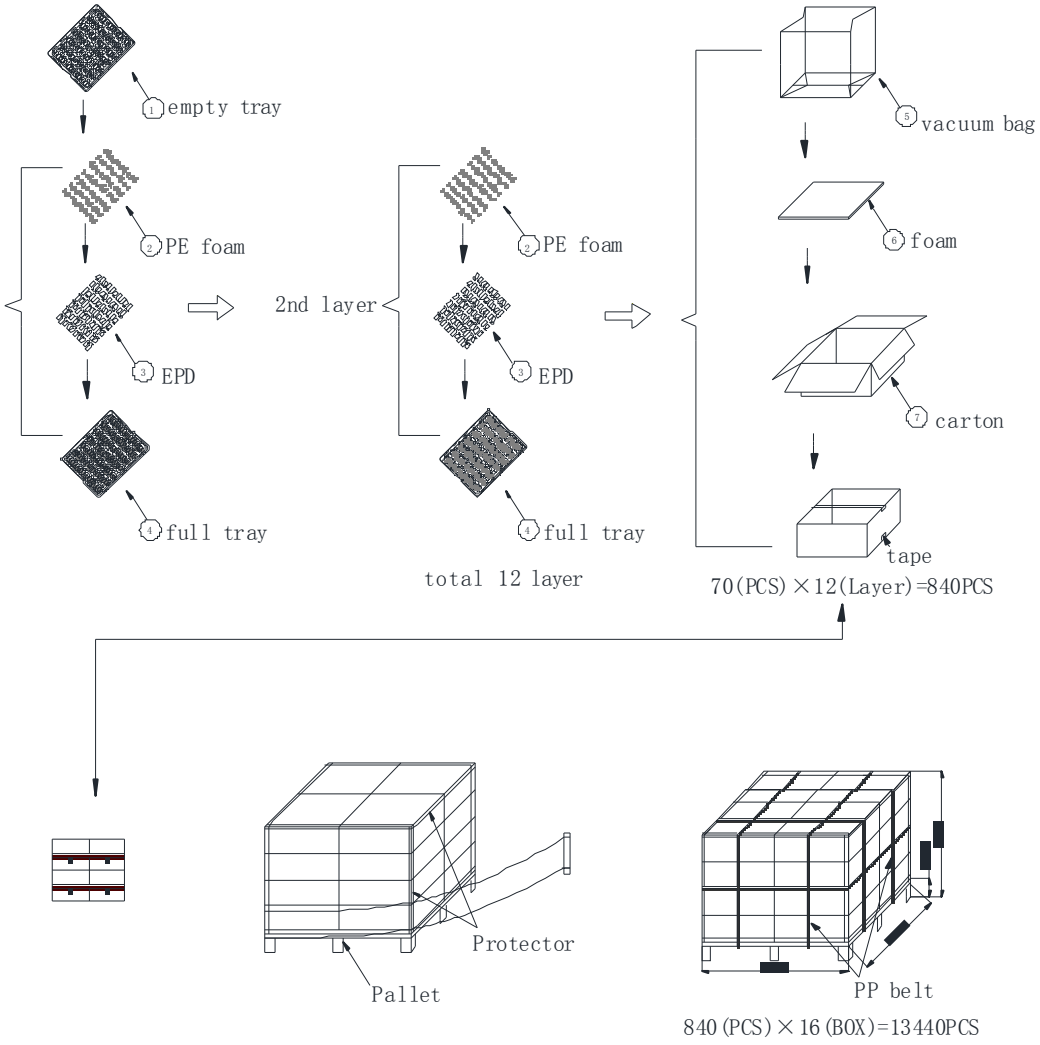






Note: AQL = 0.4

8. Packing


empty tray
PE foam
EPD
full tray
2nd layer
PE foam
EPD
full tray
total 12 layer
vacuum bag
foam
carton
tape
70(PCS)×12(Layer)=840PCS
Protector
Pallet
PP belt
840(PCS)×16(BOX)=13440PCS

9. Precautions

(1) Do not apply pressure to the EPD panel in order to prevent damaging it.

(2) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(3) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(4) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(5) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as “Ghosting” or “Image Sticking” may occur. It is recommended to refreshed the ESL /EPD Tag every 24 hours in use case. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue

(6) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel’s performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time.

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