

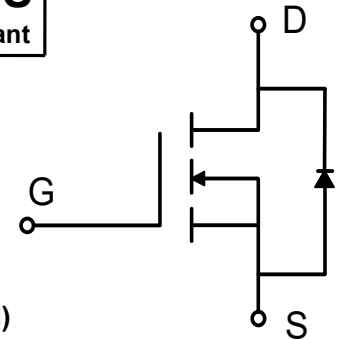
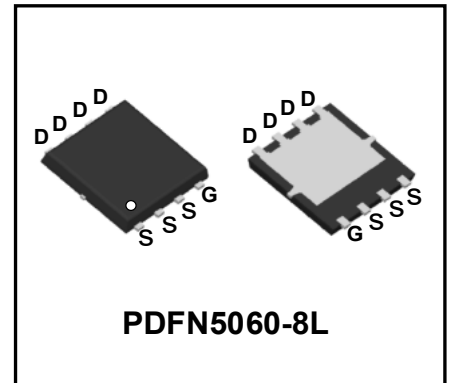
40V N-Channel Enhancement Mode Power MOSFET

Description

WMB100N04TS uses advanced power trench technology that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Features

- $V_{DS} = 40V$, $I_D = 125A$
 $R_{DS(on)} < 3.6m\Omega @ V_{GS} = 10V$
 $R_{DS(on)} < 4.6m\Omega @ V_{GS} = 4.5V$
- High Density Cell Design
- Low $R_{DS(on)}$
- 100% EAS Guaranteed



Applications

- Power Management Switches
- DC/DC Converter

Absolute Maximum Ratings ($T_A = 25^\circ C$, unless otherwise noted)

Parameter		Symbol	Value	Unit
Drain-Source Voltage		V_{DS}	40	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current	$T_C = 25^\circ C$	I_D	125	A
	$T_C = 100^\circ C$		79	
Pulsed Drain Current ¹		I_{DM}	500	A
Single Pulse Avalanche Energy ²		EAS	135.2	mJ
Total Power Dissipation	$T_C = 25^\circ C$	P_D	96	W
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction-to-Ambient ³	$R_{\theta JA}$	49	$^\circ C/W$
Thermal Resistance from Junction-to-Case	$R_{\theta JC}$	1.3	$^\circ C/W$

Electrical Characteristics ($T_J = 25^\circ\text{C}$, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static Characteristics							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	40	-	-	V	
Gate-body Leakage current	I_{GSS}	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA	
Zero Gate Voltage Drain Current	$T_J = 25^\circ\text{C}$	I_{DSS}	$V_{DS} = 40V, V_{GS} = 0V$	-	-	1	μA
	$T_J = 100^\circ\text{C}$			-	-	100	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.6	2.5	V	
Drain-Source On-Resistance ⁴	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 20A$	-	2.6	3.6	m Ω	
		$V_{GS} = 4.5V, I_D = 15A$	-	3.4	4.6		
Forward Transconductance ⁴	g_{fs}	$V_{DS} = 10V, I_D = 20A$	-	100	-	S	
Dynamic Characteristics⁵							
Input Capacitance	C_{iss}	$V_{DS} = 20V, V_{GS} = 0V, f = 1\text{MHz}$	-	5210	-	pF	
Output Capacitance	C_{oss}		-	430	-		
Reverse Transfer Capacitance	C_{rss}		-	325	-		
Gate Resistance	R_G	$f = 1\text{MHz}$	-	1.1	-	Ω	
Switching Characteristics⁵							
Total Gate Charge	Q_g	$V_{GS} = 10V, V_{DS} = 20V, I_D = 20A$	-	95	-	nC	
Gate-Source Charge	Q_{gs}		-	9.5	-		
Gate-Drain Charge	Q_{gd}		-	18.5	-		
Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 10V, V_{DD} = 20V, R_G = 3\Omega, I_D = 20A$	-	15.8	-	ns	
Rise Time	t_r		-	30.5	-		
Turn-Off Delay Time	$t_{d(off)}$		-	150	-		
Fall Time	t_f		-	82	-		
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 20A, di/dt = 100A/\mu s$	-	32	-	ns	
Body Diode Reverse Recovery Charge	Q_{rr}		-	19.2	-	nC	
Drain-Source Body Diode Characteristics							
Diode Forward Voltage ⁴	V_{SD}	$I_S = 20A, V_{GS} = 0V$	-	-	1.2	V	
Continuous Source Current	I_S	$T_C = 25^\circ\text{C}$	-	-	125	A	

Notes:

1. Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
2. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.1\text{mH}, I_{AS} = 52A$.
3. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, The value in any given application depends on the user's specific board design.
4. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
5. This value is guaranteed by design hence it is not included in the production test.

Typical Characteristics

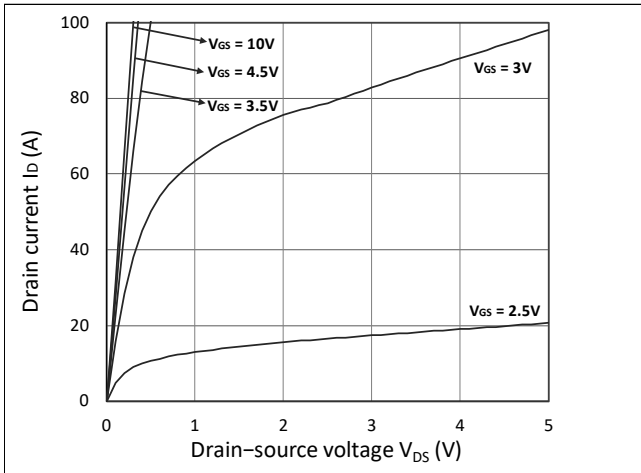


Figure 1. Output Characteristics

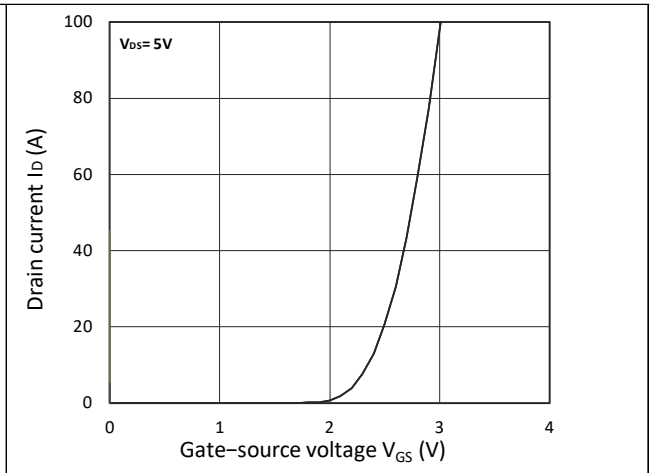


Figure 2. Transfer Characteristics

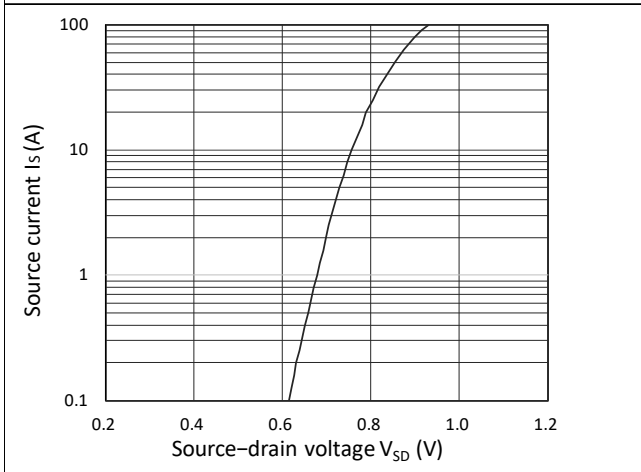


Figure 3. Forward Characteristics of Reverse

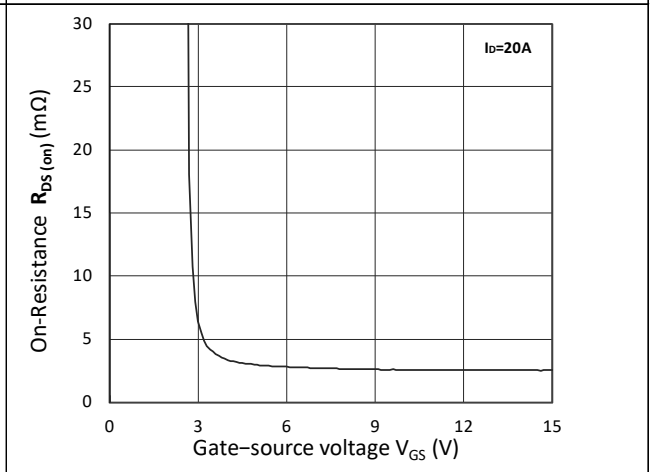


Figure 4. $R_{DS(on)}$ vs. V_{GS}

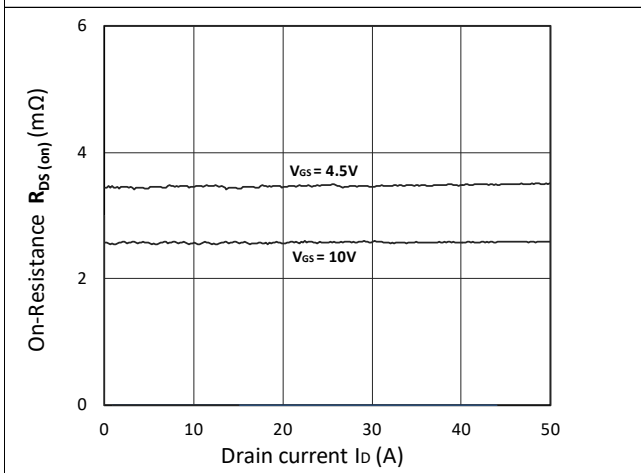


Figure 5. $R_{DS(on)}$ vs. I_D

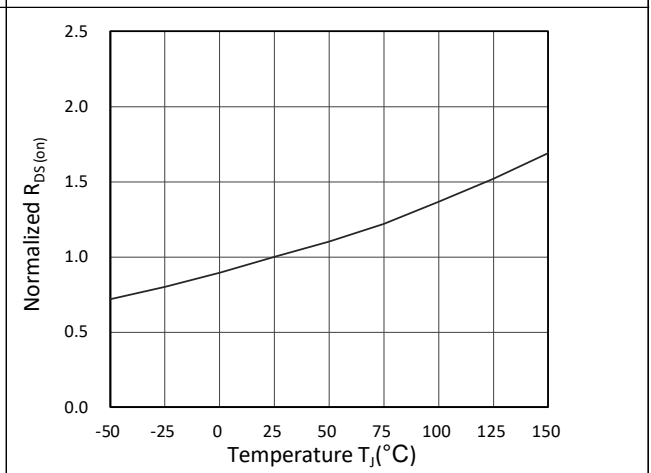


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

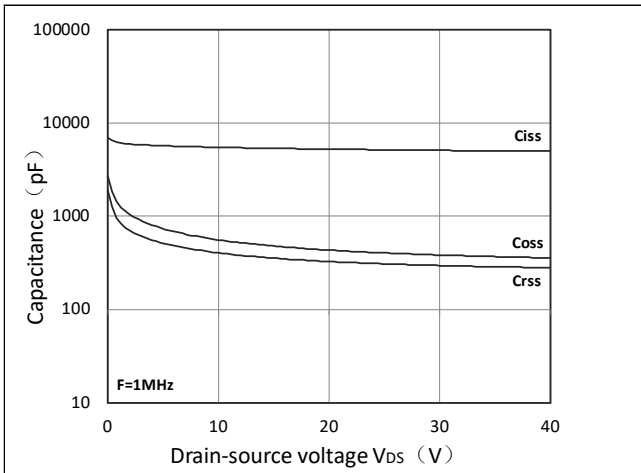


Figure 7. Capacitance Characteristics

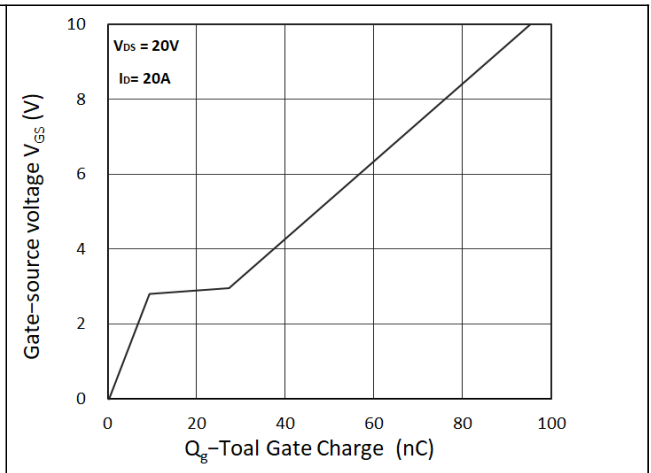


Figure 8. Gate Charge Characteristics

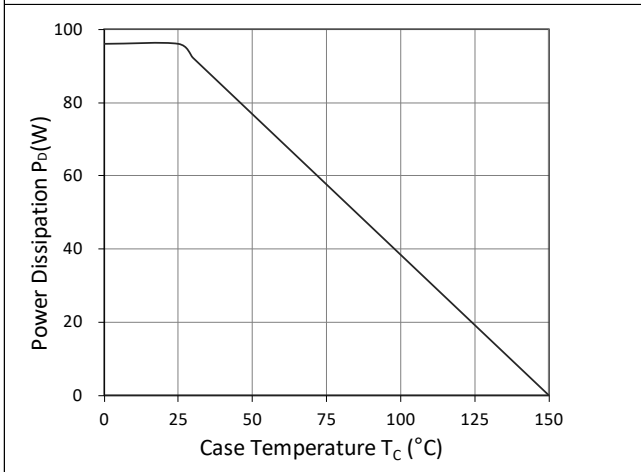


Figure 9. Power Dissipation

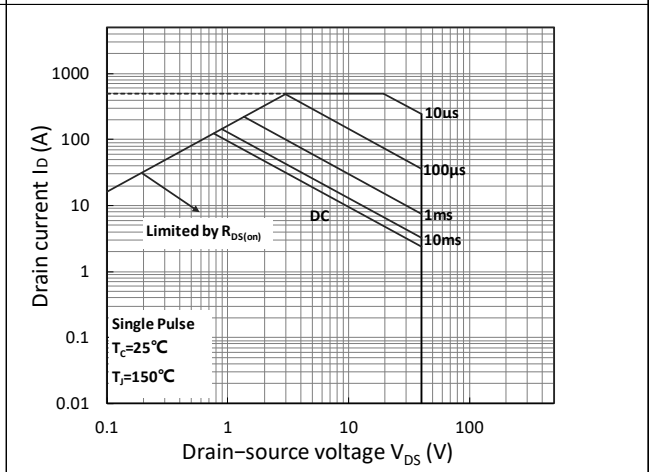


Figure 10. Safe Operating Area

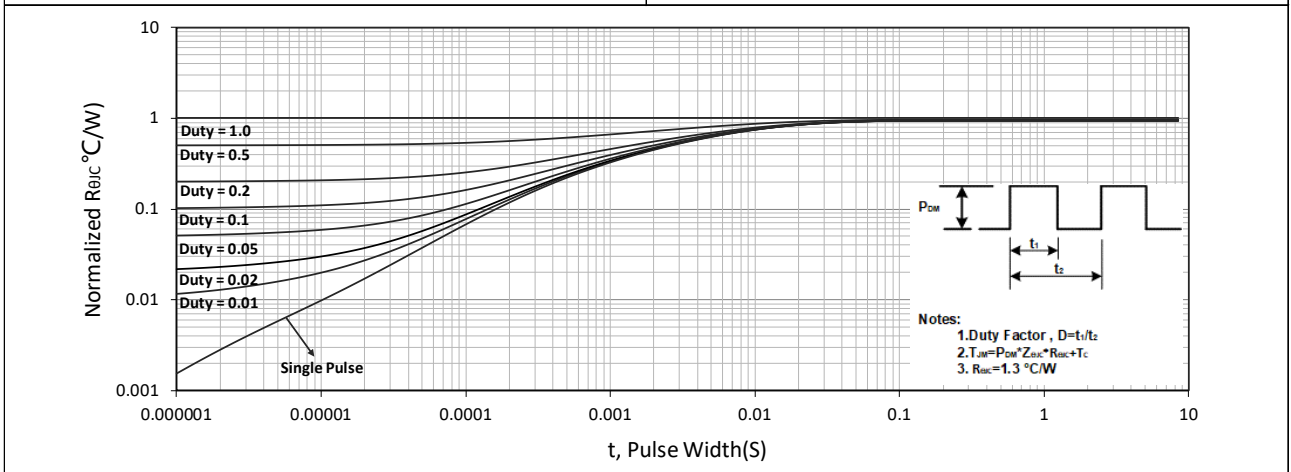


Figure 11. Normalized Maximum Transient Thermal Impedance

Test Circuit

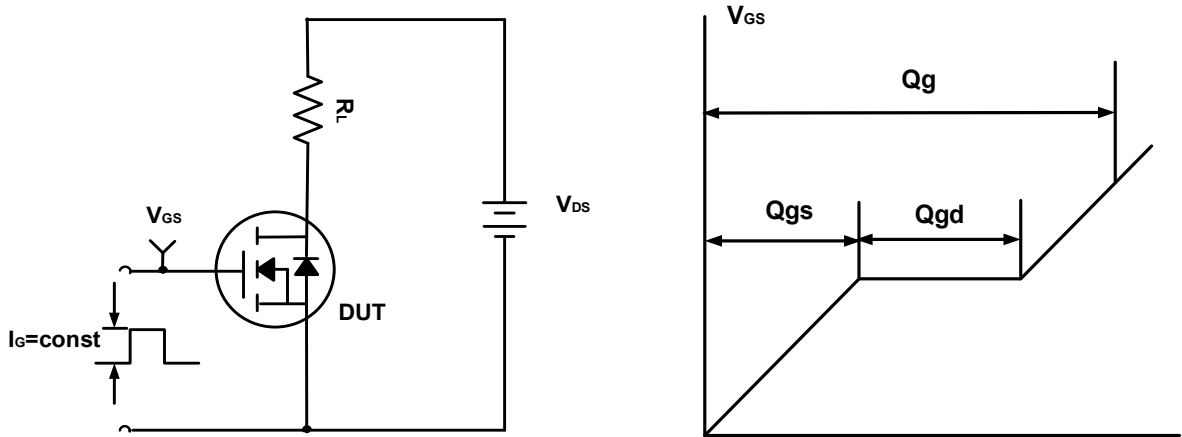


Figure A. Gate Charge Test Circuit & Waveforms

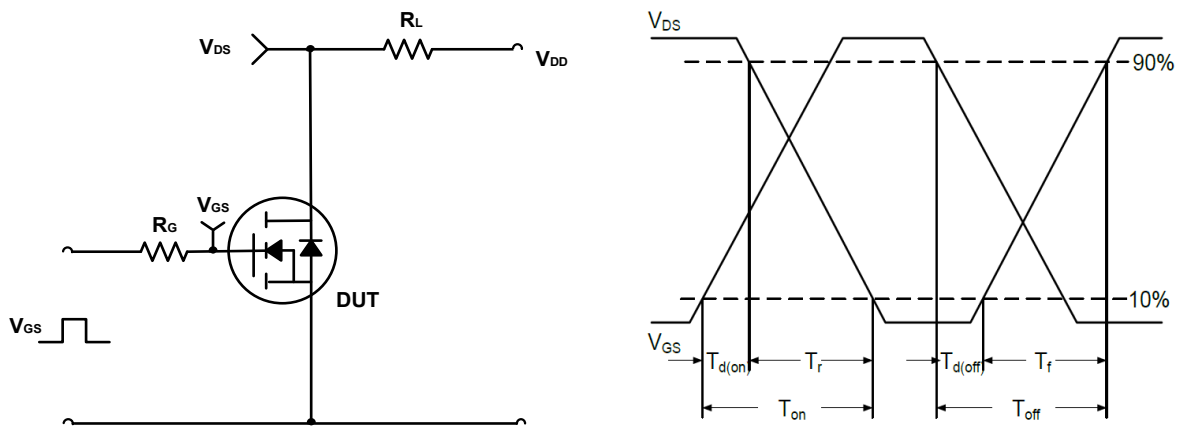


Figure B. Switching Test Circuit & Waveforms

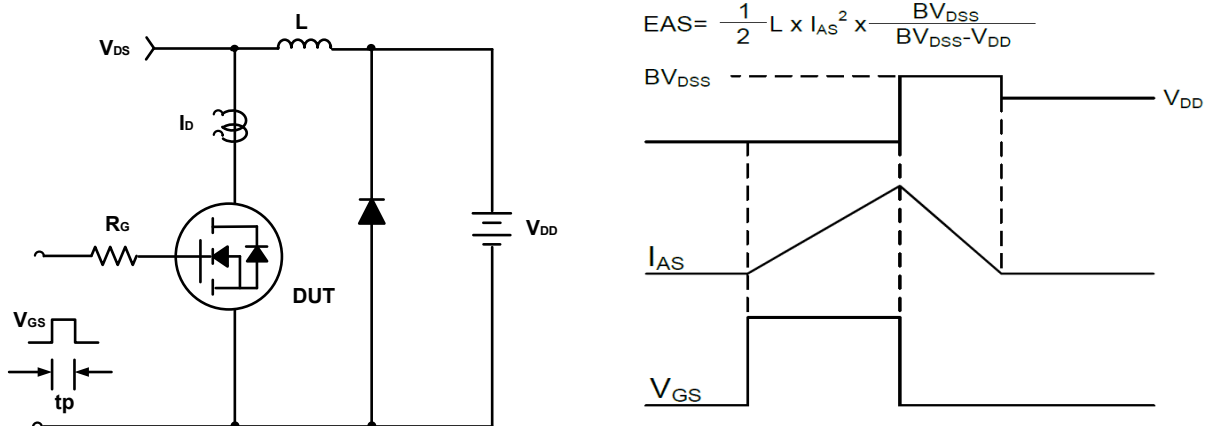
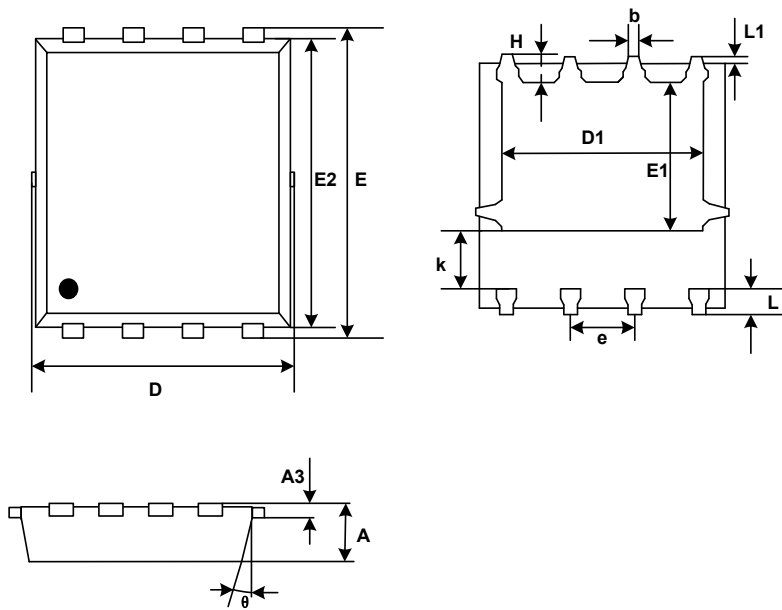


Figure C. Unclamped Inductive Switching Circuit & Waveforms

Mechanical Dimensions for PDFN5060-8L

COMMON DIMENSIONS

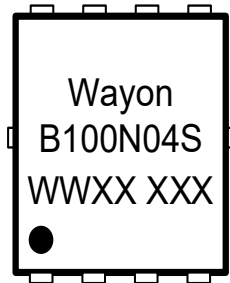


SYMBOL	MM	
	MIN	MAX
A	0.90	1.20
A3	0.15	0.35
D	4.80	5.40
E	5.90	6.35
D1	3.61	4.31
E1	3.30	3.92
E2	5.50	6.06
k	1.10	-
b	0.30	0.51
e	1.27BSC	
L	0.38	0.71
L1	0.05	0.36
H	0.38	0.71
θ	0°	12°

Ordering Information

Part	Package	Marking	Packing method
WMB100N04TS	PDFN5060-8L	B100N04S	Tape and Reel

Marking Information



B100N04S= Device code

WWXX XXX= Date code

Contact Information

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