

1. General description

Planar passivated AC Thyristor Triac power switch in a SOT186A (TO-220F) "full pack" plastic package with self-protective capabilities against low and high energy transients.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- Direct interfacing with low power drivers and microcontrollers
- Full cycle AC conduction
- Isolated mounting base package
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Safe clamping capability for low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls

4. Quick reference data

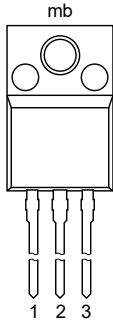
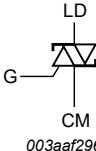
Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------|--------------------------------------|---|-----|-----|-----|------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_h \leq 94\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | - | 4 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 35 | A |
| | | full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$ | - | - | 39 | A |
| T_j | junction temperature | | - | - | 125 | °C |
| V_{PP} | peak pulse voltage | $T_j = 25\text{ °C}$; non-repetitive, off-state; Fig. 6 | - | - | 2 | kV |

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|-----|-----|-----|------|
| Static characteristics | | | | | | |
| I _{GT} | gate trigger current | V _D = 12 V; I _T = 100 mA; LD+ G+; T _j = 25 °C; Fig. 8 | - | - | 10 | mA |
| | | V _D = 12 V; I _T = 100 mA; LD+ G-; T _j = 25 °C; Fig. 8 | - | - | 10 | mA |
| | | V _D = 12 V; I _T = 100 mA; LD- G-; T _j = 25 °C; Fig. 8 | - | - | 10 | mA |
| I _H | holding current | V _D = 12 V; T _j = 25 °C; Fig. 10 | - | - | 20 | mA |
| V _T | on-state voltage | I _T = 6 A; T _j = 25 °C; Fig. 11 | - | - | 1.7 | V |
| V _{CL} | clamping voltage | I _{CL} = 0.1 mA; t _p = 1 ms; T _j = 25 °C | 850 | - | - | V |
| Dynamic characteristics | | | | | | |
| dV _D /dt | rate of rise of off-state voltage | V _{DM} = 536 V; T _j = 125 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit; Fig. 13 | 500 | - | - | V/μs |
| di _{com} /dt | rate of change of commutating current | V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 20 V/μs; (snubberless condition); gate open circuit; Fig. 14 ; Fig. 15 | 4 | - | - | A/ms |
| | | V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 10 V/μs; gate open circuit; Fig. 14 ; Fig. 15 | 5 | - | - | A/ms |
| | | V _D = 400 V; T _j = 125 °C; I _{T(RMS)} = 4 A; dV _{com} /dt = 1 V/μs; gate open circuit; Fig. 14 ; Fig. 15 | 8 | - | - | A/ms |

5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-------------------------|--|---|
| 1 | CM | common |  <p style="text-align: center;">mb</p> <p style="text-align: center;">1 2 3</p> <p style="text-align: center;">TO-220F (SOT186A)</p> |  <p style="text-align: center;">LD</p> <p style="text-align: center;">G</p> <p style="text-align: center;">CM</p> <p style="text-align: center;">003aaf296</p> |
| 2 | LD | load | | |
| 3 | G | gate | | |
| mb | n.c. | mounting base; isolated | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|---|---------|
| | Name | Description | Version |
| ACTT4X-800E | TO-220F | plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" | SOT186A |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|--|-----|-----|------------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_h \leq 94\text{ }^\circ\text{C}$; Fig. 1 ; Fig. 2 ; Fig. 3 | - | 4 | A |
| I_{TSM} | non-repetitive peak on-state current | full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5 | - | 35 | A |
| | | full sine wave; $T_{j(\text{init})} = 25\text{ }^\circ\text{C}$; $t_p = 16.7\text{ ms}$ | - | 39 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; sine-wave pulse | - | 6 | A^2s |
| di_T/dt | rate of rise of on-state current | $I_G = 20\text{ mA}$ | - | 100 | $\text{A}/\mu\text{s}$ |
| I_{GM} | peak gate current | $t = 20\text{ }\mu\text{s}$ | - | 2 | A |
| P_{GM} | peak gate power | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.5 | W |
| T_j | junction temperature | | - | 125 | $^\circ\text{C}$ |
| V_{PP} | peak pulse voltage | $T_j = 25\text{ }^\circ\text{C}$; non-repetitive, off-state; Fig. 6 | - | 2 | kV |

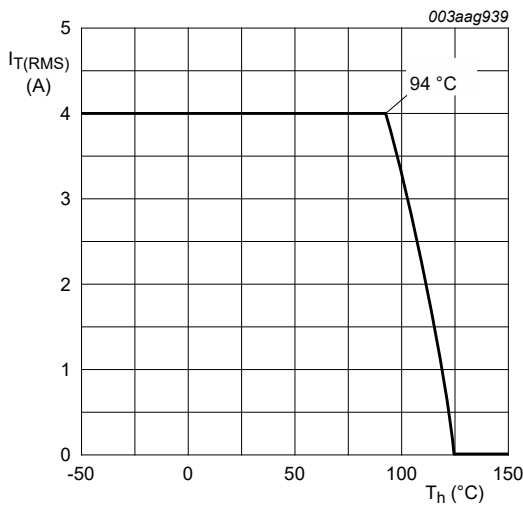


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

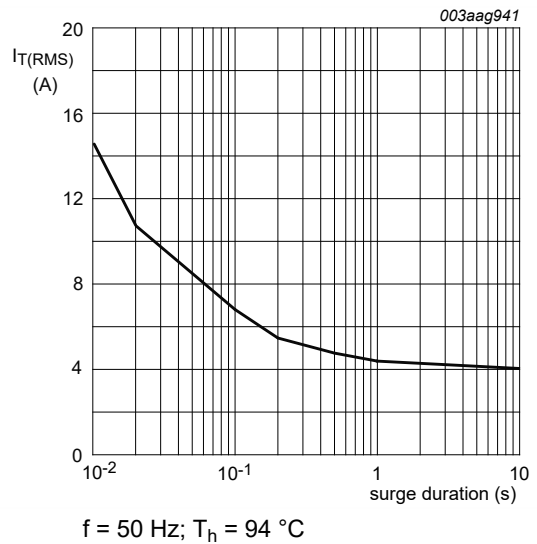


Fig. 2. on-state current as a function of surge duration; maximum values

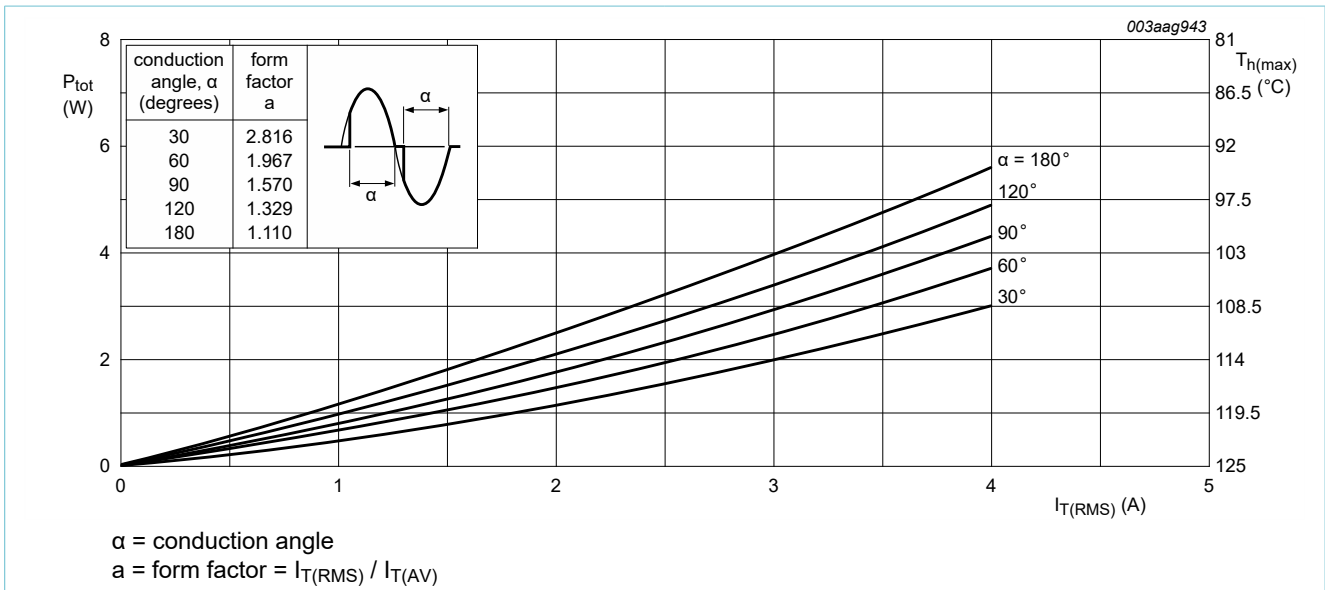


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

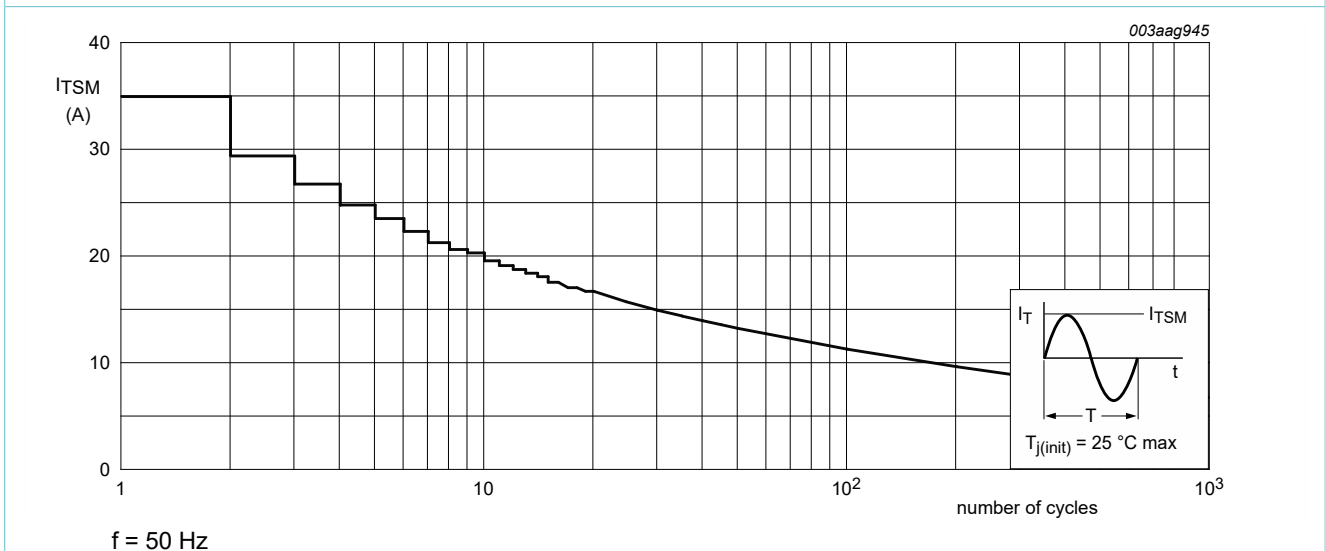


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

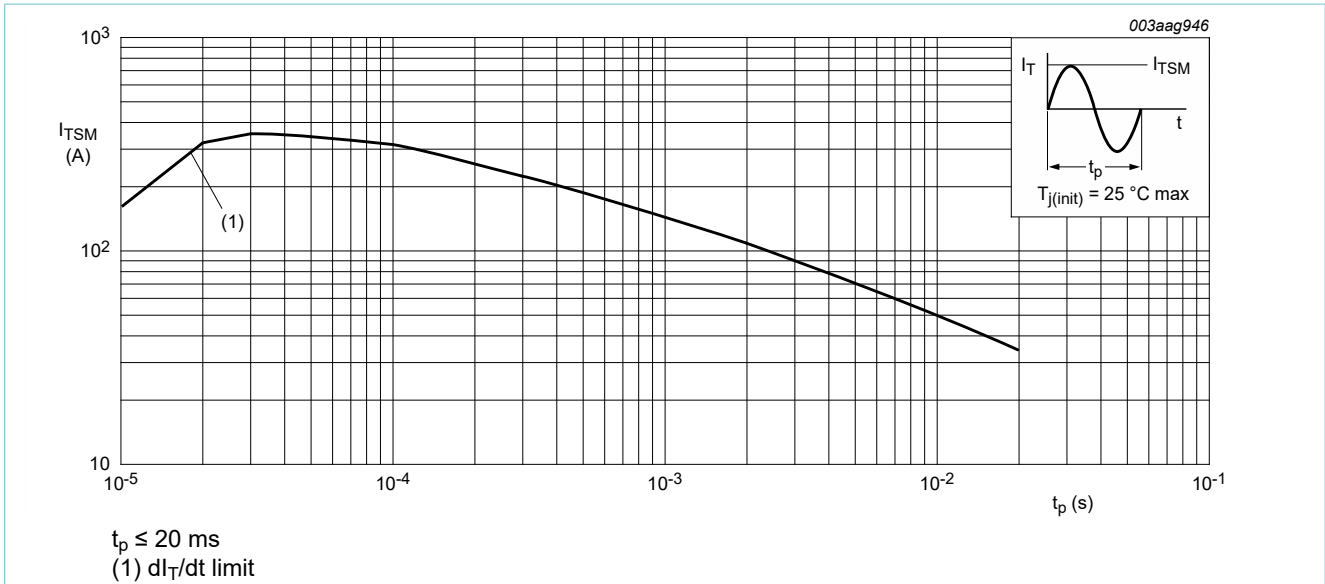


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

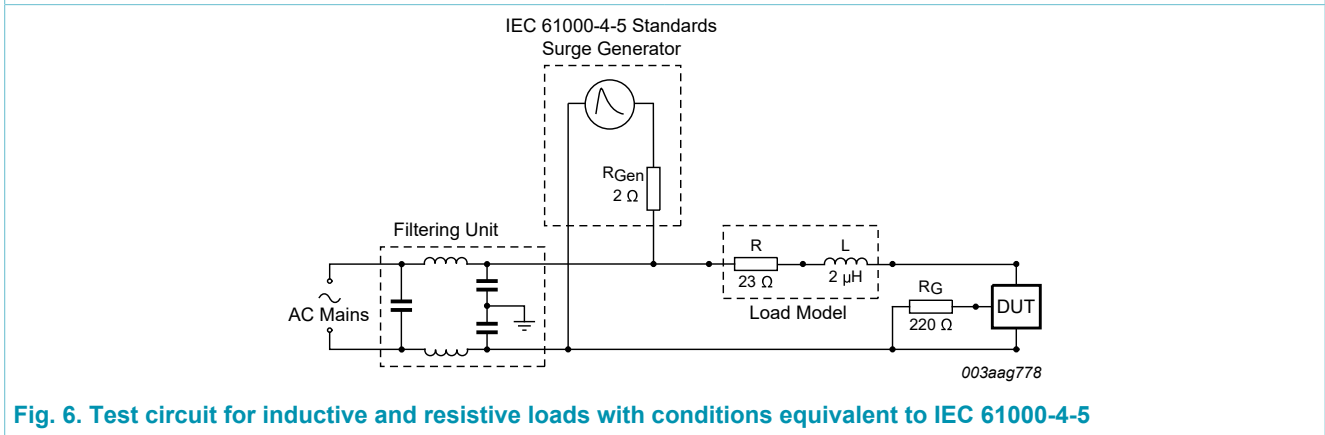
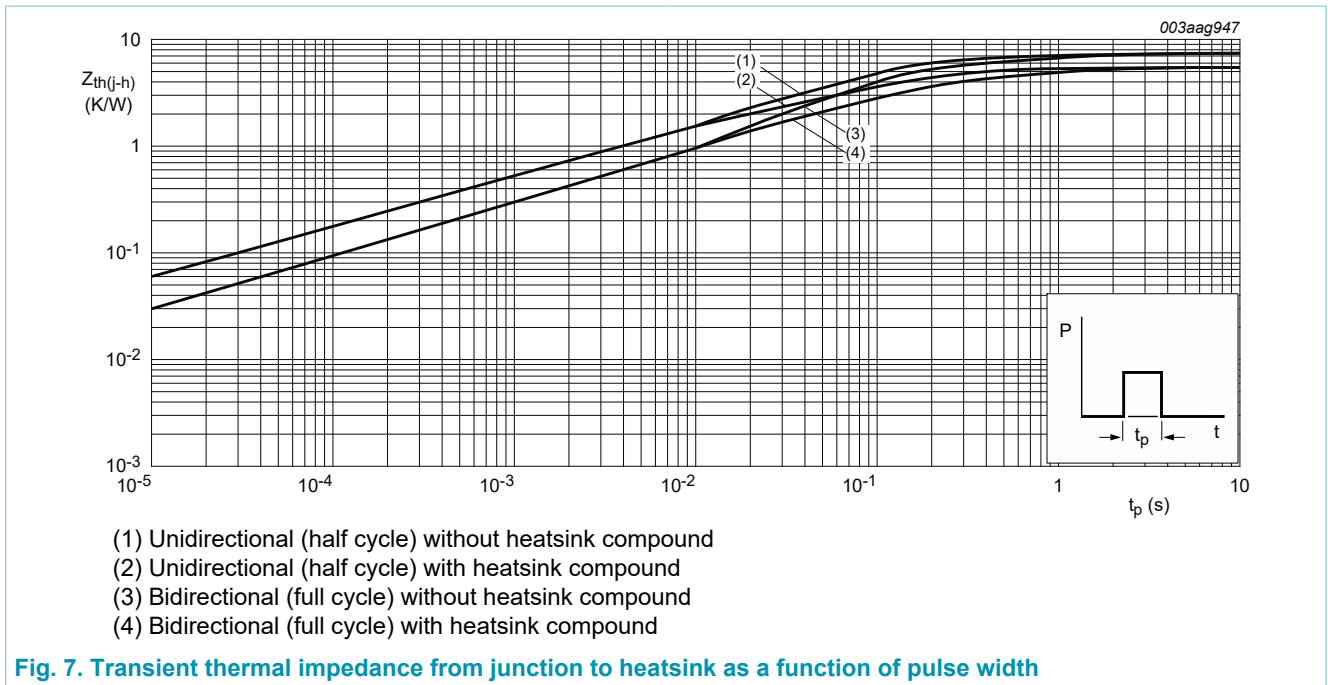


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

8. Thermal characteristics

Table 5. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--|---|-----|-----|-----|------|
| R _{th(j-h)} | thermal resistance from junction to heatsink | full cycle or half cycle; with heatsink compound; Fig. 7 | - | - | 5.5 | K/W |
| | | full cycle or half cycle; without heatsink compound; Fig. 7 | - | - | 7.2 | K/W |
| R _{th(j-a)} | thermal resistance from junction to ambient free air | in free air | - | 55 | - | K/W |



9. Isolation characteristics

Table 6. Isolation characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|-----------------------|--|-----|-----|------|------|
| V _{isol(RMS)} | RMS isolation voltage | from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz ≤ f ≤ 60 Hz; T _h = 25 °C | - | - | 2500 | V |
| C _{isol} | isolation capacitance | from main terminal 2 to external heatsink; f = 1 MHz; T _h = 25 °C | - | 10 | - | pF |

10. Characteristics

Table 7. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|--|-----|------|-----|------------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 8 | - | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 8 | - | - | 10 | mA |
| | | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 8 | - | - | 10 | mA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 30 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 40 | mA |
| | | $V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 9 | - | - | 30 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 10 | - | - | 20 | mA |
| V_T | on-state voltage | $I_T = 6\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11 | - | - | 1.7 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 12 | - | 0.8 | 1 | V |
| | | $V_D = 400\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 125\text{ °C}$; Fig. 12 | 0.2 | 0.45 | - | V |
| I_D | off-state current | $V_D = 800\text{ V}$; $T_j = 25\text{ °C}$ | - | - | 10 | μA |
| | | $V_D = 800\text{ V}$; $T_j = 125\text{ °C}$ | - | - | 0.5 | mA |
| V_{CL} | clamping voltage | $I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ °C}$ | 850 | - | - | V |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 13 | 500 | - | - | V/ μs |
| dI_{com}/dt | rate of change of commutating current | $V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 4\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; (snubberless condition); gate open circuit; Fig. 14 ; Fig. 15 | 4 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 4\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit; Fig. 14 ; Fig. 15 | 5 | - | - | A/ms |
| | | $V_D = 400\text{ V}$; $T_j = 125\text{ °C}$; $I_{T(RMS)} = 4\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit; Fig. 14 ; Fig. 15 | 8 | - | - | A/ms |

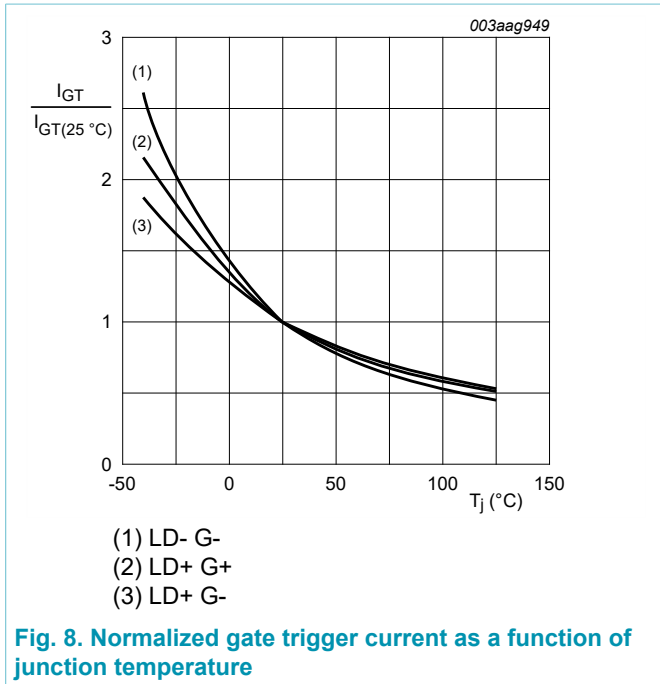


Fig. 8. Normalized gate trigger current as a function of junction temperature

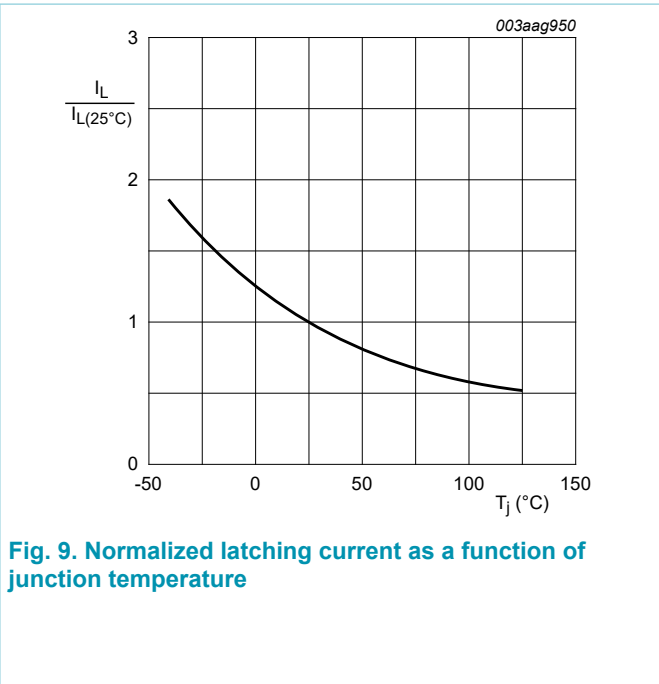


Fig. 9. Normalized latching current as a function of junction temperature

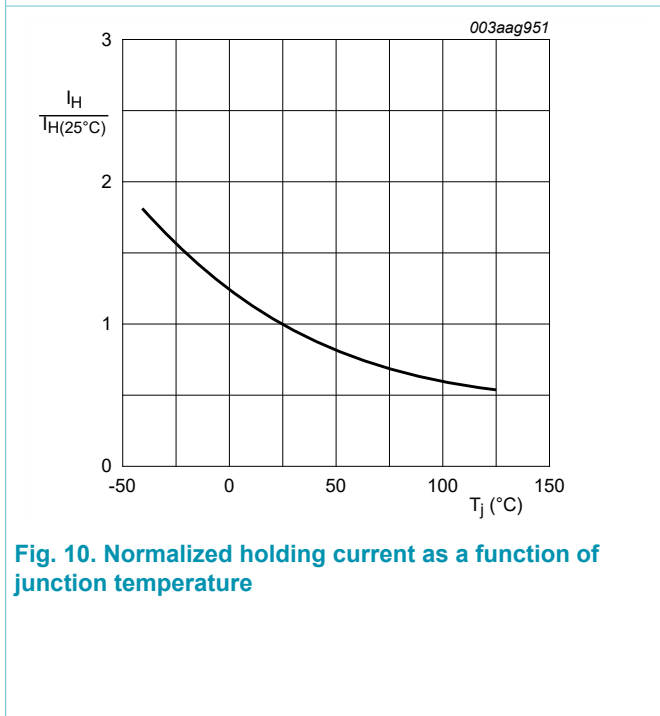


Fig. 10. Normalized holding current as a function of junction temperature

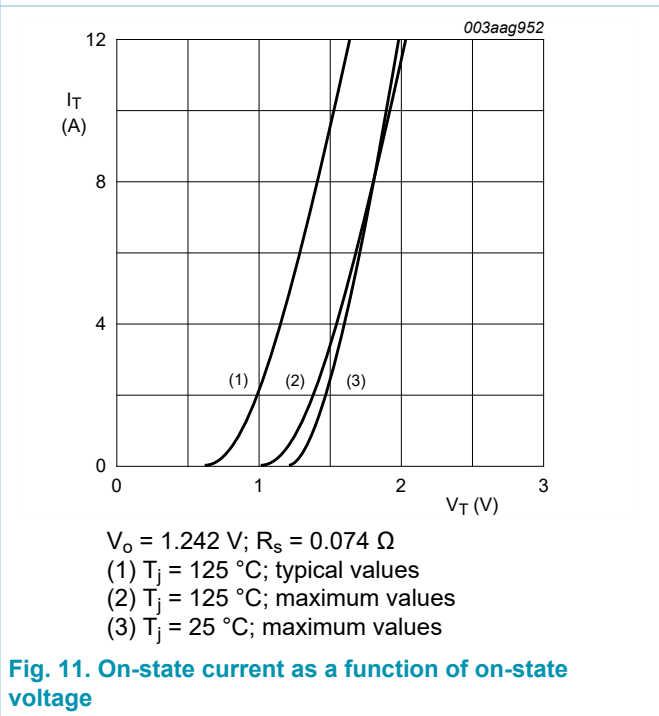


Fig. 11. On-state current as a function of on-state voltage

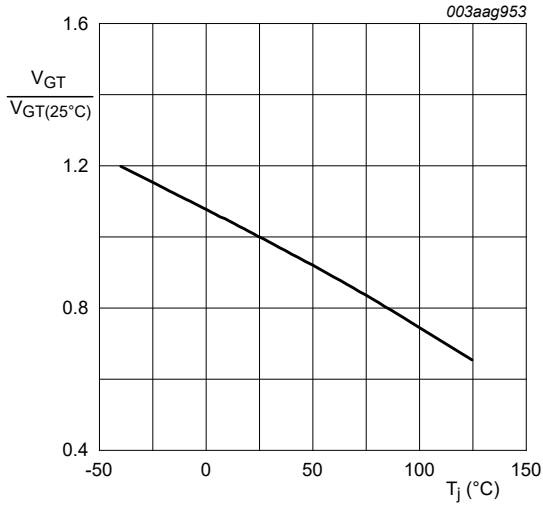
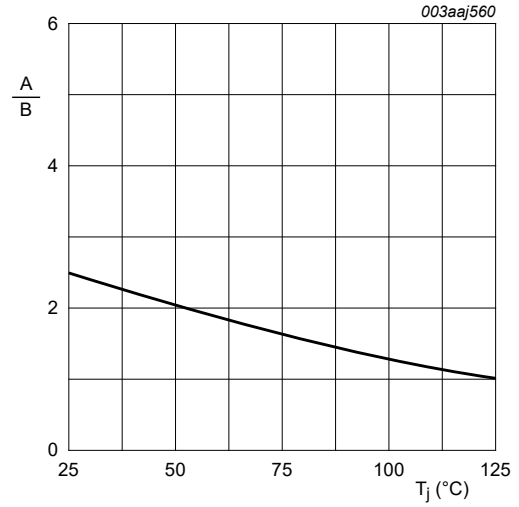
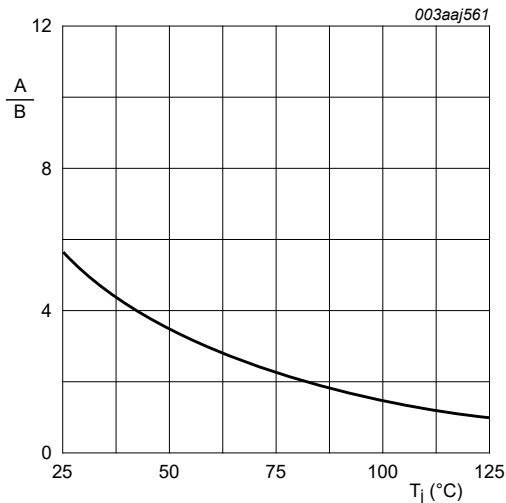


Fig. 12. Normalized gate trigger voltage as a function of junction temperature



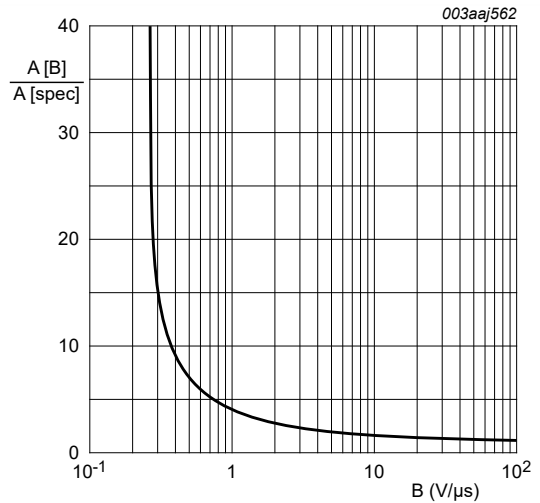
A = dV_D/dt at condition T_j °C
 B = dV_D/dt at condition T_j [125] °C

Fig. 13. Normalized rate of rise of off-state voltage as a function of junction temperature



A = di_{com}/dt at condition T_j °C
 B = di_{com}/dt at condition T_j [125] °C
 $V_D = 400$ V

Fig. 14. Normalized critical rate of rise of commutating current as a function of junction temperature



A [B] is di_{com}/dt at condition B, dV_{com}/dt
 A [spec] is the specified data sheet value of di_{com}/dt
 turn-off time < 20 ms

Fig. 15. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

11. Package outline

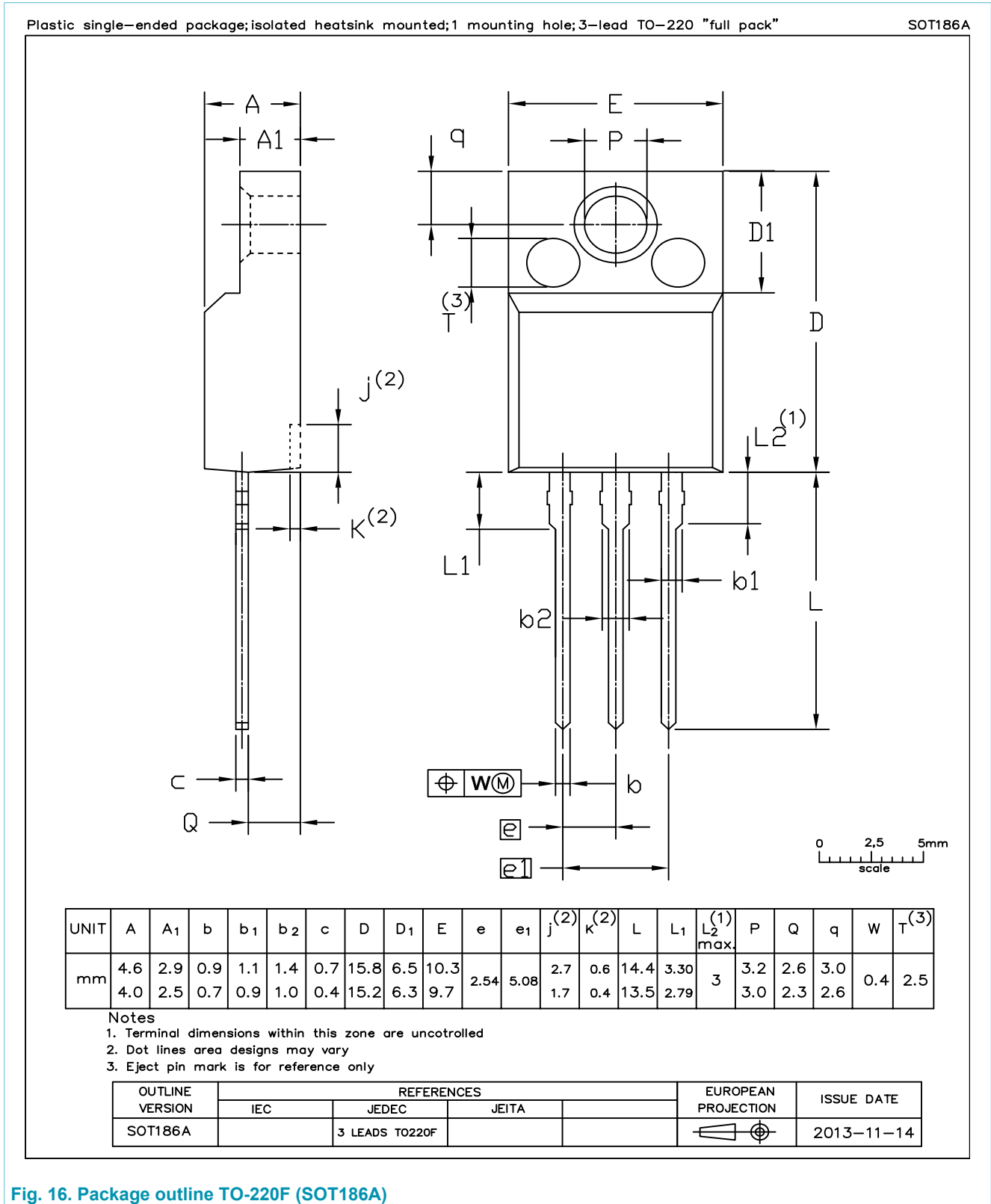


Fig. 16. Package outline TO-220F (SOT186A)

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|--------------------------------|--------------------|---|
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13. Contents

| | |
|-----------------------------------|----|
| 1. General description..... | 1 |
| 2. Features and benefits..... | 1 |
| 3. Applications..... | 1 |
| 4. Quick reference data..... | 1 |
| 5. Pinning information..... | 2 |
| 6. Ordering information..... | 3 |
| 7. Limiting values..... | 4 |
| 8. Thermal characteristics..... | 7 |
| 9. Isolation characteristics..... | 7 |
| 10. Characteristics..... | 8 |
| 11. Package outline..... | 11 |
| 12. Legal information..... | 12 |

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