**Product data sheet** 

## 1. General description

Planar passivated very sensitive gate four quadrant triac in a SOT54 plastic package intended for use in general purpose bidirectional switching and phase control applications. This very sensitive gate "series D" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drivers and microcontrollers
- Enhanced current surge capability
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Triggering in all four quadrants
- Very sensitive gate

## 3. Applications

- · Air conditioner indoor fan control
- · Battery powered applications
- · General purpose switching and phase control

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{DRM}$	repetitive peak off- state voltage		-	-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; $T_{lead} \le 51$ °C; <u>Fig. 1</u> ; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	-	1	А
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 20 \text{ ms}$ ; $Fig. 4$ ; $Fig. 5$	-	-	16	А
		full sine wave; $T_{j(init)} = 25 ^{\circ}C$ ; $t_p = 16.7  ms$	-	-	17.5	Α
Tj	junction temperature		-	-	125	°C
Static characte	eristics					
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	-	2	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ \text{ G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	2.5	5	mA

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	2.5	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G+};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	5	10	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	1.2	10	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 5 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.4	1.7	V
Dynamic char	acteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; $T_j$ = 125 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; $R_{GT1(ext)}$ = 1 kΩ	-	5	-	V/µs

# 5. Pinning information

## **Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T2	main terminal 2		T2——T1
2	G	gate		G sym051
3	T1	main terminal 1	TO-92 (SOT54)	Sylnoon

# 6. Ordering information

### **Table 3. Ordering information**

Type number	Package	kage				
	Name	Description	Version			
BT132-600D	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54			

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# 7. Limiting values

## **Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; T <sub>lead</sub> ≤ 51 °C; <u>Fig. 1</u> ; <u>Fig. 2</u> ; <u>Fig. 3</u>	-	1	Α
	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5	-	16	Α
		full sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 16.7 \text{ ms}$	-	17.5	Α
I <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN	-	1.28	A²s
dl <sub>T</sub> /dt	rate of rise of on-state	I <sub>G</sub> = 0.2 A	-	50	A/µs
	current		-	50	A/µs
			-	50	A/µs
			-	10	A/µs
I <sub>GM</sub>	peak gate current		-	2	Α
$P_{GM}$	peak gate power		-	5	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period	-	0.5	W
T <sub>stg</sub>	storage temperature		-40	150	°C
Tj	junction temperature		-	125	°C

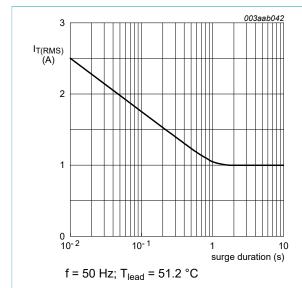


Fig. 1. RMS on-state current as a function of surge duration; maximum values

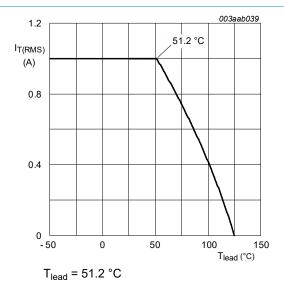


Fig. 2. RMS on-state current as a function of lead temperature; maximum values

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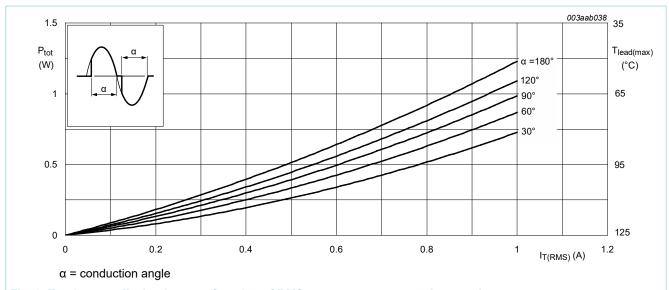


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

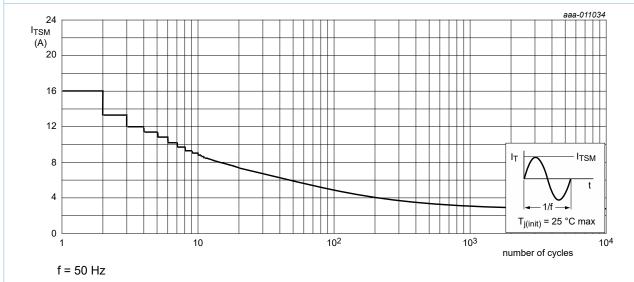
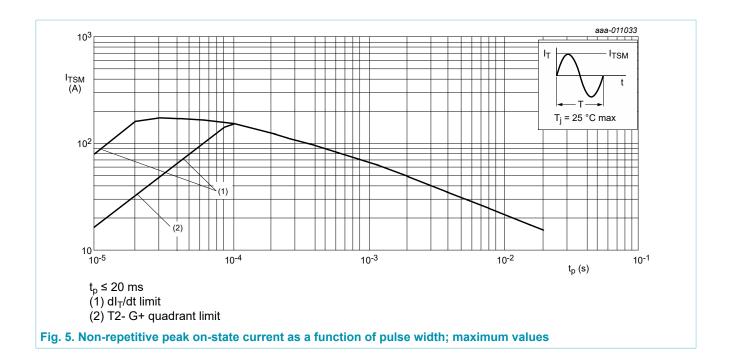


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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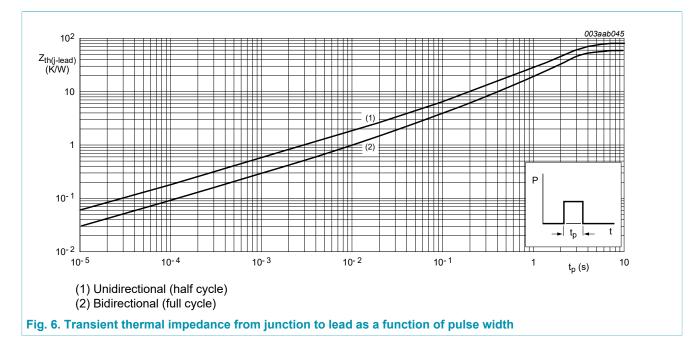


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## 8. Thermal characteristics

**Table 5. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-lead)</sub>	thermal resistance from junction to lead	full cycle; Fig. 6	-	-	60	K/W
		half cycle; Fig. 6	-	-	80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit mounted: lead length = 4 mm	-	150	-	K/W



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## 9. Characteristics

### **Table 6. Characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics				,	
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T2+ G+; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	2	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ \text{ G-};$ $T_j = 25 \text{ °C}; Fig. 7$	-	2.5	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	2.5	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- G+;$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	5	10	mA
l <sub>L</sub>	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 8}}{}$	-	1.6	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2+ G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 8}}{\text{C}}$	-	4.5	15	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 8}}{\text{C}}$	-	1.2	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G+};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 8}}{\text{C}}$	-	2.2	15	mA
Н	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	1.2	10	mA
/ <sub>T</sub>	on-state voltage	I <sub>T</sub> = 5 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.4	1.7	V
√ <sub>GT</sub>	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11	-	0.7	1	V
		$V_D = 400 \text{ V}; I_T = 0.1 \text{ A}; T_j = 125 ^{\circ}\text{C};$ Fig. 11	0.25	0.4	-	V
D	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 125 °C	-	0.1	0.5	mA
Dynamic ch	naracteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; $T_j$ = 125 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; $R_{GT1(ext)}$ = 1 kΩ	-	5	-	V/µs
gt	gate-controlled turn-on time	$I_{TM}$ = 6 A; $V_D$ = 600 V; $I_G$ = 0.1 A; $dI_G/$ dt = 5 A/µs	-	2	-	μs

7 / 13

3

2

1

0

-60

I<sub>L</sub> (25 °C)

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140

T<sub>i</sub> (°C)

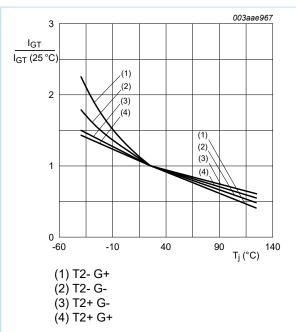


Fig. 8. Normalized latching current as a function of junction temperature

40

-10



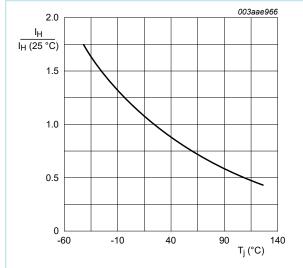
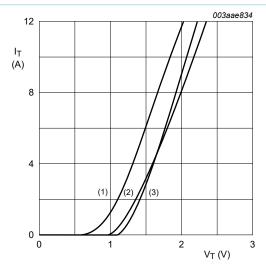


Fig. 9. Normalized holding current as a function of junction temperature



 $V_0 = 1.27 \text{ V}$  $R_s = 0.091 \Omega$ 

(1)  $T_j = 125$  °C; typical values (2)  $T_j = 125$  °C; maximum values (3)  $T_j = 25$  °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

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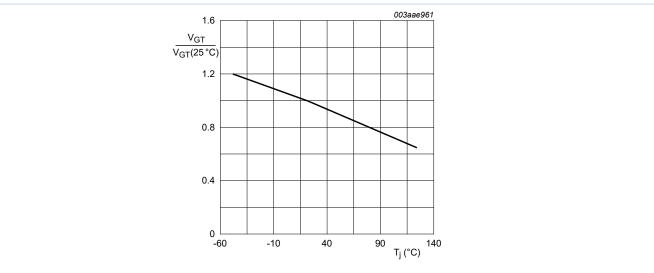
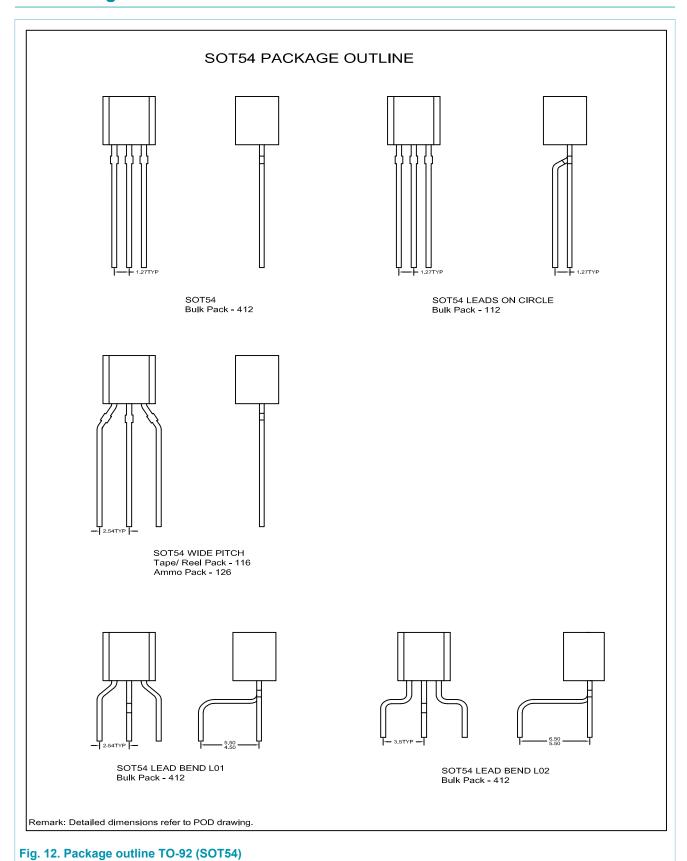


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

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# 10. Package outline



T422 COOD

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# 11. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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For more information, please visit: http://www.ween-semi.com
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