BT134-800E

4Q Triac

Rev.01 - 28 April 2018 Product data sheet

1. General description

Planar passivated sensitive gate four quadrant triac in a SOT82 (SIP3) plastic package intended for use in general purpose bidirectional switching and phase control applications. This "series E" sensitive gate triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Low holding current for low current loads and lowest EMI at commutation
- Triggering in all four quadrants
- Compact package
- Direct interfacing to logic level ICs
- Direct interfacing to low power gate drive circuits
- Sensitive gate

3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control

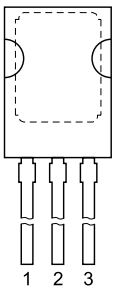
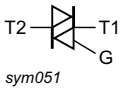
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Values				Unit
Absolute maximum rating							
V_{DRM}	repetitive peak off-state voltage		800				V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C; Fig. 1; Fig. 2; Fig. 3	4				A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5	25				A
Symbol	**Parameter**	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12$ V; $I_T = 0.1$ A; T2+ G+; $T_j = 25$ °C; Fig. 7		-	2.5	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2+ G-; $T_j = 25$ °C; Fig. 7		-	4	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2- G-; $T_j = 25$ °C; Fig. 7		-	5	10	mA
		$V_D = 12$ V; $I_T = 0.1$ A; T2- G+; $T_j = 25$ °C; Fig. 7		-	11	25	mA
I_H	holding current	$V_D = 12$ V; $T_j = 25$ °C; Fig. 9		-	2.2	15	mA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT134-800E	SIP3	plastic single-ended package; 3-leads (in-line)	SOT82

7. Marking

Table 4. Marking codes

Type number	Marking codes
BT134-800E	BT134-800E

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C; Fig 1; Fig 2; Fig 3	4	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig 4; Fig 5	25	A
		full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.7$ ms	27	A
I^2t	I^2t for fusing	$t_P = 10$ ms; SIN	3.1	A^2s
dI_T/dt	rate of rise of on-state current	$I_G = 20$ mA; T2+ G+	50	A/µs
		$I_G = 20$ mA; T2+ G-	50	A/µs
		$I_G = 20$ mA; T2- G-	50	A/µs
		$I_G = 50$ mA; T2- G+	10	A/µs
I_{GM}	peak gate current		2	A
P_{GM}	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.5	W
T_{stg}	storage temperature		-40 to 150	°C
T_j	junction temperature		125	°C

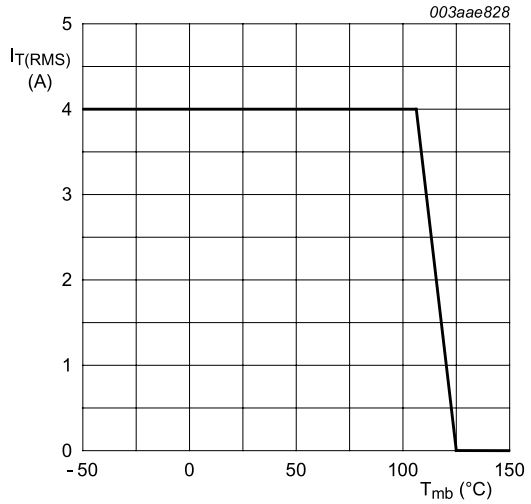
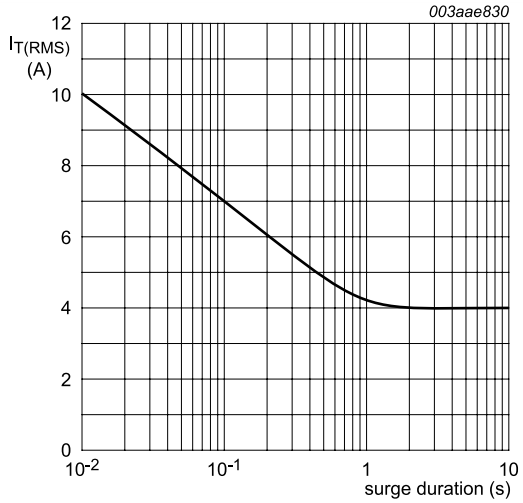
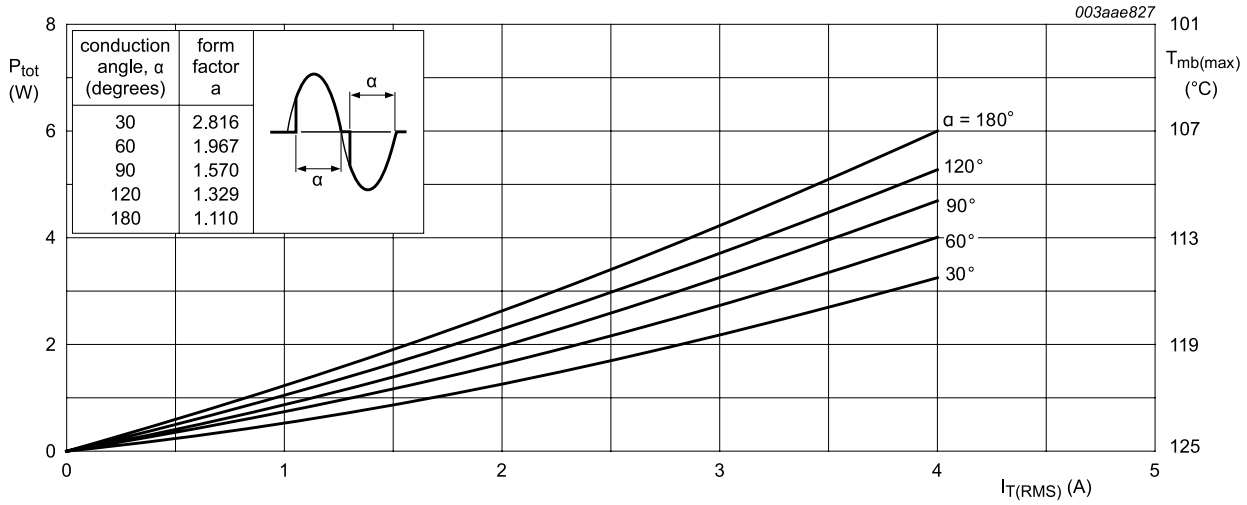


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz; $T_{mb} \leq 107$ °C

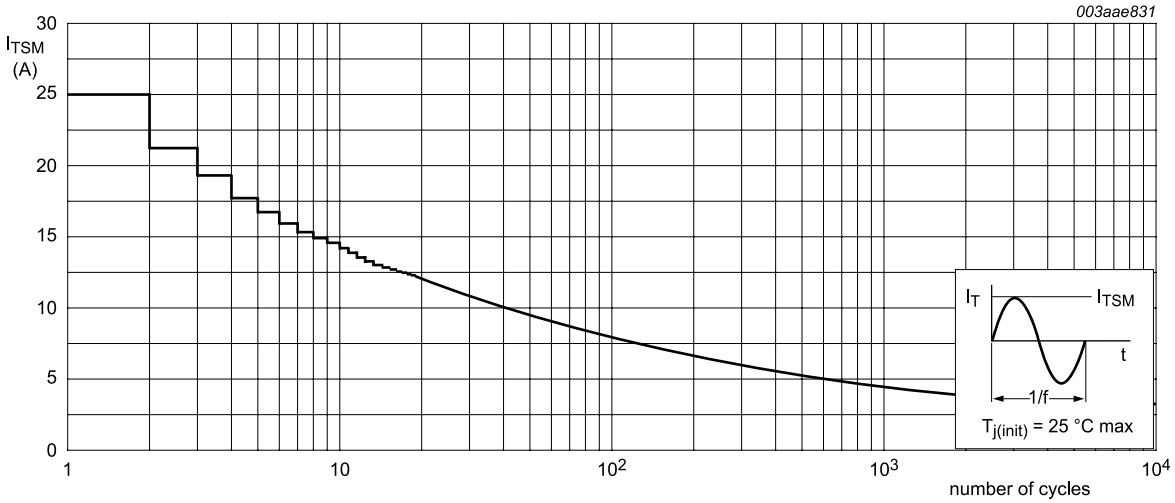
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

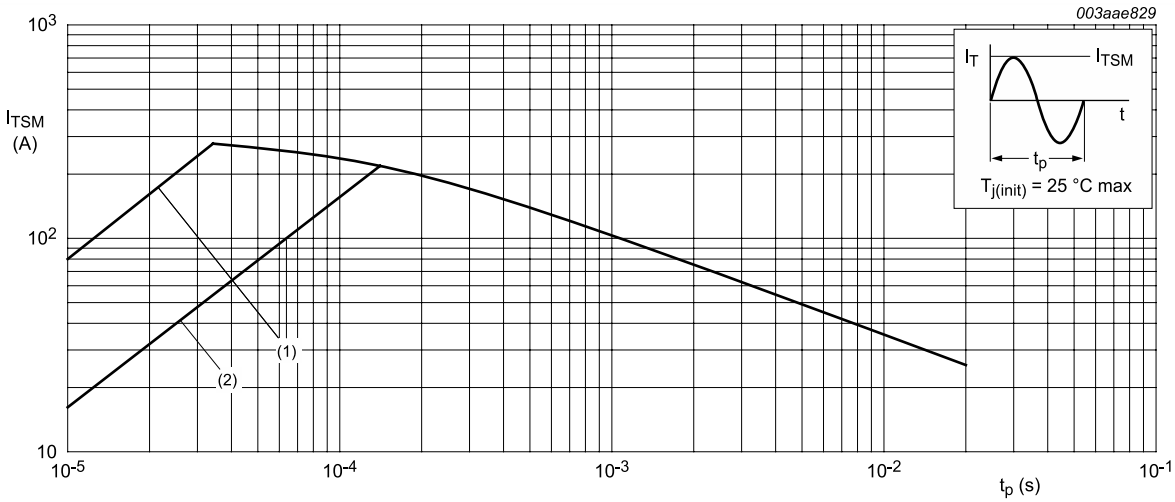
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

(2) T2- G+ quadrant limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	half cycle; Fig 6		-	-	3.7	K/W
		full cycle; Fig 6		-	-	3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	100	-	K/W

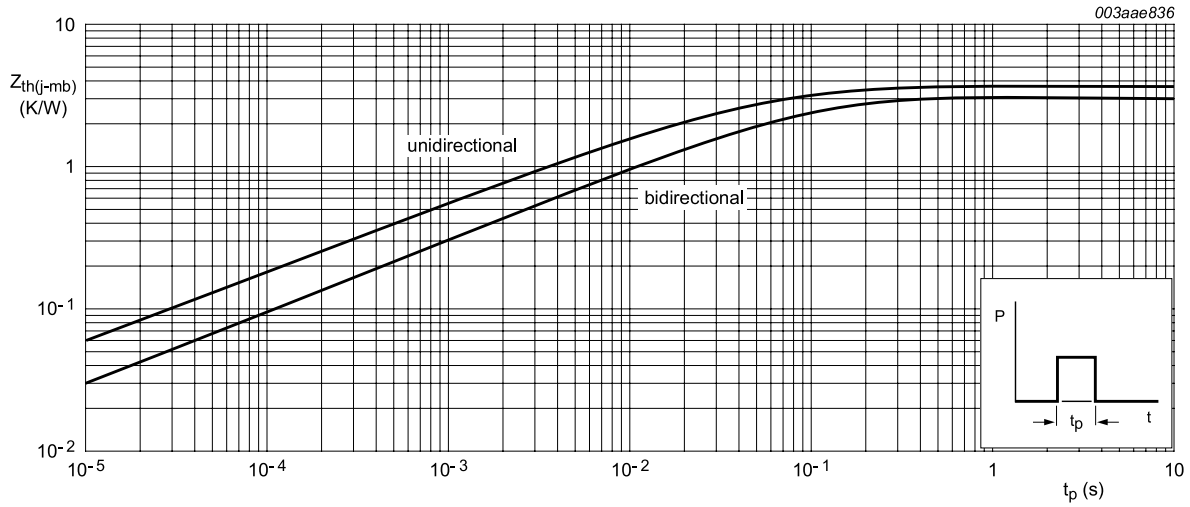
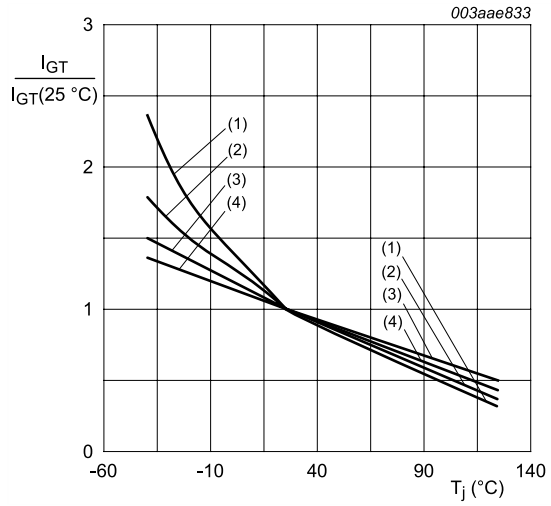


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		-	2.5	10	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		-	4	10	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		-	5	10	mA
		V_D = 12 V; I_T = 0.1 A; T2- G+; T_j = 25 °C; Fig. 7		-	11	25	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 8		-	3	15	mA
		V_D = 12 V; I_G = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 8		-	10	20	mA
		V_D = 12 V; I_G = 0.1 A; T2- G-; T_j = 25 °C; Fig. 8		-	2.5	15	mA
		V_D = 12 V; I_G = 0.1 A; T2- G+; T_j = 25 °C; Fig. 8		-	4	20	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	2.2	15	mA
V_T	on-state voltage	I_T = 5 A; T_j = 25 °C; Fig. 10		-	1.4	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.7	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C; Fig. 11		0.25	0.4	-	V
I_D	off-state current	V_D = 800 V; T_j = 125 °C		-	0.1	0.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		-	50	-	V/µs
t_{gt}	gate-controlled turn-on time	V_D = 800 V; I_{TM} = 6 A; I_G = 0.1 A; dI_G/dt = 5 A/µs		-	2	-	µs



(1) T2- G+
(2) T2- G-
(3) T2+ G-
(4) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

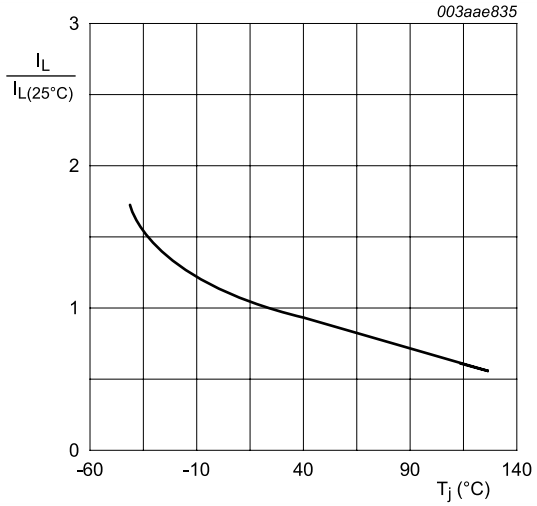


Fig. 8. Normalized latching current as a function of junction temperature

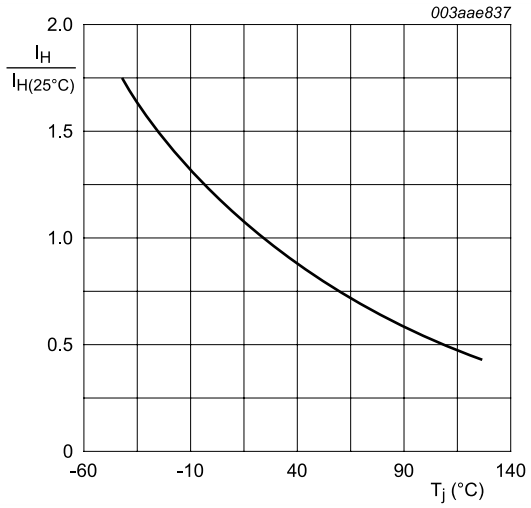
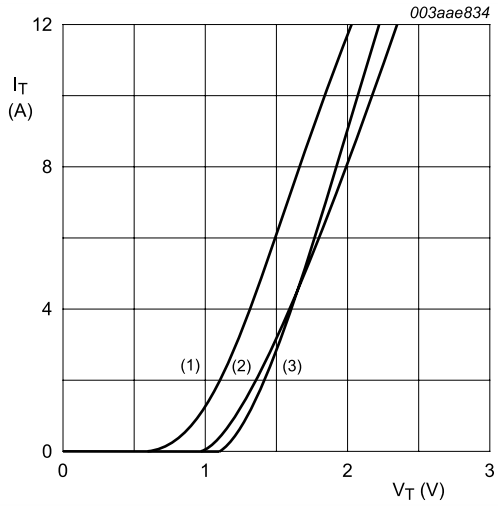


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.27 V; R_s = 0.091 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

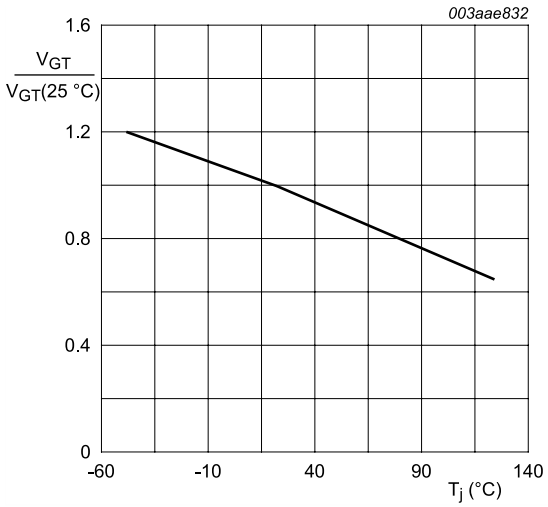
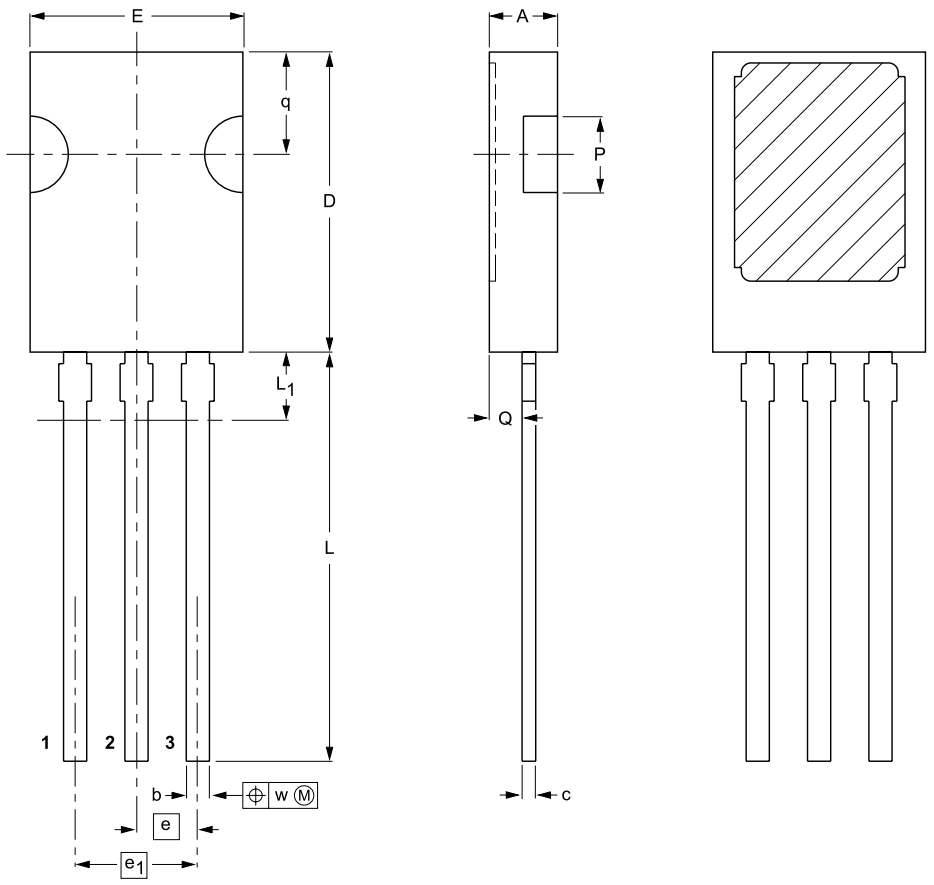


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic single-ended package; 3 leads (in-line) **SOT82**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	e_1	L	L_1 (1) max.	P	Q	q	w
mm	2.8 2.3	0.88 0.65	0.58 0.47	11.1 10.5	7.8 7.2	2.29	4.58	16.5 15.3	2.54	3.1 2.5	1.5 0.9	3.9 3.5	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for body and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT82						97-06-11

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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