**Product data sheet** 

## 1. General description

Planar passivated very sensitive gate four quadrant triac in a TO252 (DPAK) surface-mountable plastic package intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants. This very sensitive gate "series D" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

### 2. Features and benefits

- Direct triggering from low power drivers and logic ICs
- High blocking voltage capability
- Low holding current for low current loads and lowest EMI at commutation
- Planar passivated for voltage ruggedness and reliability
- Surface-mountable package
- Triggering in all four quadrants
- · Very sensitive gate

## 3. Applications

- General purpose motor control
- · General purpose switching

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Va	lues		Unit
Absolute	maximum rating						
$V_{DRM}$	repetitive peak off-state voltage		800			V	
$I_{T(RMS)}$	RMS on-state current	full sine wave; T <sub>mb</sub> ≤ 107 °C; Fig. 1; Fig. 2; Fig. 3	4			А	
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5	25			А	
		full sine wave; $T_{j(init)} = 25  ^{\circ}C$ ; $t_p = 16.7  \text{ms}$		2	27		Α
T <sub>j</sub>	junction temperature		125			°C	
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static ch	aracteristics						
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2 + G+;$ $T_j = 25 \text{ °C; } Fig. 7$		-	2	5	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; T2+ G-;}$ $T_j = 25 \text{ °C; } Fig. 7$		-	2.5	5	mA

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Static cha	Static characteristics						
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- \text{ G-};$ $T_j = 25 \text{ °C}; Fig. 7$		-	2.5	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2- G+; $ $T_j = 25 \text{ °C}; Fig. 7$		-	5	10	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>		-	1.2	10	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 5 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>		-	1.4	1.7	V
Dynamic	characteristics						
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 536 V; $T_{j}$ = 125 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; gate open circuit		-	5	-	V/µs

Although not recommended, off-state voltages up to 900V may be applied without damage, but the triac may switch to the on-state.

# 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		N
2	T2	main terminal 2		T2 T1
3	G	gate	[ <del>                                    </del>	sym051
mb	T2	mounting base; connected to main terminal 2		

# 6. Ordering information

Table 3. Ordering information

Type number	Package	Orderable part number	Packing	Small packing	Package	Package
	Name		method	quantity	version	issue date
BT136S-800D	TO252	BT136S-800DJ	Reel	2500	TO252N	14-Nov-2016

## 7. Marking

Table 4. Marking codes

Type number	Marking codes
BT136S-800D	136S8D

# 8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
$V_{DRM}$	repetitive peak off-state voltage		800	V
I <sub>T(RMS)</sub>	RMS on-state current	full sine wave; T <sub>mb</sub> ≤ 107 °C; Fig 1; Fig 2; Fig 3	4	А
I <sub>TSM</sub>	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 20 \text{ ms}$ ; Fig 4; Fig 5	25	А
		full sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 16.7 \text{ ms}$	27	Α
l <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN	3.1	A <sup>2</sup> s
dl <sub>⊤</sub> /dt	rate of rise of on-state current	I <sub>G</sub> = 20 mA	50	A/µs
I <sub>GM</sub>	peak gate current		2	Α
$P_{GM}$	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.5	W
T <sub>stg</sub>	storage temperature		-40 to 150	°C
T <sub>j</sub>	junction temperature		125	°C

Note: Although not recommended, off-state voltages up to 900V may be applied without damage, but the triac may switch to the on-state.

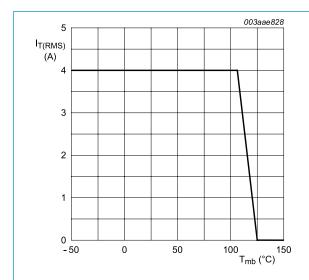
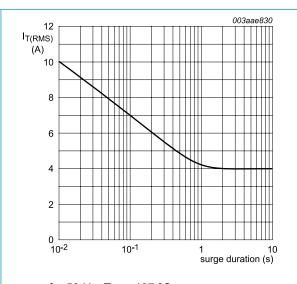
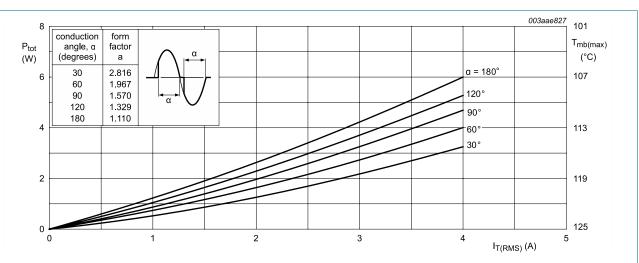


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



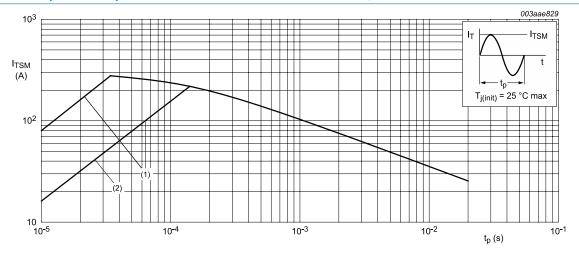
f = 50 Hz; T<sub>mb</sub> = 107 °C Fig. 2. RMS on-state current as a function of surge duration; maximum values



 $\alpha$  = conduction angle

a = form factor =  $I_{T(RMS)}$  /  $I_{T(AV)}$ 

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

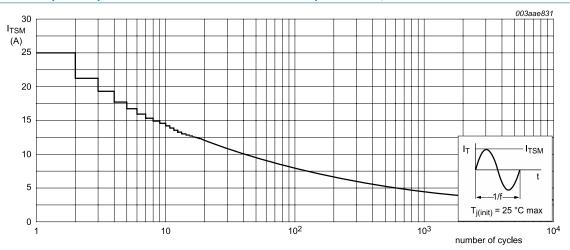


 $t_p \le 20 \text{ ms}$ 

 $(1) dI_T/dt limit$ 

(2) T2- G+ quadrant limit

Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values



f = 50 Hz

Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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## 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{\text{th(j-mb)}}$	thermal resistance	full; <u>Fig 6</u>	-	-	3	K/W
	from junction to mounting base	half cycle; <u>Fig 6</u>	-	-	3.7	
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	in free air	-	75	-	K/W

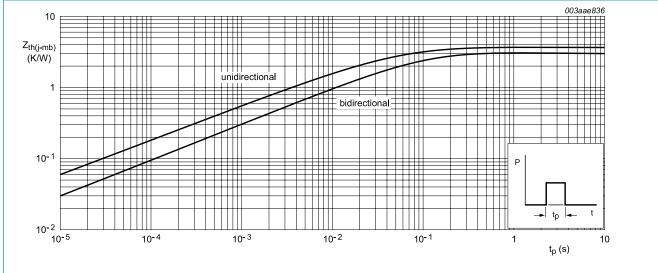
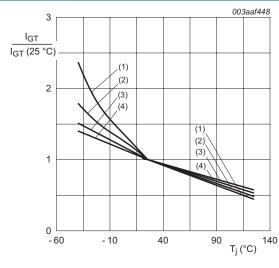


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

## 10. Characteristics

## **Table 7. Characteristics**

<b>Symbol</b>	Parameter	Conditions	Min	Тур	Max	Unit
Static ch	aracteristics				,	
I <sub>GT</sub>	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;  T_j = 25 °C; Fig. 7$	-	2	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G-;$ $T_j = 25 \text{ °C}; Fig. 7$	-	2.5	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \text{ Fig. 7}$	-	2.5	5	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G+};$ $T_j = 25 \text{ °C}; \text{ Fig. 7}$	-	5	10	mA
l <sub>t</sub>	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{T2+ G+};$ $T_j = 25 \text{ °C}; \text{Fig. 8}$	-	1.6	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2+ G-};$ $T_j = 25 \text{ °C}; \text{Fig. 8}$	-	4.5	15	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \text{ Fig. 8}$	-	1.2	10	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G+};$ $T_j = 25 \text{ °C}; \text{Fig. 8}$	-	2.2	15	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	1.2	10	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 5 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.4	1.7	V
$V_{\text{GT}}$	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11	-	0.7	1	V
		V <sub>D</sub> = 400 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 125 °C	0.25	0.4	-	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 800 V; T <sub>j</sub> = 125 °C	-	0.1	0.5	mA
Dynamic	characteristics			1		-
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 536 V; $T_{j}$ = 125 °C; ( $V_{DM}$ = 67% of $V_{DRM}$ ); exponential waveform; gate open circuit	-	5	-	V/µs



- (1) T2- G+
- (2) T2- G-
- (3) T2+ G-
- (4) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

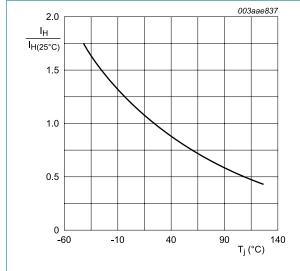


Fig. 9. Normalized holding current as a function of junction temperature

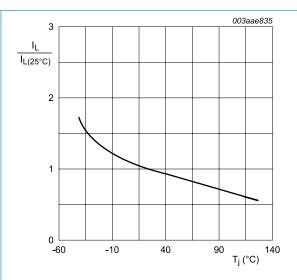
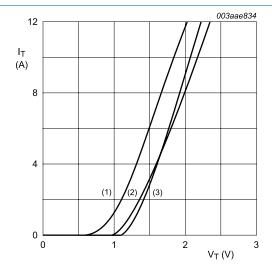


Fig. 8. Normalized latching current as a function of junction temperature



- $V_o$  = 1.27 V;  $R_s$  = 0.091  $\Omega$
- (1) T<sub>j</sub> = 125 °C; typical values (2) T<sub>j</sub> = 125 °C; maximum values
- (3)  $T_i = 25$  °C; maximum values
- Fig. 10. On-state current as a function of on-state voltage

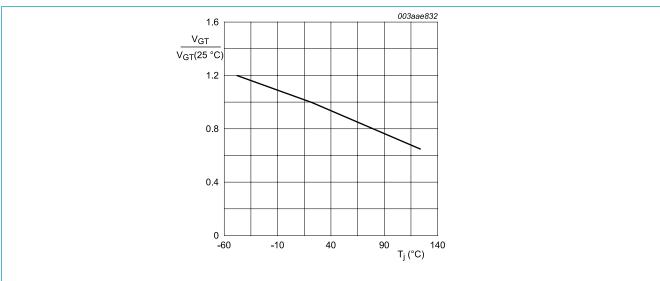
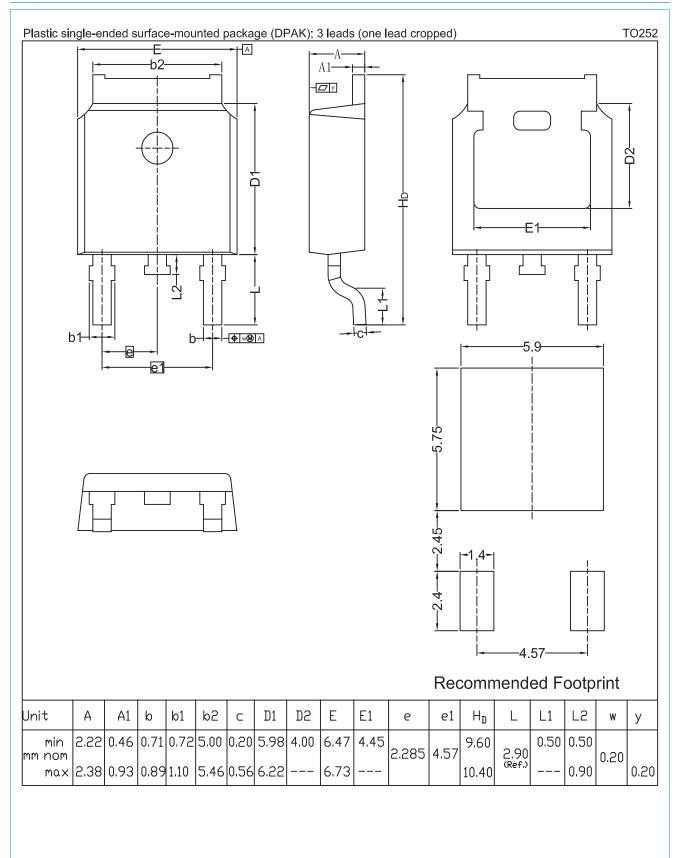


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

# 11. Package outline



## 12. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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**4Q Triac** 

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