Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT404 plastic package. This "series E" triac balances the requirements of commutation performance and gate sensitivity. The "sensitive gate" "series E" is intended for interfacing with low power drivers including microcontrollers.

2. Features and benefits

- · 3Q technology for improved noise immunity
- Direct interfacing with low power drivers and microcontrollers
- · Good immunity to false turn-on by dV/dt
- · High commutation capability with sensitive gate
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Surface mountable package
- · Triggering in three quadrants only

3. Applications

- Electronic thermostats (heating and cooling)
- · High power motor controls e.g. washing machines and vacuum cleaners

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DRM}	repetitive peak off- state voltage		-	-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{mb} \le 101 ^{\circ}\text{C}$; Fig. 1; Fig. 2; Fig. 3	-	-	16	Α
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 20 \text{ ms}$; Fig. 4; Fig. 5	-	-	140	Α
		full sine wave; $T_{j(init)} = 25 \text{ °C}$; $t_p = 16.7 \text{ ms}$	-	-	150	Α
Tj	junction temperature		-	-	125	°C
Static characte	eristics					
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	10	mA
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ \text{ G-};$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	10	mA

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
		$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 \text{ °C}; \frac{\text{Fig. 7}}{}$	-	-	10	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	15	mA
V _T	on-state voltage	I _T = 18 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.3	1.5	V
Dynamic cl	haracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit	60	-	-	V/µs
dI _{com} /dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit	5	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 10 V/ μ s; gate open circuit	8	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 1 V/ μ s; gate open circuit	12	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	mb	T2——T1
2	T2	main terminal 2		G sym051
3	G	gate		Symost
mb	T2	mounting base; main terminal 2	D2PAK (SOT404)	

6. Ordering information

Table 3. Ordering information

Type number	Package	e				
	Name	Description	Version			
BTA316B-800E	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404			

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; $T_{mb} \le 101 ^{\circ}\text{C}$; Fig. 1; Fig. 2; Fig. 3	-	16	А
I _{TSM}	non-repetitive peak on- state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5	-	140	А
		full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms	-	150	Α
l ² t	I ² t for fusing	t _p = 10 ms; SIN	-	98	A²s
dl _T /dt	rate of rise of on-state current	I _G = 20 mA	-	100	A/µs
I _{GM}	peak gate current		-	2	Α
P_{GM}	peak gate power		-	5	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.5	W
T _{stg}	storage temperature		-40	150	°C
Tj	junction temperature		-	125	°C

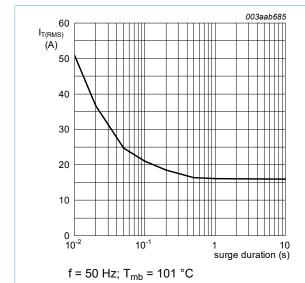


Fig. 1. RMS on-state current as a function of surge duration; maximum values

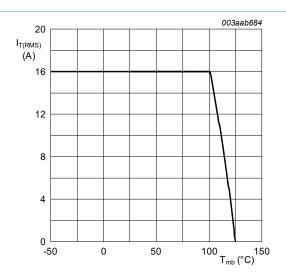


Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values

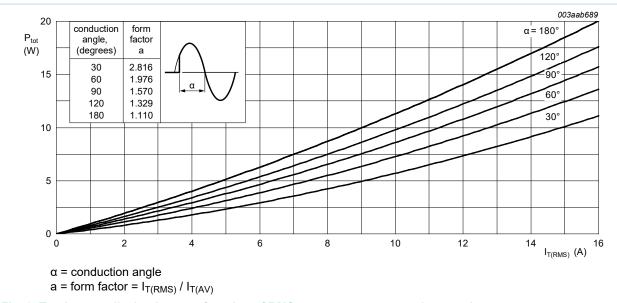


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

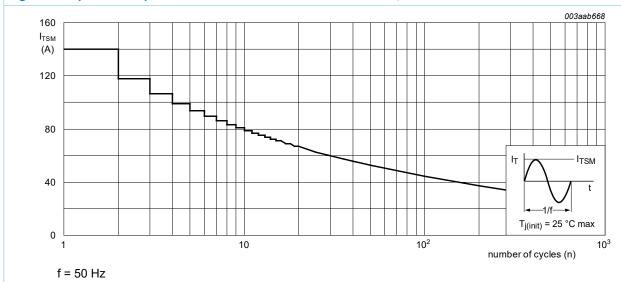
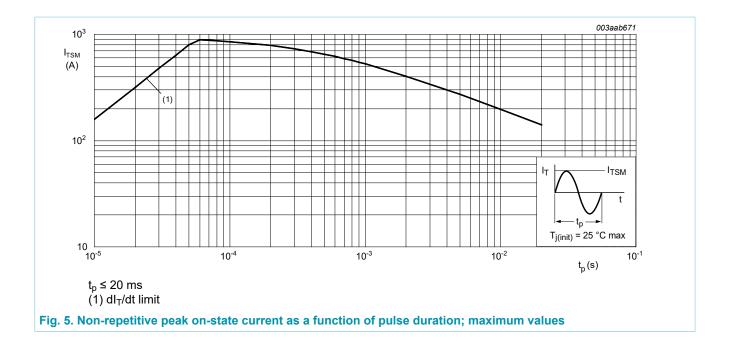


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

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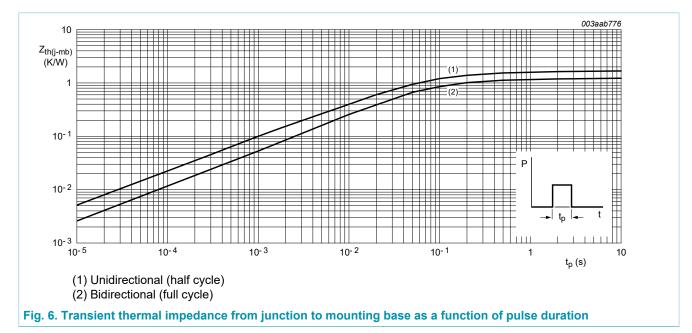
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8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	full cycle; Fig. 6	-	-	1.2	K/W
		half cycle; Fig. 6	-	-	1.7	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted; minimum footprint	-	55	-	K/W



9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static char	acteristics		,			,
I _{GT}	gate trigger current	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 7$	-	-	10	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; } T2 + G-;$ $T_j = 25 \text{ °C; } Fig. 7$	-	-	10	mA
		$V_D = 12 \text{ V; } I_T = 0.1 \text{ A; T2- G-;}$ $T_j = 25 \text{ °C; } Fig. 7$	-	-	10	mA
IL	latching current	$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; T2+ G+;$ $T_j = 25 \text{ °C}; Fig. 8$	-	-	25	mA
		$V_D = 12 \text{ V; } I_G = 0.1 \text{ A; } T2+ \text{ G-;}$ $T_j = 25 \text{ °C; } \underline{\text{Fig. 8}}$	-	-	30	mA
		$V_D = 12 \text{ V}; I_G = 0.1 \text{ A}; \text{ T2- G-};$ $T_j = 25 ^{\circ}\text{C}; \text{ Fig. 8}$	-	-	30	mA
I _H	holding current	V _D = 12 V; T _j = 25 °C; <u>Fig. 9</u>	-	-	15	mA
V _T	on-state voltage	I _T = 18 A; T _j = 25 °C; <u>Fig. 10</u>	-	1.3	1.5	V
V _{GT}	gate trigger voltage	$V_D = 12 \text{ V}; I_T = 0.1 \text{ A}; T_j = 25 \text{ °C};$ Fig. 11	-	0.8	1	V
		V _D = 400 V; I _T = 0.1 A; T _j = 125 °C; Fig. 11	0.25	0.4	-	V
I _D	off-state current	V _D = 800 V; T _j = 125 °C	-	0.1	0.5	mA
Dynamic cl	haracteristics					
dV _D /dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit	60	-	-	V/µs
dl _{com} /dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 20 V/ μ s; (snubberless condition); gate open circuit	5	-	-	A/ms
		V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 10 V/µs; gate open circuit	8	-	-	A/ms
		$V_D = 400 \text{ V}; T_j = 125 ^{\circ}\text{C}; I_{T(RMS)} = 16 \text{ A};$ $dV_{com}/dt = 1 \text{ V}/\mu\text{s}; gate open circuit}$	12	-	-	A/ms

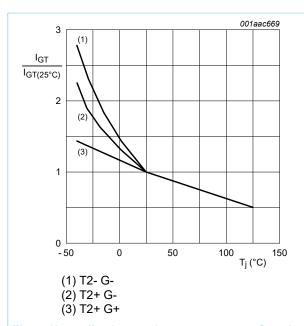


Fig. 7. Normalized gate trigger current as a function of junction temperature

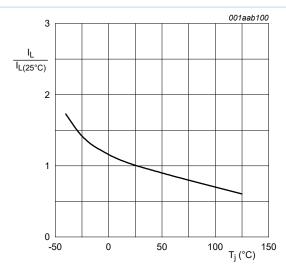


Fig. 8. Normalized latching current as a function of junction temperature

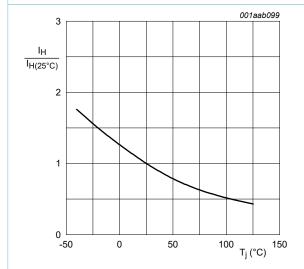
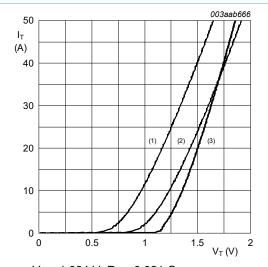


Fig. 9. Normalized holding current as a function of junction temperature

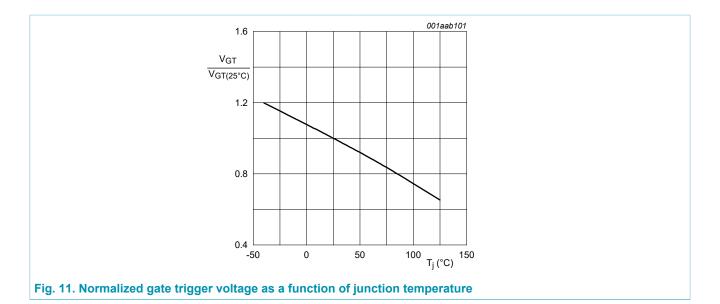


 V_o = 1.024 V; R_s = 0.021 Ω (1) T_j = 125 °C; typical values (2) T_j = 125 °C; maximum values (3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

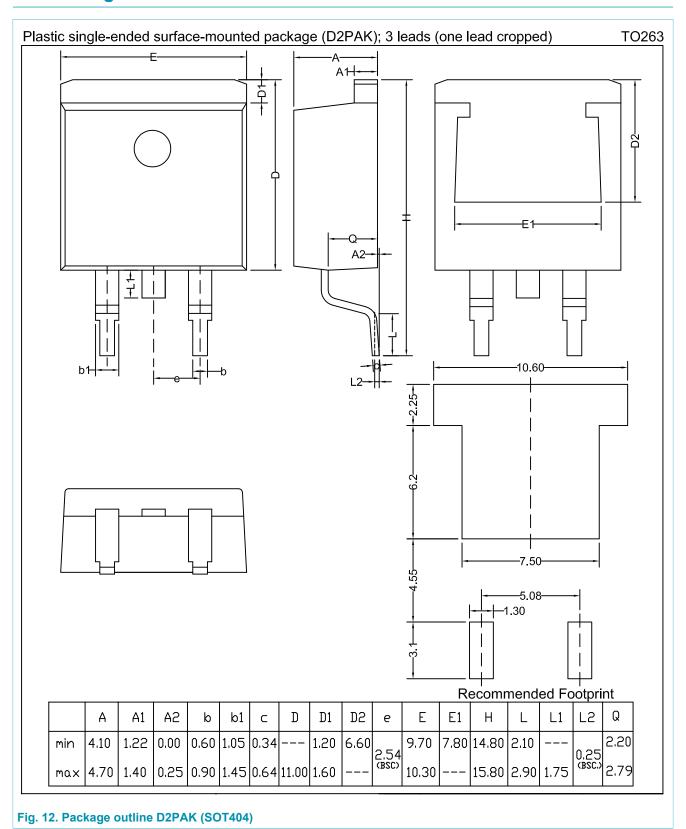
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10. Package outline



11. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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