BTA316X-800CT

3Q Triac

Rev.02 - 12 September 2018 Product data sheet

1. General description

Planar passivated high commutation three quadrant triac in a SOT186A "full pack" plastic package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series CT" triac will commutate the full RMS current at the maximum rated junction temperature ($T_{j(max)}$ = 150 °C) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High junction operating temperature capability ($T_{j(max)}$ = 150 °C)
- High immunity to false turn-on by dV/dt
- High voltage capability
- Isolated mounting base package
- Less sensitive gate for very high noise immunity
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only

3. Applications

- Applications subject to high temperature ($T_{j(max)}$ = 150 °C)
- Electronic thermostats
- High power motor controls e.g. washing machines and vacuum cleaners
- Rectifier-fed DC inductive loads e.g. DC motors and solenoids
- Refrigeration and air conditioning compressor

4. Quick reference data

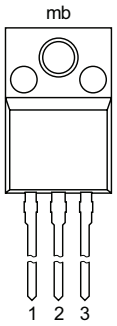
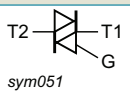
Table 1. Quick reference data

Symbol	Parameter	Conditions	Values	Unit
Absolute maximum rating				
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 67$ °C; Fig. 1; Fig. 2; Fig. 3	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; t_p = 20 ms; $T_{j(init)}$ = 25 °C; Fig. 4; Fig. 5	140	A
		full sine wave; t_p = 16.7 ms; $T_{j(init)}$ = 25 °C	150	A
T_j	junction temperature		150	°C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+ T_j = 25 °C; Fig. 7		2	-	35	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G- T_j = 25 °C; Fig. 7		2	-	35	mA
		V_D = 12 V; I_T = 0.1 A; T2- G- T_j = 25 °C; Fig. 7		2	-	35	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	-	35	mA
V_T	on-state voltage	I_T = 18 A; T_j = 25 °C; Fig. 10		-	1.3	1.5	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		500	-	-	V/µs
		V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		200	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 20 V/µs; gate open circuit; snubberless condition		8	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1		
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BTA316X-800CT	TO-220F	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 'full pack'	SOT186A

7. Marking

Table 4. Marking codes

Type number	Marking codes
BTA316X-800CT	BTA316X-800CT

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Values	Unit
V_{DRM}	repetitive peak off-state voltage		800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 67$ °C; Fig. 1; Fig. 2; Fig. 3	16	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; t_p = 20 ms; $T_{j(init)}$ = 25 °C; Fig. 4; Fig. 5	140	A
		full sine wave; t_p = 16.7 ms; $T_{j(init)}$ = 25 °C	150	A
I^2t	I^2t for fusing	t_p = 10ms; sine wave	98	A^2s
dI_T/dt	rate of rise of on-state current	I_G = 70mA	100	A/µs
I_{GM}	peak gate current		2	A
P_{GM}	peak gate power		5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	0.5	W
T_{stg}	storage temperature		-40 to 150	°C
T_j	junction temperature		150	°C

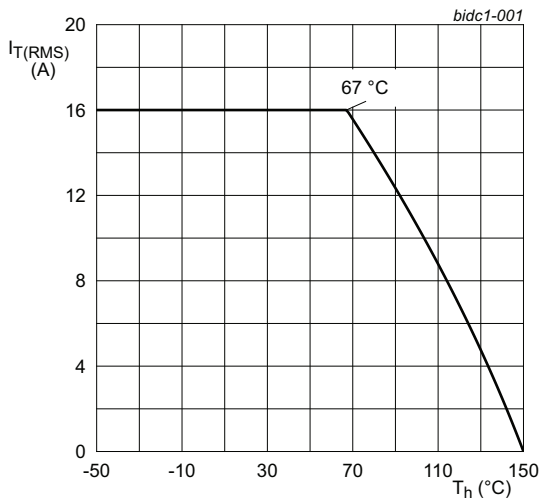
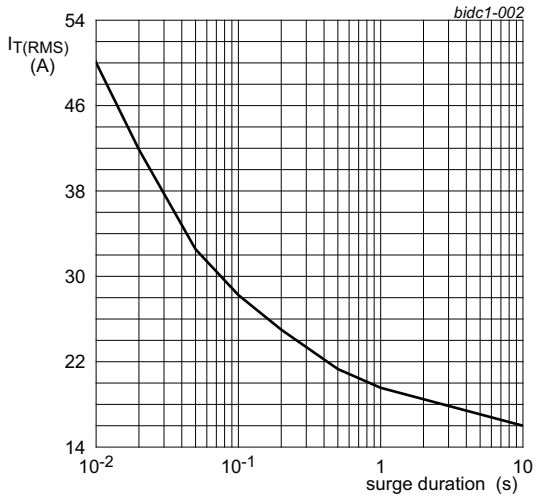
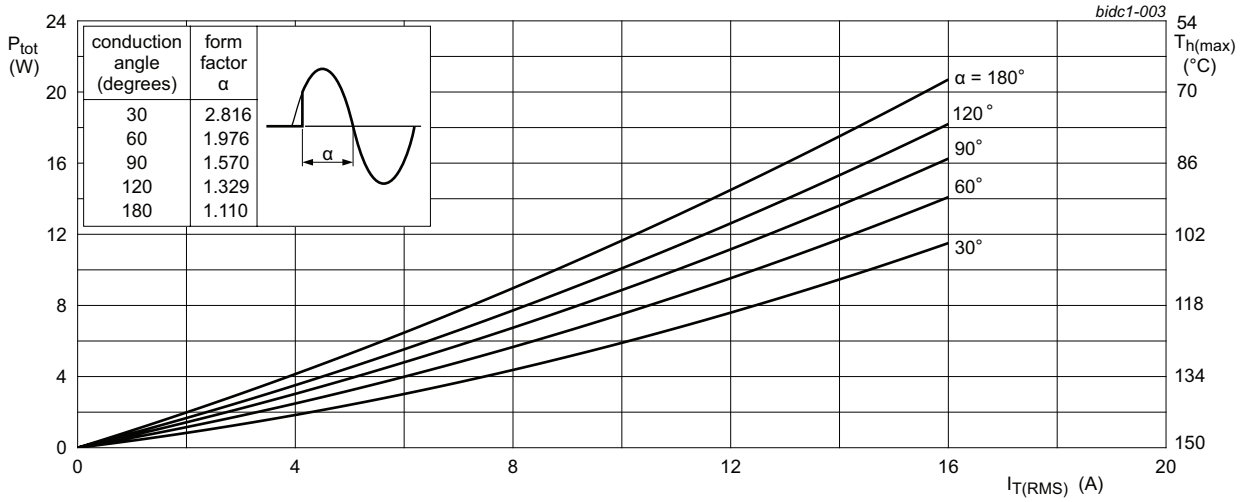


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values



f = 50Hz; T_h = 67 °C

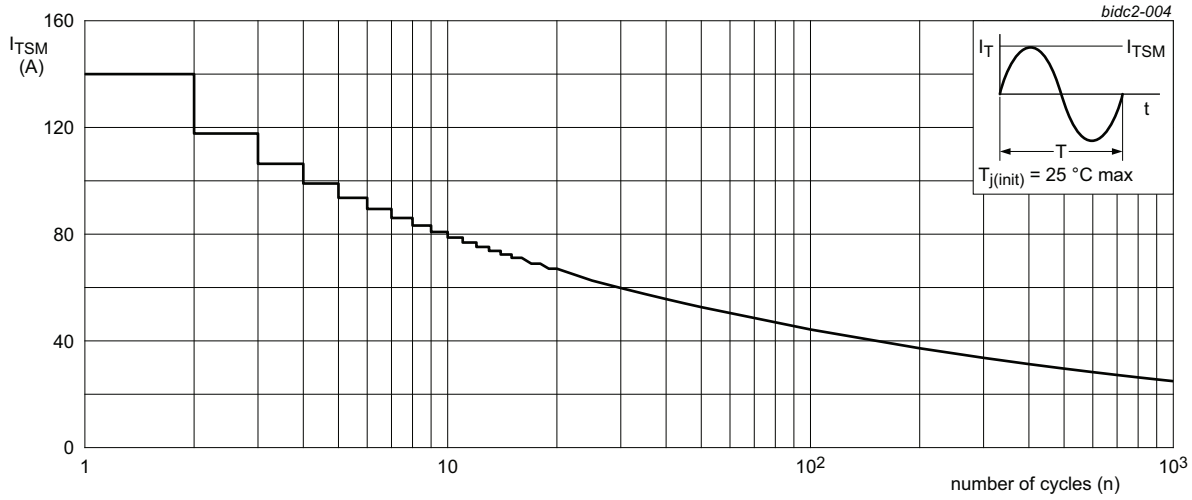
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

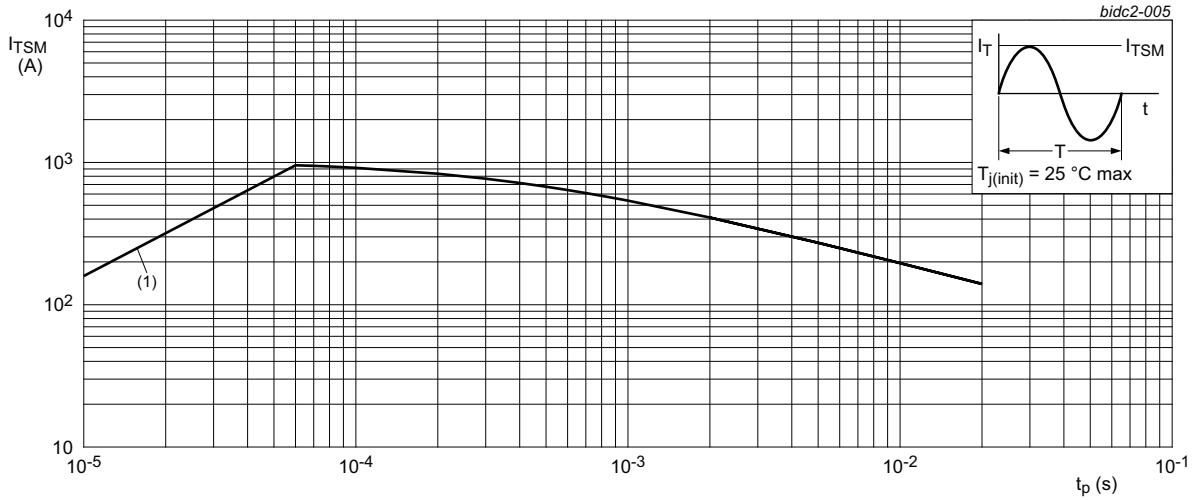
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms ;

(1) dI_T/dt limit

Fig. 5. Total power dissipation as a function of RMS on-state current; maximum values

9. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 6		-	-	4	K/W
		without heatsinkcompound; Fig. 6		-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	55	-	K/W

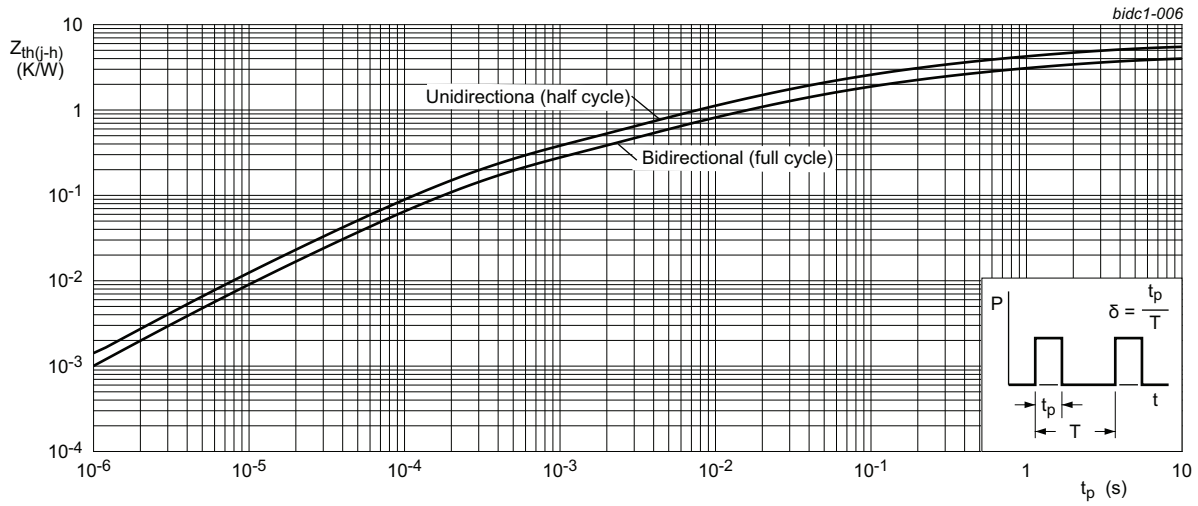


Fig. 6. Transient thermal impedance from junction to heatsink as a function of pulse duration

10. Isolation characteristics

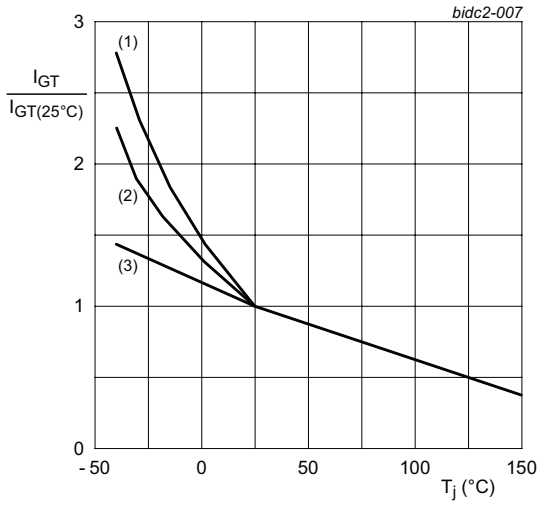
Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	50 Hz ≤ f ≤ 60 Hz; RH ≤ 65 %; from all pins to external heatsink; sinusoidal waveform; clean and dust free		-	-	2500	V
C_{isol}	isolation capacitance	from cathode to external heatsink		-	10	-	PF

11. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 7		2	-	35	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 7		2	-	35	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 7		2	-	35	mA
I_L	latching current	V_D = 12 V; I_T = 0.1 A; T2+ G+; T_j = 25 °C; Fig. 8		-	-	50	mA
		V_D = 12 V; I_T = 0.1 A; T2+ G-; T_j = 25 °C; Fig. 8		-	-	60	mA
		V_D = 12 V; I_T = 0.1 A; T2- G-; T_j = 25 °C; Fig. 8		-	-	50	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	-	35	mA
V_T	on-state voltage	I_T = 18 A; T_j = 25 °C; Fig. 10		-	1.3	1.5	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.8	1	V
		V_D = 400 V; I_T = 0.1 A; T_j = 150 °C; Fig. 11		0.25	0.4	-	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	10	µA
		V_D = 800 V; T_j = 150 °C		-	-	2	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		500	-	-	V/µs
		V_{DM} = 536 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit		200	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 150 °C; $I_{T(RMS)}$ = 16 A; dV_{com}/dt = 20 V/µs; gate open circuit; snubberless condition		8	-	-	A/ms



(1) T2- G-
(2) T2+ G-
(3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

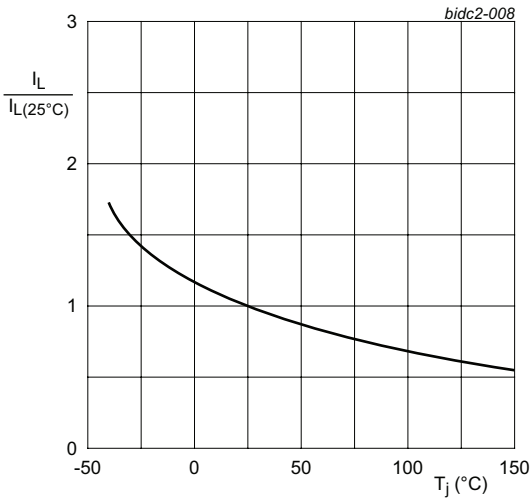


Fig. 8. Normalized latching current as a function of junction temperature

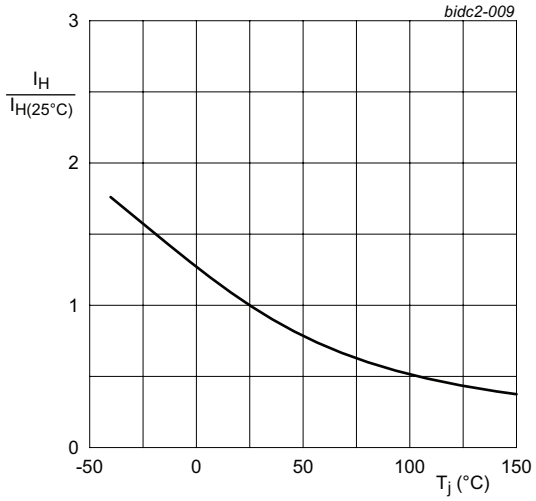
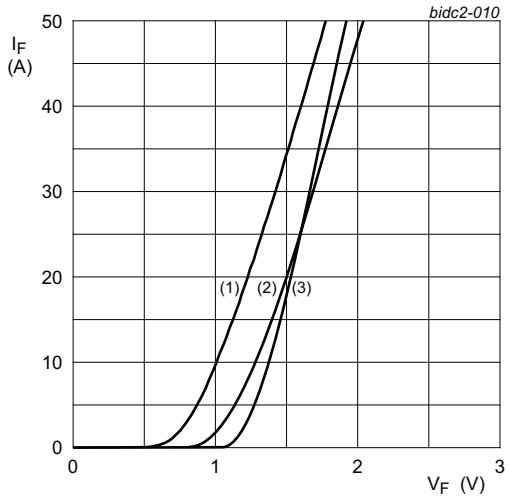


Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.053 V; R_s = 0.0216 Ω
(1) T_j = 150 °C; typical values
(2) T_j = 150 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

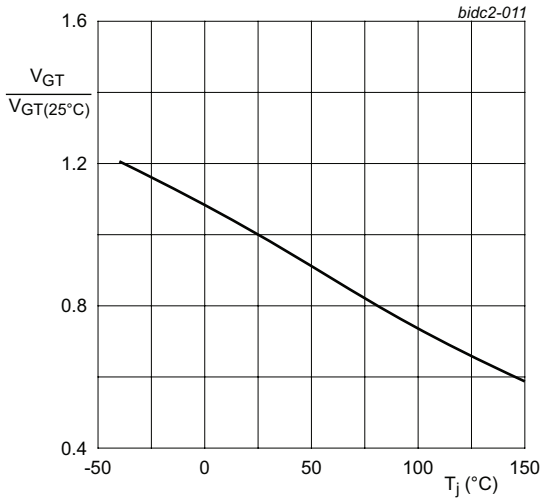
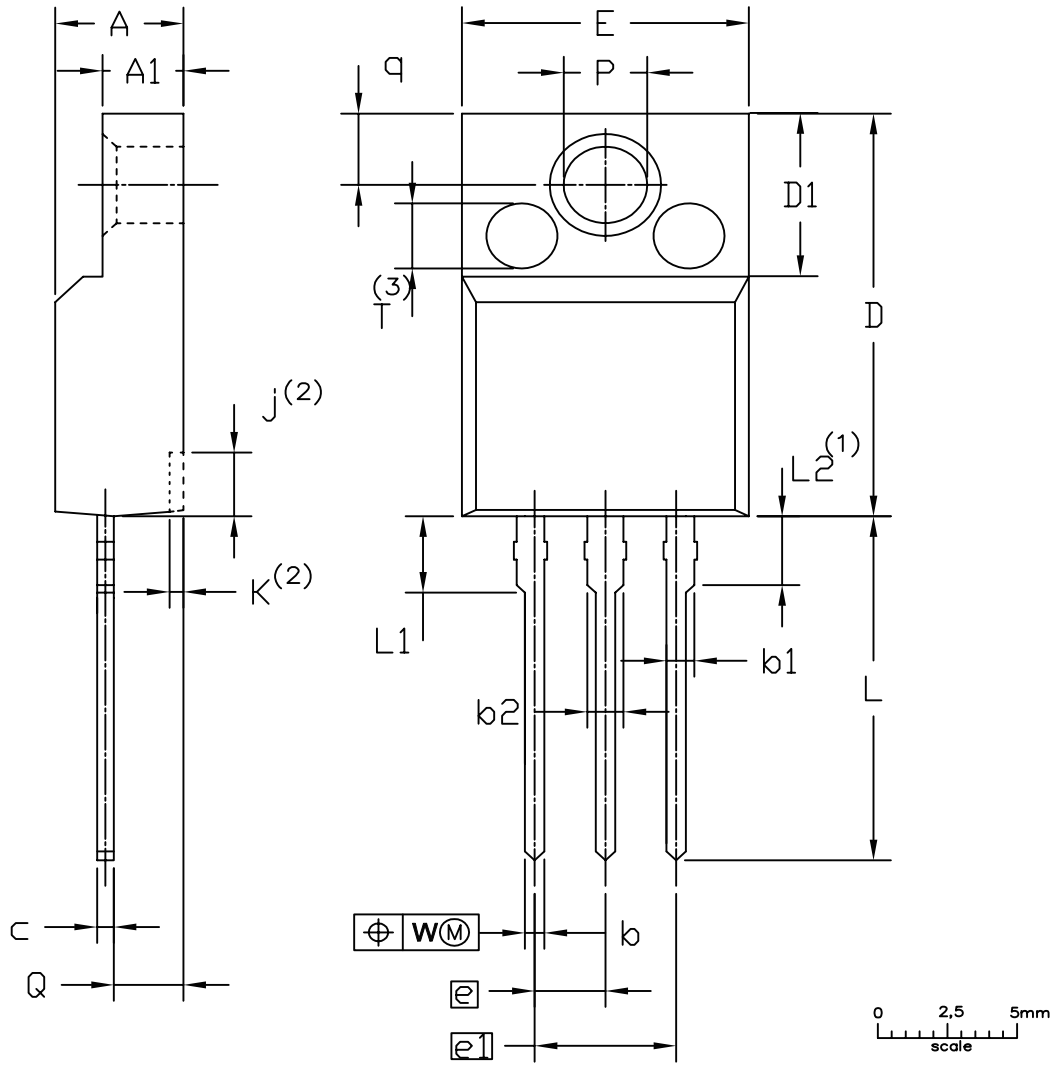


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

12. Package outline

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack" SOT186A



UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j(2)	K(2)	L	L_1	L_2(1) max.	P	Q	q	W	T(3)
mm	4.6	2.9	0.9	1.1	1.4	0.7	15.8	6.5	10.3	2.54	5.08	2.7	0.6	14.4	3.30	3	3.2	2.6	3.0	0.4	2.5
	4.0	2.5	0.7	0.9	1.0	0.4	15.2	6.3	9.7			1.7	0.4	13.5	2.79		3.0	2.3	2.6		

Notes
1. Terminal dimensions within this zone are uncotrolled
2. Dot lines area designs may vary
3. Eject pin mark is for reference only

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT186A		3 LEADS TO220F				2013-11-14

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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