

1. General description

Planar passivated high commutation three quadrant triac in a ITO3P package intended for use in circuits where high static and dynamic dV/dt and high dI/dt can occur. This "series BT" triac will commute the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- High current TRIAC
- 3Q technology for improved noise immunity
- High commutation capability with maximum false trigger immunity
- High immunity to false turn-on by dV/dt
- High junction operating temperature capability ($T_{j(max)} = 150\text{ °C}$)
- High voltage capability
- Least sensitive gate for highest noise immunity
- Low thermal resistance
- Planar passivated for voltage ruggedness and reliability
- Triggering in three quadrants only
- Insulated tab rated at 2500Vrms

3. Applications

- High current / high surge applications
- High power / industrial controls - e.g. heating, motors, lighting

4. Quick reference data

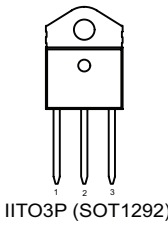
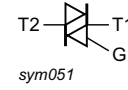
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5	-	-	250	A
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 121\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	25	A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I _{GT}	gate trigger current	V _D = 12 V; I _T = 0.1 A; T2+ G+; T _j = 25 °C; Fig. 7	-	-	50	mA
		V _D = 12 V; I _T = 0.1 A; T2+ G-; T _j = 25 °C; Fig. 7	-	-	50	mA
		V _D = 12 V; I _T = 0.1 A; T2- G-; T _j = 25 °C; Fig. 7	-	-	50	mA
Dynamic characteristics						
dV _D /dt	rate of rise of off-state voltage	V _{DM} = 536 V; T _j = 150 °C; (V _{DM} = 67% of V _{DRM}); exponential waveform; gate open circuit	2000	-	-	V/μs
dI _{com} /dt	rate of change of commutating current	V _D = 400 V; T _j = 150 °C; I _{T(RMS)} = 25 A; dV _{com} /dt = 20 V/μs; (snubberless condition); gate open circuit	15	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p>IITO3P (SOT1292)</p>	 <p>sym051</p>
2	T2	main terminal 2		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package Name	Orderable part number	Packing method	Small packing quantity	Package version	Package issue date
BTA425Z-800BT	IITO3P	BTA425Z-800BTQ	Tube	30	SOT1292	21-Jun-2017

7. Marking

Table 4. Marking codes

Type number	Marking codes
BTA425Z-800BT	BTA425Z 800BT

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 121\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	25	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 20\text{ ms}$; Fig 4 ; Fig 5	-	250	A
		full sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 16.7\text{ ms}$	-	275	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	340	A ² s
di_T/dt	rate of rise of on-state current	$I_G = 0.1\text{ A}$	-	100	A/ μ s
I_{GM}	peak gate current		-	4	A
P_{GM}	peak gate power		-	10	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	1	W
T_{stg}	storage temperature		-40	150	°C
T_j	junction temperature		-	150	°C

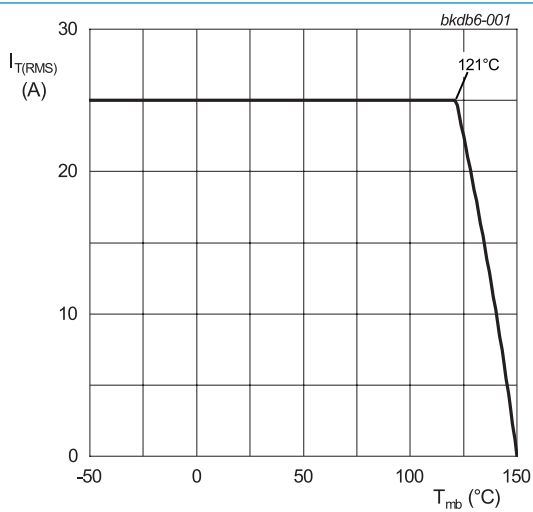


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values

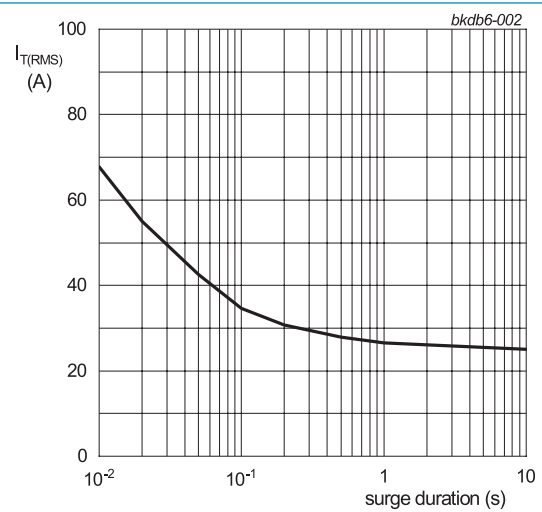


Fig. 2. RMS on-state current as a function of surge duration; maximum values
 $f = 50\text{ Hz}$; $T_{mb} = 121\text{ °C}$

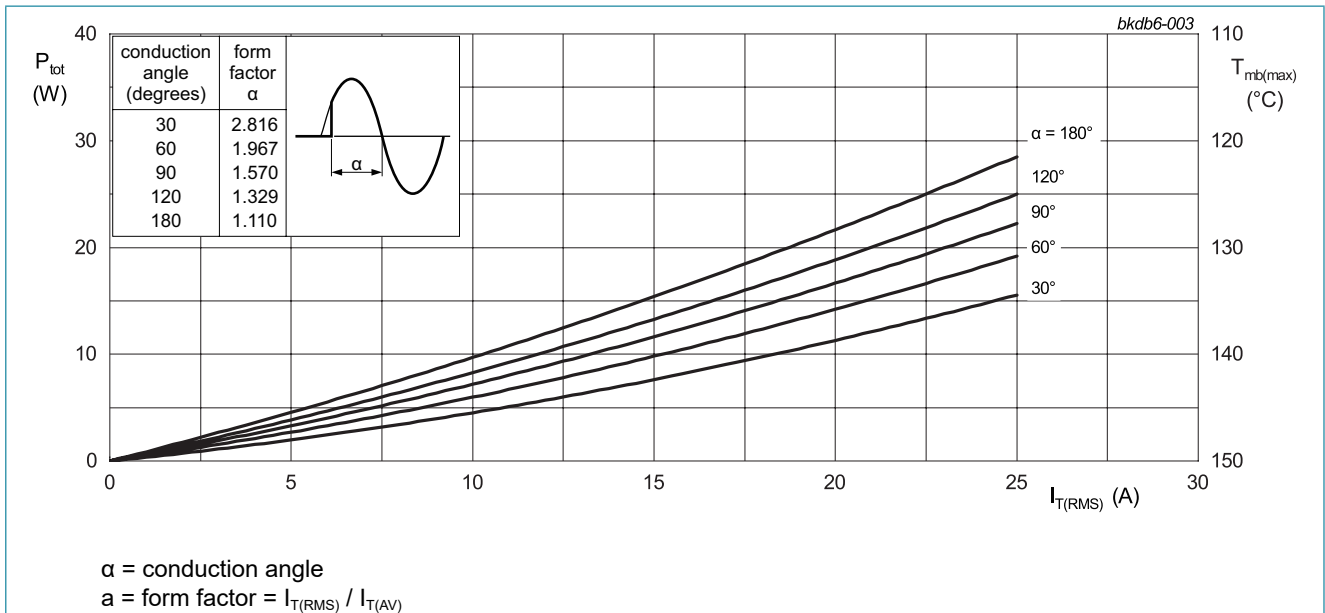


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

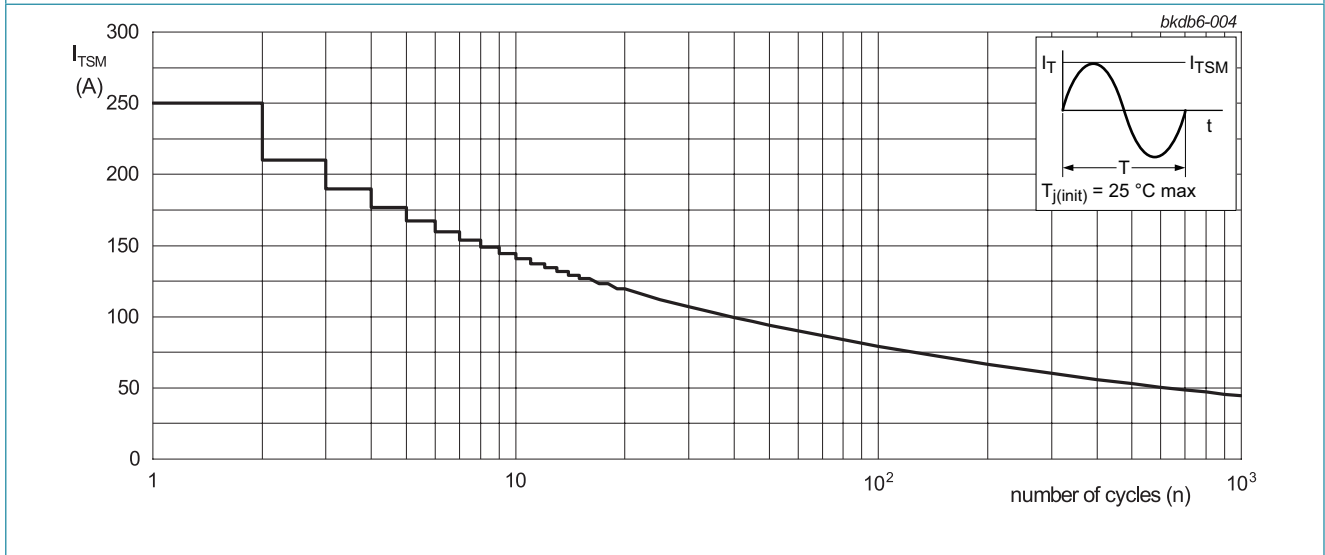
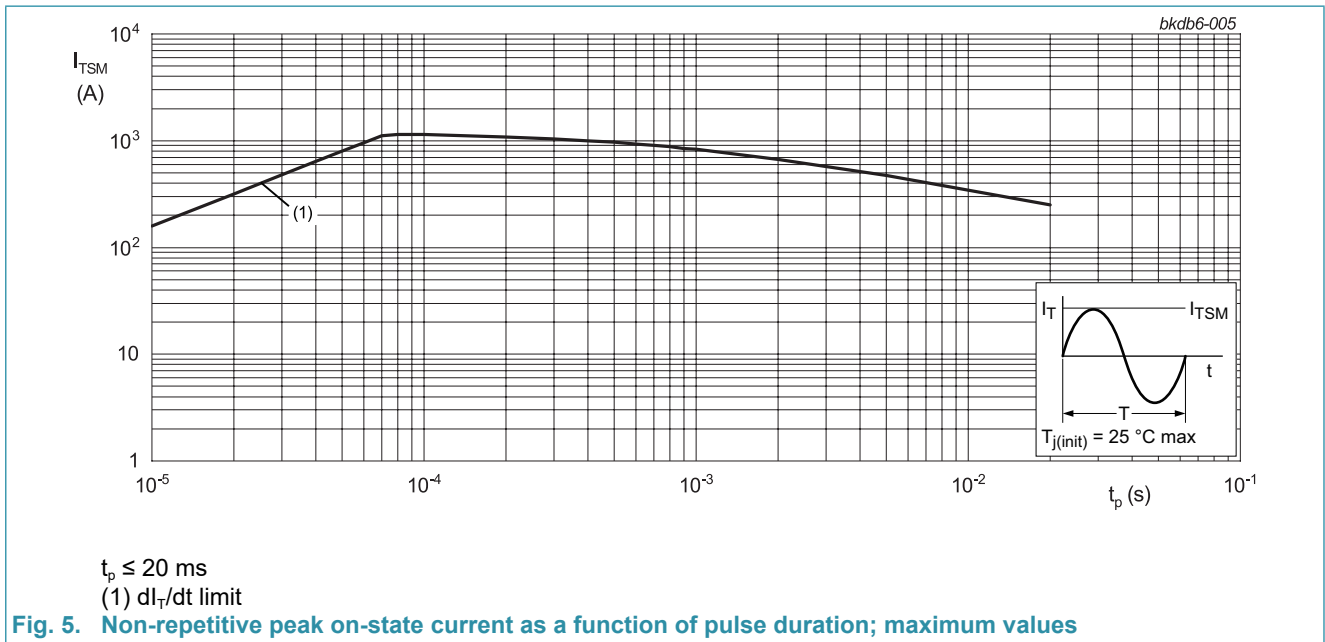


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	full cycle; with heatsink compound; Fig. 6	-	-	1	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	-	50	-	K/W

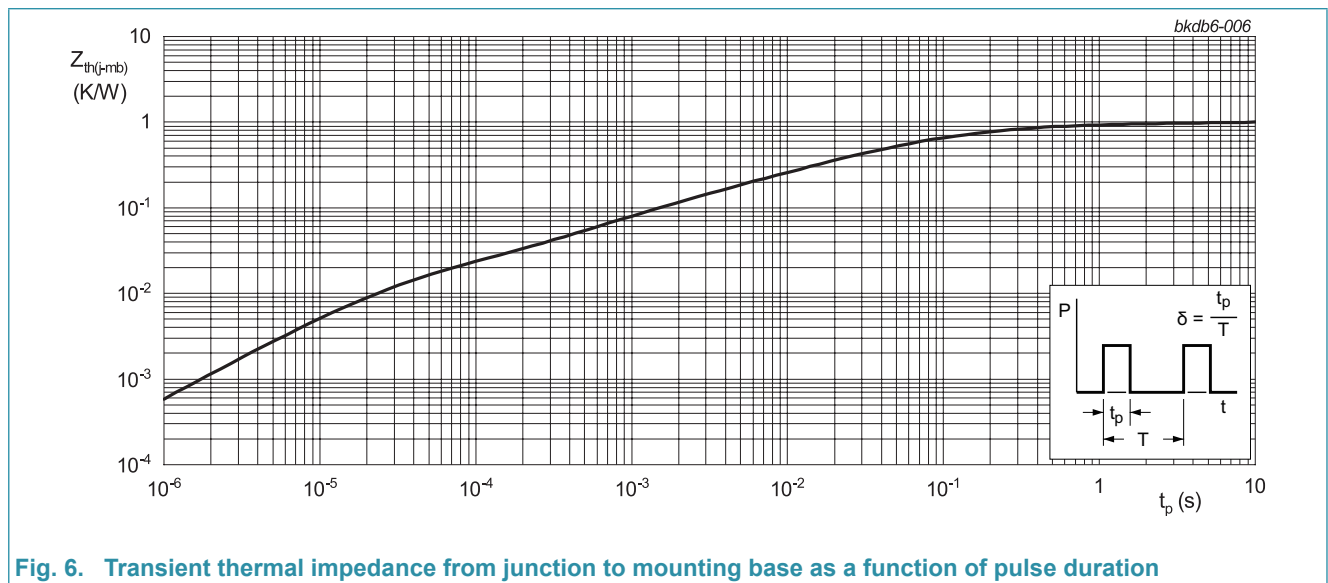


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Isolation characteristics

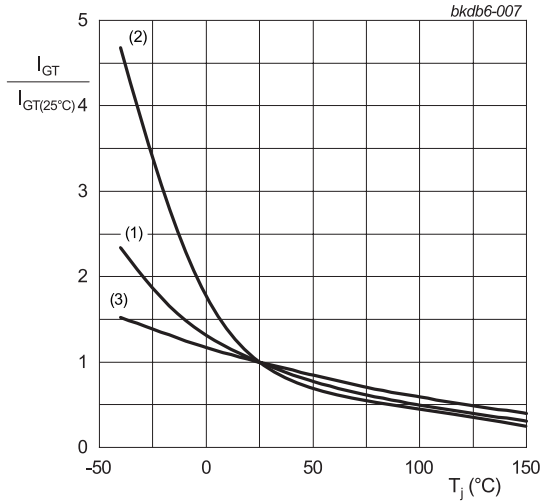
Table 7. Isolation characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $RH \leq 65\%$; $T_h = 25\text{ }^\circ\text{C}$	-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; $f = 1\text{ MHz}$; $T_h = 25\text{ }^\circ\text{C}$	-	10	-	pF

11. Characteristics

Table 8. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G+;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2+ G-;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 7	-	-	50	mA
		$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_2- G-;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 7	-	-	50	mA
I_L	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2+ G+;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	80	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2+ G-;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	100	mA
		$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_2- G-;$ $T_J = 25\text{ }^\circ\text{C};$ Fig. 8	-	-	80	mA
I_H	holding current	$V_D = 12\text{ V}; T_J = 25\text{ }^\circ\text{C};$ Fig. 9	-	-	75	mA
V_T	on-state voltage	$I_T = 35\text{ A}; T_J = 25\text{ }^\circ\text{C};$ Fig. 10	-	1.2	1.4	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_J = 25\text{ }^\circ\text{C};$ Fig. 11	-	0.9	1.3	V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_J = 150\text{ }^\circ\text{C}$	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}; T_J = 25\text{ }^\circ\text{C}$	-	-	5	μA
		$V_D = 800\text{ V}; T_J = 150\text{ }^\circ\text{C}$	-	0.4	2	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}; T_J = 150\text{ }^\circ\text{C}; (V_{DM} = 67\%$ of $V_{DRM});$ exponential waveform; gate open circuit	2000	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}; T_J = 150\text{ }^\circ\text{C}; I_{T(RMS)} = 25\text{ A};$ $dV_{com}/dt = 20\text{ V}/\mu\text{s};$ (snubberless condition); gate open circuit	15	-	-	A/ms



- (1) T2- G-
- (2) T2+ G-
- (3) T2+ G+

Fig. 7. Normalized gate trigger current as a function of junction temperature

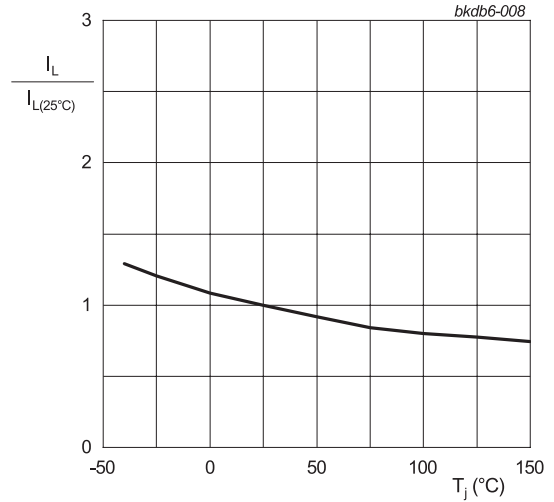


Fig. 8. Normalized latching current as a function of junction temperature

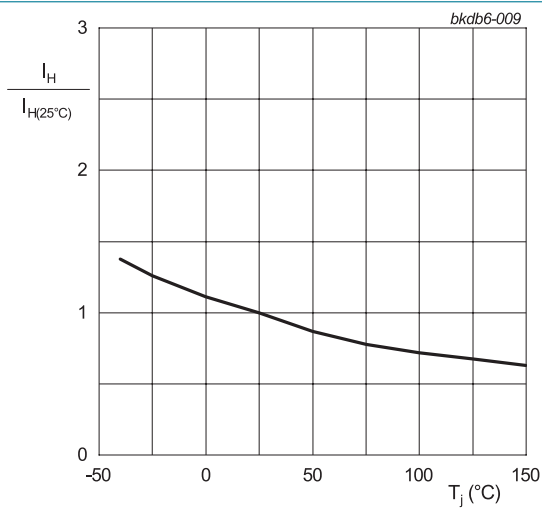
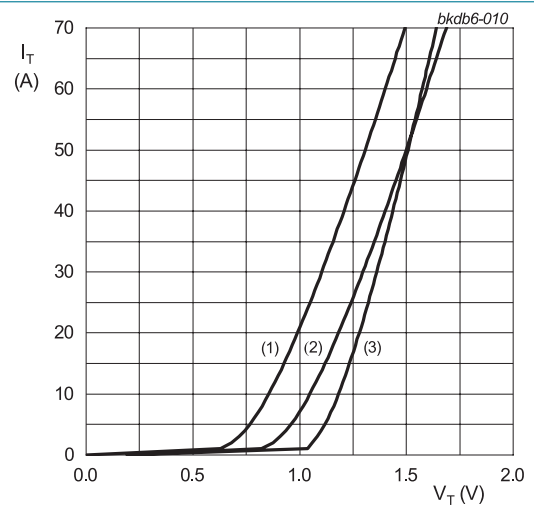


Fig. 9. Normalized holding current as a function of junction temperature



- $V_o = 0.949\text{ V}; R_s = 0.114\ \Omega$
 (1) $T_j = 150^\circ\text{C}$; typical values
 (2) $T_j = 150^\circ\text{C}$; maximum values
 (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 10. On-state current as a function of on-state voltage

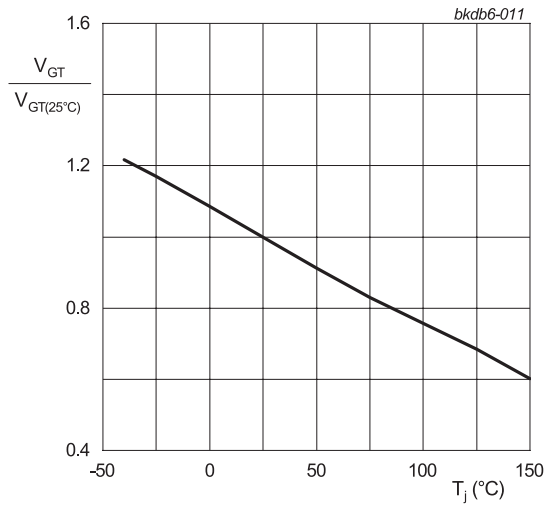
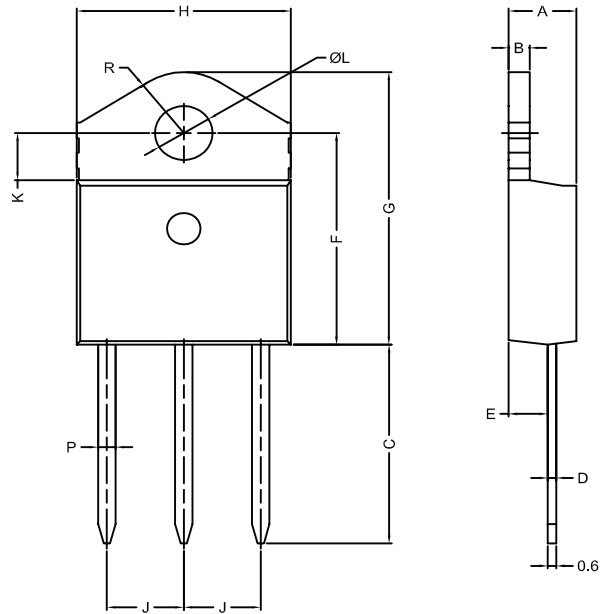


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

12. Package outline

Plastic single-ended through-hole package; isolated heatsink mounted; 1 mounting hole; 3-lead TO3P

SOT1292



Unit		A	B	C	D	E	F	G	H	J	K	L	P	R
mm	min	4.75	1.45	14.35	0.50	2.70	15.80	20.40	15.10	5.40	3.40	4.08	1.20	4.6
	max	4.95	1.55	15.60	0.70	2.90	16.50	21.10	15.50	5.65	3.65	4.17	1.40	4.6 (typ)

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT1292		-				

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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