

## 1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT186A (TO-220F) "full pack" plastic package intended for use in applications requiring high thermal cycling performance and high junction temperature capability ( $T_{j(max)} = 150$  °C).

## 2. Features and benefits

- · High junction operating temperature capability
- High thermal cycling performance
- High voltage capability
- Planar passivated for voltage ruggedness and reliability

## 3. Applications

- Ignition circuits
- Motor control
- Protection circuits e.g. SMPS inrush current
- Voltage regulation

## 4. Quick reference data

### Table 1. Quick reference data

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>RRM</sub>	repetitive peak reverse voltage		-	-	600	V
I <sub>T(AV)</sub>	average on-state current	half sine wave; T <sub>h</sub> ≤ 81 °C; <u>Fig. 1</u>	-	-	10.2	A
I <sub>T(RMS)</sub>	RMS on-state current	half sine wave; T <sub>h</sub> ≤ 81 °C; <u>Fig. 2;</u> <u>Fig. 3</u>	-	-	16	A
I <sub>TSM</sub>	non-repetitive peak on- state current	half sine wave; T <sub>j(init)</sub> = 25 °C; t <sub>p</sub> = 10 ms; <u>Fig. 4; Fig. 5</u>	-	-	180	A
		half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 8.3 ms	-	-	198	A
Тj	junction temperature		-	-	150	°C
Static charact	eristics					
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	-	15	mA
Dynamic char	acteristics	·				
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; T <sub>j</sub> = 150 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit	500	-	-	V/µs

## 5. Pinning information

Table 2.	Pinning in	formation		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	К	cathode	mb	А- <del>Ы</del> -К
2	А	anode		Ğ sym037
3	G	gate		Symoor
mb	n.c.	mounting base; isolated	TO-220F (SOT186A)	

# 6. Ordering information

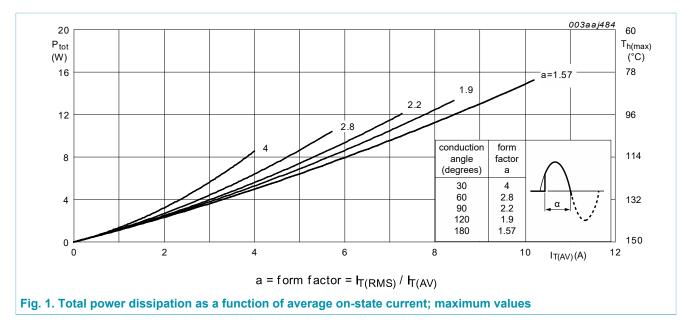
Table 3. Ordering information							
Type number	Package	ckage					
	Name	Description	Version				
TYN16X-600CT	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A				

## 7. Limiting values

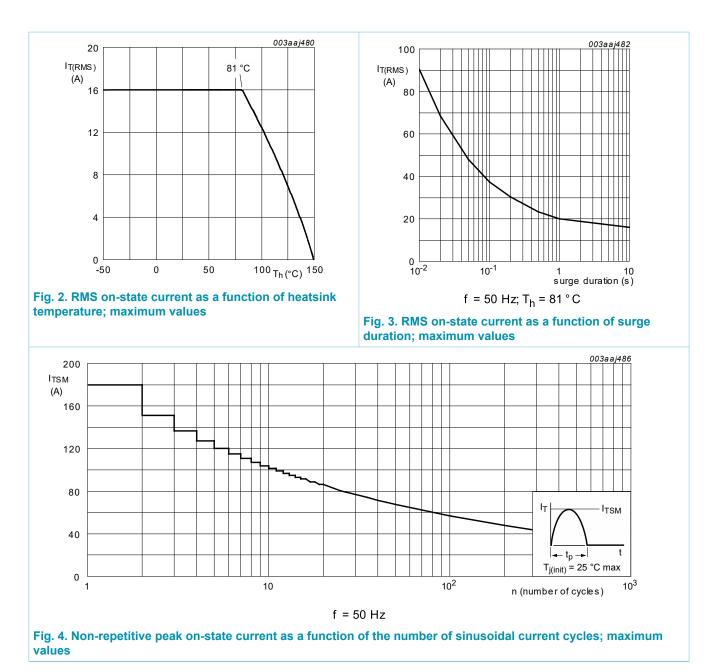
### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DRM</sub>	repetitive peak off-state voltage		-	600	V
V <sub>RRM</sub>	repetitive peak reverse voltage		-	600	V
I <sub>T(AV)</sub>	average on-state current	half sine wave; T <sub>h</sub> ≤ 81 °C; <u>Fig. 1</u>	-	10.2	А
I <sub>T(RMS)</sub>	RMS on-state current	half sine wave; $T_h \le 81 \text{ °C}$ ; Fig. 2; Fig. 3	-	16	А
I <sub>TSM</sub>	non-repetitive peak on- state current	half sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 10 ms; Fig. 4; Fig. 5	-	180	A
		half sine wave; $T_{j(init)} = 25 \text{ °C}$ ; $t_p = 8.3 \text{ ms}$	-	198	А
l <sup>2</sup> t	I <sup>2</sup> t for fusing	t <sub>p</sub> = 10 ms; SIN	-	162	A²s
dl <sub>T</sub> /dt	rate of rise of on-state current	I <sub>G</sub> = 30 mA	-	50	A/µs
I <sub>GM</sub>	peak gate current		-	4	А
V <sub>RGM</sub>	peak reverse gate voltage		-	5	V
P <sub>GM</sub>	peak gate power		-	10	W
P <sub>G(AV)</sub>	average gate power	over any 20 ms period	-	1	W
T <sub>stg</sub>	storage temperature		-40	150	°C
Tj	junction temperature		-	150	°C

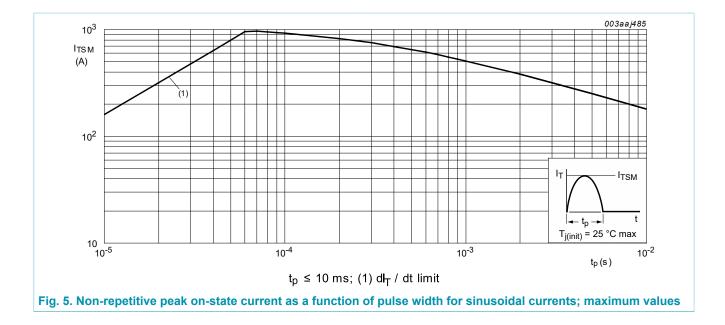


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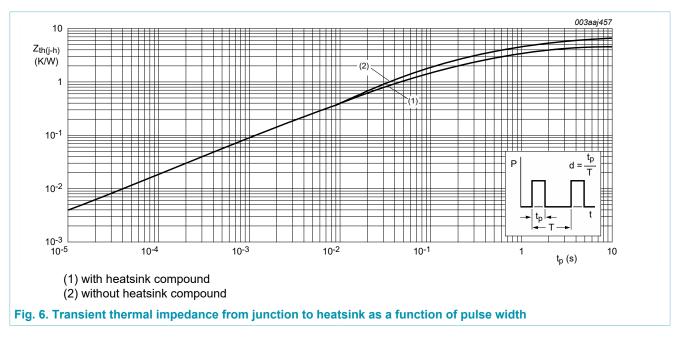


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### 8. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	with heatsink compound; Fig. 6	-	-	4.5	K/W
		without heatsink compound; Fig. 6	-	-	6.5	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient free air	in free air	-	55	-	K/W



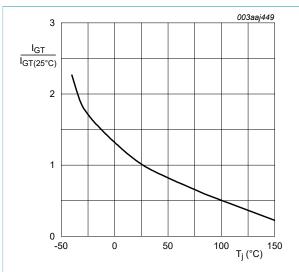
## 9. Isolation characteristics

### Table 6. Isolation characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>isol(RMS)</sub>	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; 50 Hz $\leq$ f $\leq$ 60 Hz; RH $\leq$ 65 %; T <sub>h</sub> = 25 °C	-	-	2500	V
C <sub>isol</sub>	isolation capacitance	from anode to external heatsink; f = 1 MHz; T <sub>h</sub> = 25 °C	-	10	-	pF

## **10. Characteristics**

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 25 °C; <u>Fig. 7</u>	-	-	15	mA
IL	latching current	V <sub>D</sub> = 12 V; I <sub>G</sub> = 0.1 A; T <sub>j</sub> = 25 °C; <u>Fig. 8</u>	-	-	60	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <u>Fig. 9</u>	-	-	40	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 32 A; T <sub>j</sub> = 25 °C; <u>Fig. 10</u>	-	1.2	1.6	V
V <sub>GT</sub>	gate trigger voltage	V <sub>D</sub> = 12 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 25 °C; Fig. 11	-	0.7	1.3	V
		$V_D$ = 400 V; I <sub>T</sub> = 0.1 A; T <sub>j</sub> = 150 °C; Fig. 11	0.2	0.4	-	V
ID	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 150 °C	-	0.2	1	mA
I <sub>R</sub>	reverse current	V <sub>R</sub> = 600 V; T <sub>j</sub> = 150 °C	-	0.2	1	mA
Dynamic ch	aracteristics					
dV <sub>D</sub> /dt	rate of rise of off-state voltage	$V_{DM}$ = 402 V; T <sub>j</sub> = 150 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit	500	-	-	V/µs
t <sub>gt</sub>	gate-controlled turn-on time	$I_{TM}$ = 40 A; V <sub>D</sub> = 600 V; I <sub>G</sub> = 100 mA; dI <sub>G</sub> /dt = 5 A/µs; T <sub>j</sub> = 25 °C	-	2	-	μs
t <sub>q</sub>	commutated turn-off time		-	70	-	μs





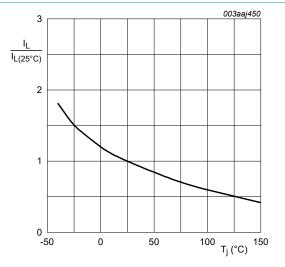
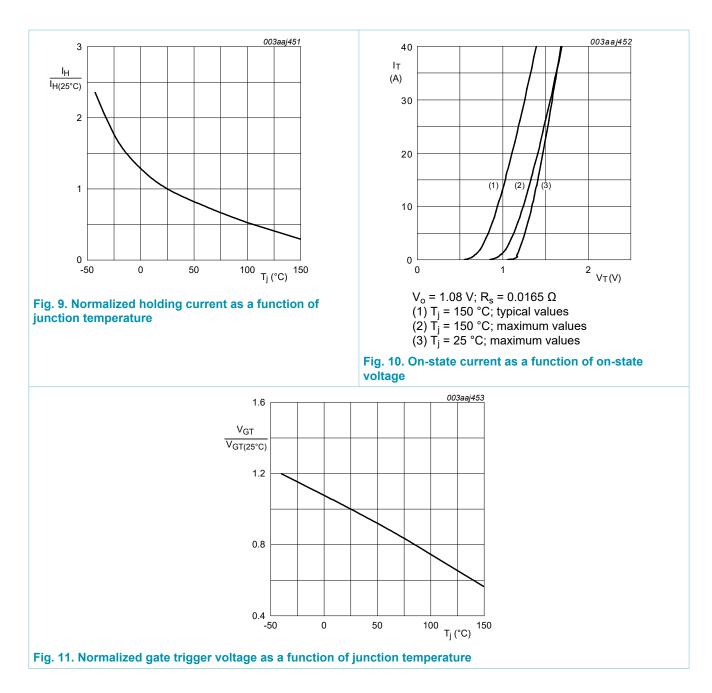


Fig. 8. Normalized latching current as a function of junction temperature

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## 11. Package outline

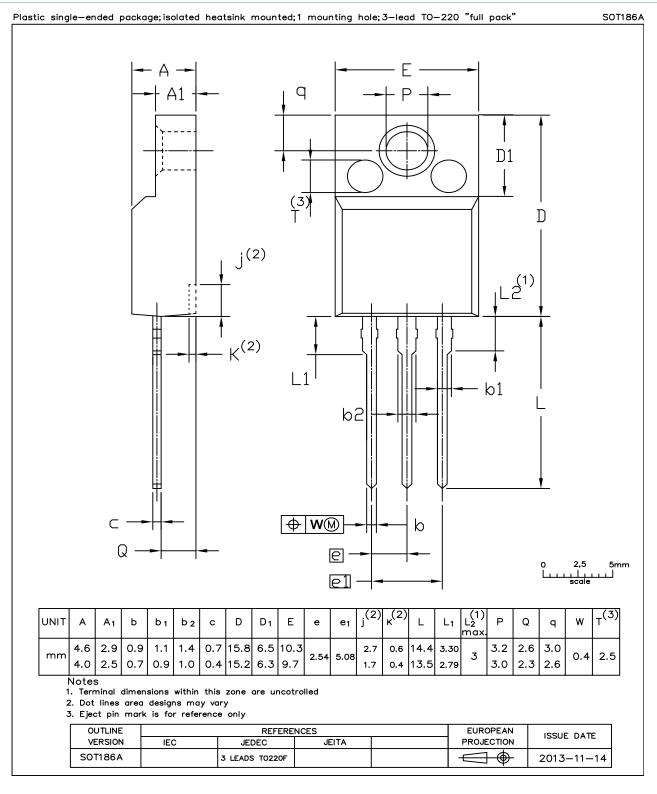


Fig. 12. Package outline TO-220F (SOT186A)

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## 12. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [ <u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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