# Z0109NN0

## 4Q Triac

15 September 2018 Product data sheet

## 1. General description

Planar passivated sensitive gate four quadrant triac in a SOT223 (SC-73) surface-mountable plastic package intended for applications requiring enhanced immunity to noise and direct interfacing to logic level ICs and low power gate drivers.

## 2. Features and benefits

- Direct interfacing to logic level ICs
- Enhanced current surge capability
- Enhanced noise immunity
- High blocking voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate in four quadrants
- Surface-mountable package
- Triggering in all four quadrants

## 3. Applications

- General purpose low power motor control
- Home appliances
- Industrial process control
- Low power AC Fan controllers

## 4. Quick reference data

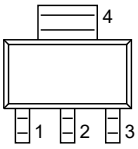
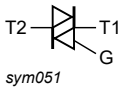
**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq$ 105 °C; Fig. 1; Fig. 2; Fig. 3 | | - | - | 1 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5 | | - | - | 12.5 | A |
| | | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.7 ms | | - | - | 13.8 | A |
| $T_j$ | junction temperature | | | - | - | 125 | °C |
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 9 | | 0.4 | - | 10 | mA |

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 9 | | 0.4 | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 9 | | 0.4 | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G+; $T_j$ = 25 °C; Fig. 9 | | 0.4 | - | 10 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 11 | | - | - | 10 | mA |
| $V_T$ | on-state voltage | $I_T$ = 1.4 A; $T_j$ = 25 °C; Fig. 12 | | - | 1.3 | 1.6 | V |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 110 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit; Fig. 14 | | 120 | - | - | V/µs |
| $dV_{com}/dt$ | rate of change of commutating voltage | $V_D$ = 400 V; $T_j$ = 110 °C; $dI_{com}/dt$ = 0.44 A/ms; gate open circuit | | 2 | - | - | V/µs |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | T1 | main terminal 1 |   SC-73 (SOT223) |   sym051 |
| 2 | T2 | main terminal 2 | | |
| 3 | G | gate | | |
| 4 | T2 | main terminal 2 | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| Z0109NN0 | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{sp} \leq$ 105 °C; Fig. 1; Fig. 2; Fig. 3 | | - | 1 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5 | | - | 12.5 | A |
| | | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 16.7 ms | | - | 13.8 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p$ = 10 ms; SIN | | - | 0.78 | A²s |
| $dI_T/dt$ | rate of rise of on-state current | $I_G$ = 20 mA; T2+ G+ | | - | 50 | A/µs |
| | | $I_G$ = 20 mA; T2+ G- | | - | 50 | A/µs |
| | | $I_G$ = 20 mA; T2- G- | | - | 50 | A/µs |
| | | $I_G$ = 20 mA; T2- G+ | | - | 20 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 1 | A |
| $P_{GM}$ | peak gate power | | | - | 2 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 0.1 | W |
| $T_{stg}$ | storage temperature | | | -40 | 150 | °C |
| $T_j$ | junction temperature | | | - | 125 | °C |

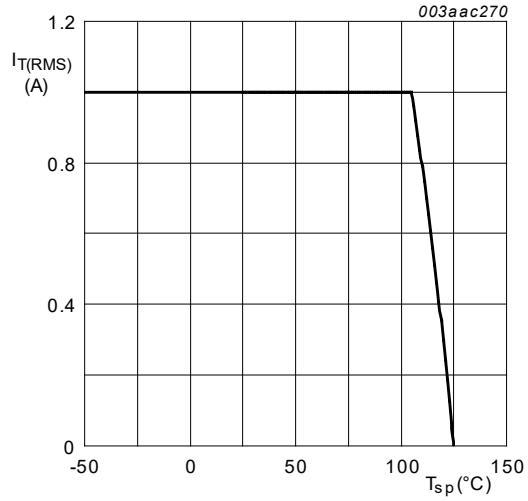
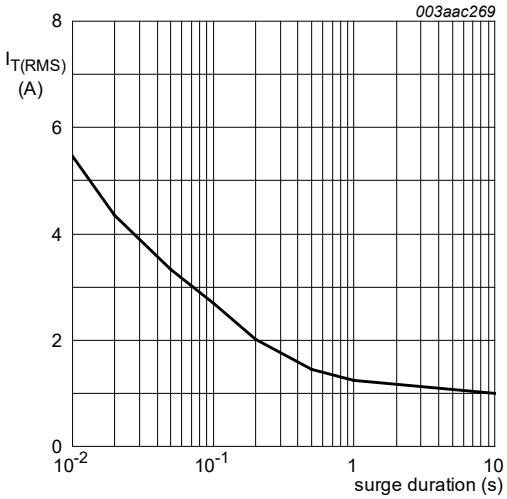
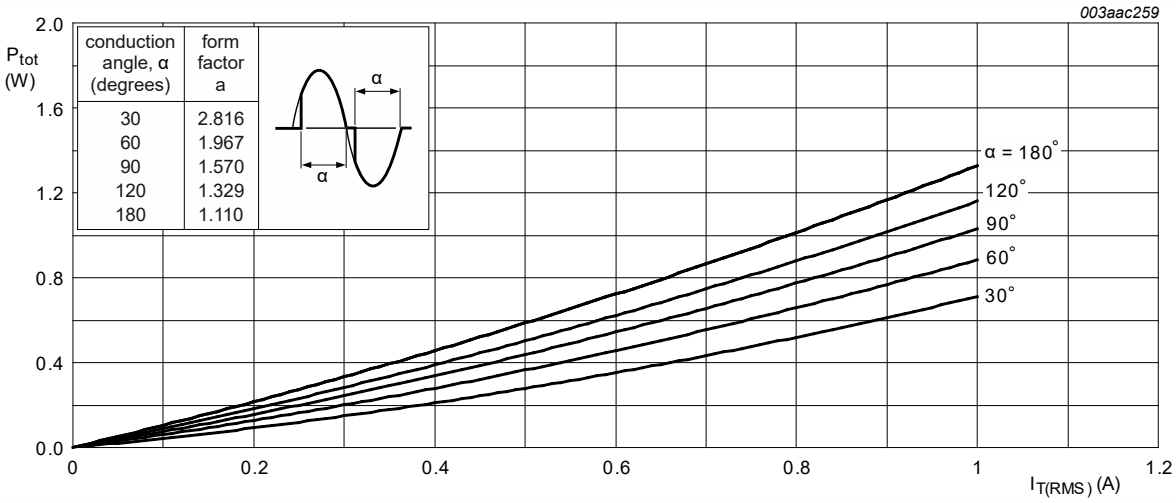



**Fig. 1. RMS on-state current as a function of solder point temperature; maximum values**




f = 50 Hz; $T_{sp}$ = 105 °C

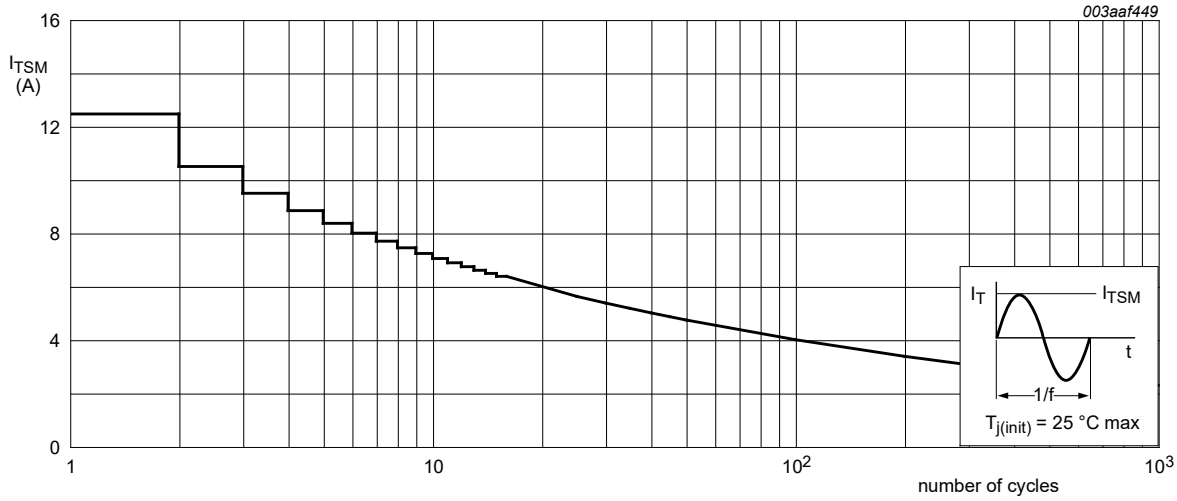
**Fig. 2. RMS on-state current as a function of surge duration; maximum values**




α = conduction angle

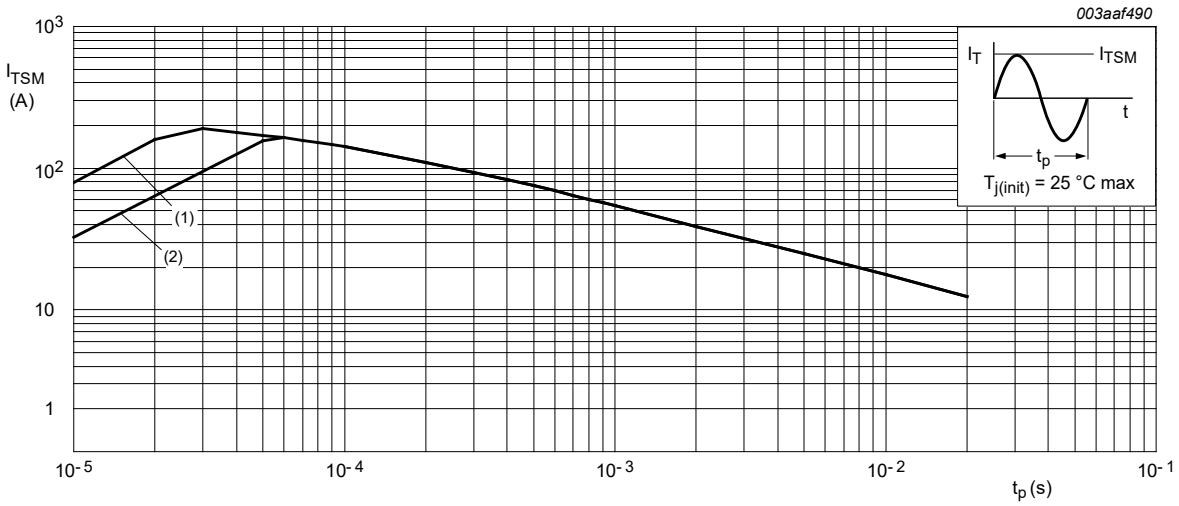
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

**Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values**




f = 50 Hz

**Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**




$t_p \leq 20$ ms
(1) $dI_T/dt$ limit
(2) T2- G+ quadrant limit

**Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values**

# 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | full cycle; Fig. 6 | | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient free air | in free air; printed-circuit board mounted: minimum footprint; full cycle; Fig. 7 | | - | 156 | - | K/W |
| | | in free air; printed-circuit board mounted: pad area; full cycle; Fig. 8 | | - | 70 | - | K/W |

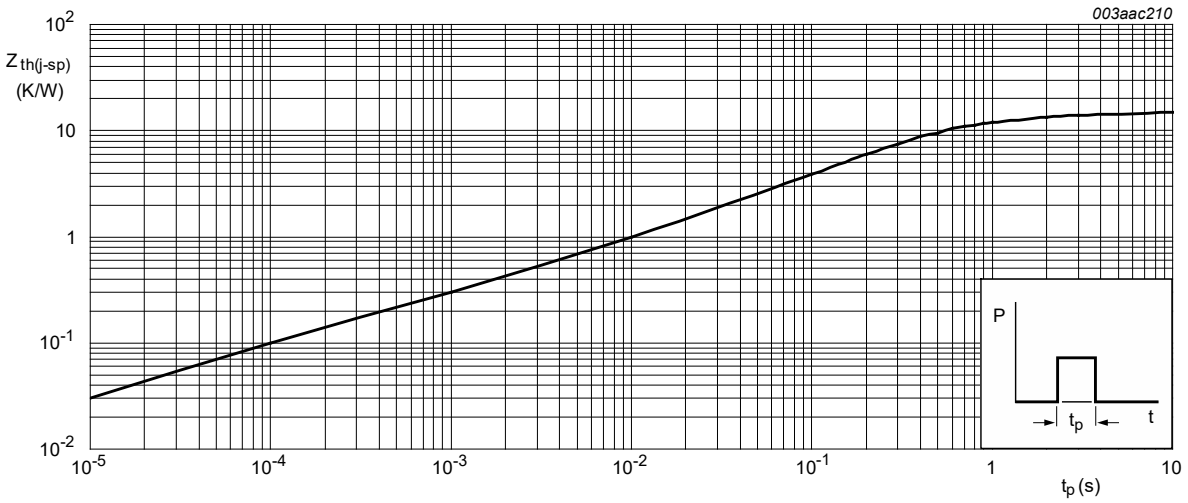
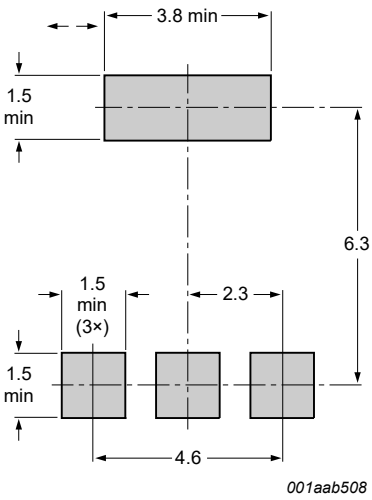
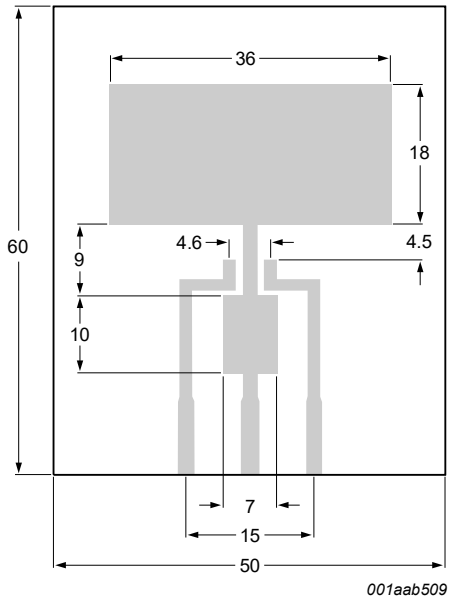



**Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width**




All dimensions are in mm

**Fig. 7. Minimum footprint SOT223**



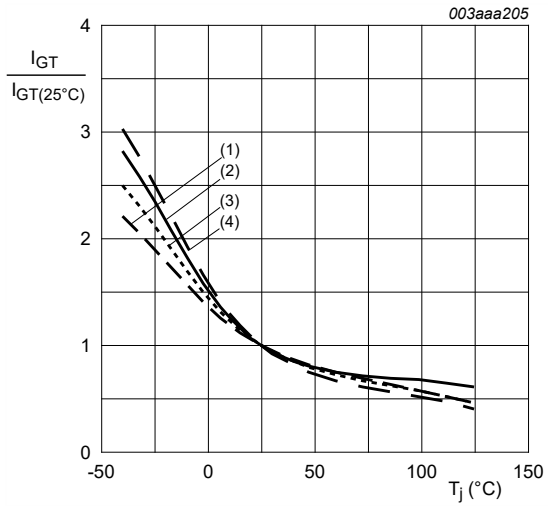

All dimensions are in mm
Printed circuit board:
FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

**Fig. 8. Printed circuit board pad area: SOT223**

# 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 9 | | 0.4 | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 9 | | 0.4 | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 9 | | 0.4 | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G+; $T_j$ = 25 °C; Fig. 9 | | 0.4 | - | 10 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 10 | | - | - | 15 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 10 | | - | - | 30 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 10 | | - | - | 15 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2- G+; $T_j$ = 25 °C; Fig. 10 | | - | - | 15 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 11 | | - | - | 10 | mA |
| $V_T$ | on-state voltage | $I_T$ = 1.4 A; $T_j$ = 25 °C; Fig. 12 | | - | 1.3 | 1.6 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 13 | | - | - | 1 | V |
| | | $V_D$ = 800 V; $I_T$ = 0.1 A; $T_j$ = 125 °C; Fig. 13 | | 0.2 | - | - | V |
| $I_D$ | off-state current | $V_D$ = 800 V; $T_j$ = 125 °C | | - | - | 0.5 | mA |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 110 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit; Fig. 14 | | 120 | - | - | V/µs |
| $dV_{com}/dt$ | rate of change of commutating voltage | $V_D$ = 400 V; $T_j$ = 110 °C; $dI_{com}/dt$ = 0.44 A/ms; gate open circuit | | 2 | - | - | V/µs |




(1) T2- G+
(2) T2- G-
(3) T2+ G-
(4) T2+ G+

**Fig. 9. Normalized gate trigger current as a function of junction temperature**

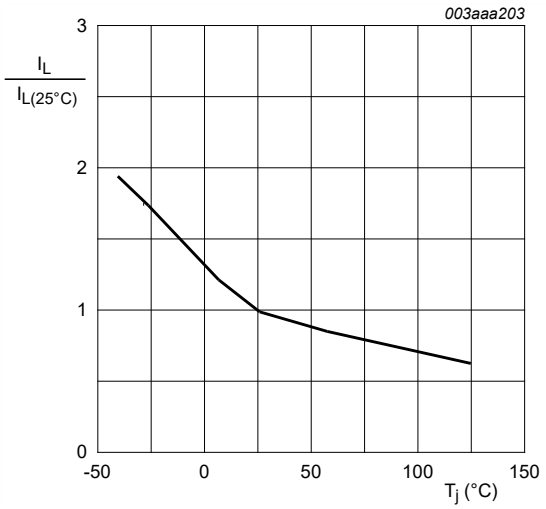



**Fig. 10. Normalized latching current as a function of junction temperature**

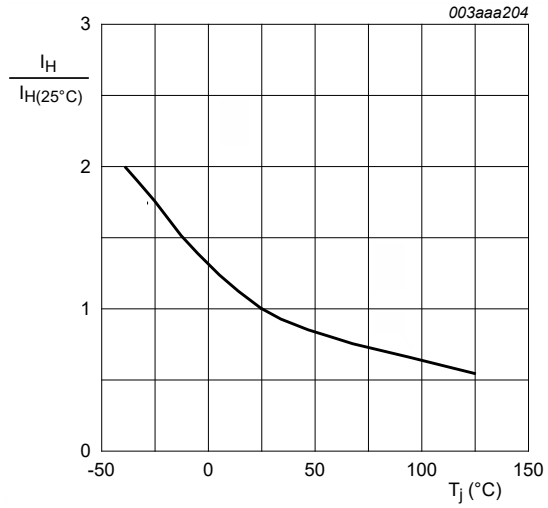
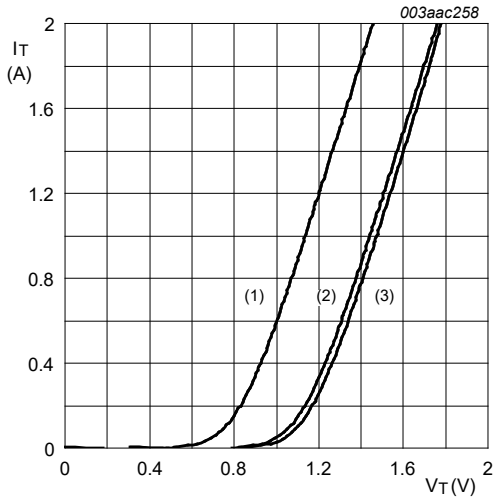



**Fig. 11. Normalized holding current as a function of junction temperature**




$V_o$ = 1.13 V
$R_s$ = 0.31 Ω
(1) $T_j$ = 125 °C; typical values
(2) $T_j$ = 125 °C; maximum values
(3) $T_j$ = 25 °C; maximum values

**Fig. 12. On-state current as a function of on-state voltage**

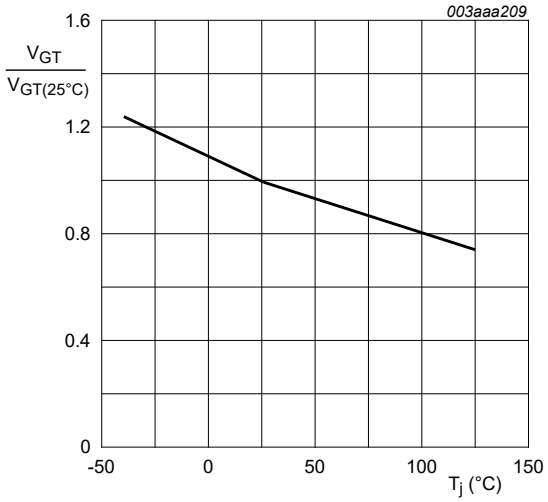
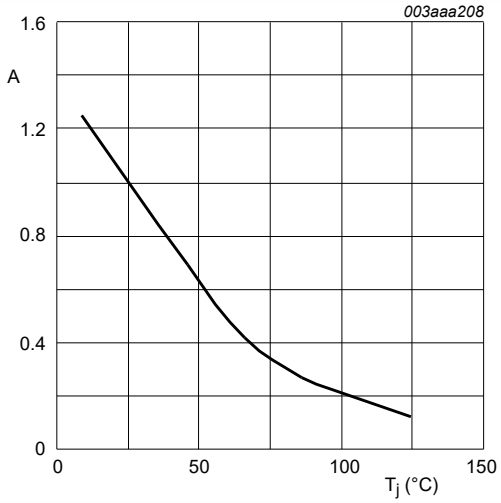



**Fig. 13. Normalized gate trigger voltage as a function of junction temperature**

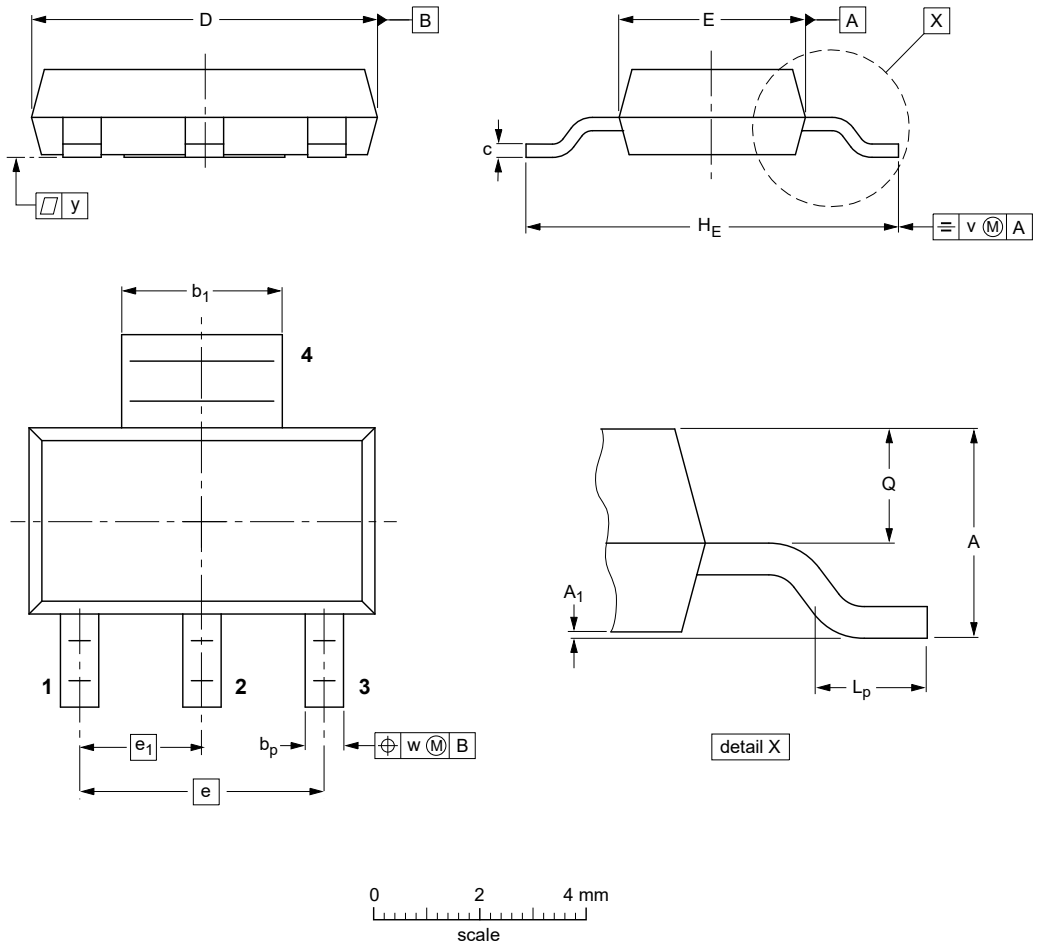



$$A = \frac{dV_{D(Tj\,^\circ C)} / dt}{dV_{D(25\,^\circ C)} / dt}$$

**Fig. 14. Normalized critical rate of rise of off-state voltage as a function of junction temperature; typical values**

## 10. Package outline

**Plastic surface-mounted package with increased heatsink; 4 leads** **SOT223**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | $b_1$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.8<br>1.5 | 0.10<br>0.01 | 0.80<br>0.60 | 3.1<br>2.9 | 0.32<br>0.22 | 6.7<br>6.3 | 3.7<br>3.3 | 4.6 | 2.3 | 7.3<br>6.7 | 1.1<br>0.7 | 0.95<br>0.85 | 0.2 | 0.1 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT223 | | | SC-73 | | | ~~04-11-10~~<br>06-03-16 |

**Fig. 15. Package outline SC-73 (SOT223)**

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| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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**Date of release: 15 September 2018**

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