



GNSS Module W2SG0021i

Product Datasheet

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Revision History:

Rev.	Revision Date	Originator	Changes
0.1	March 9, 2014	WJL	First preliminary draft
1.0	May 1, 2015	DS	Updated text, figures, tables, schematics, pin description, etc.
1.1	July 20, 2015	DS	Defined part ordering, updated figures, ref. schematic, etc.
1.13	August 18, 2015	DS	Modified part ordering information, shield marking, reference schematic, antenna configuration, MSL-1 reflow profile, evaluation kit images, etc.
1.14	April 12, 2016	DS	Added pin descriptions, updated part ordering information

1 General Description

This specification provides a general guideline on the performance and the integration of the Wi2Wi, Inc. GNSS Receiver Module Solution. The solder-down module, Part Number W2SG0021i is targeted to assist companies to easily integrate GNSS functionally into their products. This is accomplished by reducing their development times and cost by using a complete, small form factor, low power, ready to integrate GNSS Receiver System Solution.

W2SG0021i is a Global Navigation Satellite System (GNSS) engine optimized for low power operation. It provides highly accurate location and positioning for devices including mobile phones, cameras, and health and fitness products. By supporting GPS, GLONASS, BeiDou, QZSS, SBAS and Galileo ready, the highest accuracy and fastest time-to-first-fix (TTFF) are ensured.

Key features of the W2SG0021i are as follows:

- GNSS technology based upon SiRFstarV™ by CSR/SiRF™
- Compact design for easy integration: 7.00 mm x 7.00 mm x 2.00 mm
- Fast, Responsive Location Experience
 - 52 track verification channels
 - Concurrent tracking modes available: GPS+GLONASS, GPS+BeiDou, along with QZSS and SBAS (WAAS, EGNOS, MSAS, GAGAN)
 - Galileo ready
 - Low acquisition time and high sensitivity GNSS Receiver
 - High sensitivity navigation engine (PVT) to track signals as low as -165 dBm
- Breakthrough Power Consumption
 - Adaptive micro power controller
 - Ultra-low power consumption (Only 50 to 500µA maintains hot start capability)
 - 50 Ω Antenna Launch
 - 52 verification channel GNSS receiver
- Reliable in Difficult Environments
 - CW detection: enable scanning for narrowband interference in GPS/GLONASS signal path
 - GPS narrowband rejection: rejects up to 8 narrowband interferers in the GPS band
 - GPS out of band detection and band pass filtering
 - GLONASS interference cancellation: cancels up to 8 CW interferers in the GLONASS band
- Enhanced Navigation
 - Smart MEMS sensor interface
 - Multi-master I²C bus for smart sensors (Compass, Accelerometer)
 - Interrupt input for context change alarms

1.1 Pin Definition

The functional pin definition for the W2SG0021i is presented below in Table 1.

Table 1: Pin Definition

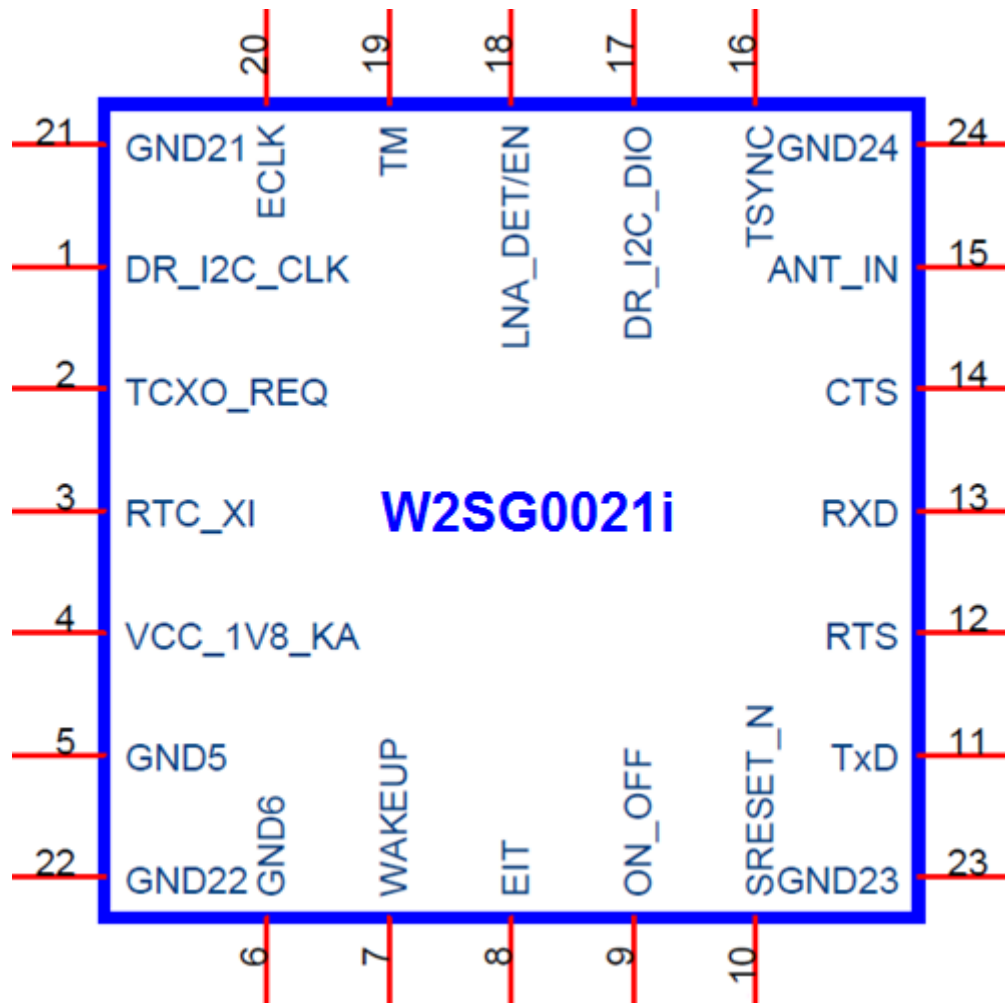
1	DR_I2C_CLK	O	Baud Rate Selection or I2C Clock
2	TCXO_REQ	I	Active low request to power on the VDD_TCXO_REG regulator
3	RTC_XI	I	Real Time Clock (32.768 KHz)
4	VCC_1V8_KA	PWR	1.8V DC power supply
5	GND5	GND	Ground
6	GND6	GND	Ground
7	WAKEUP	O	Wake up output for control of external PMIC
8	EIT	I	External Interrupt Trigger
9	ON/OFF	I	Power state control input
10	SRESET_N	I	Active low device reset
11	TXD	O	UART TX or I2C Clock
12	RTS	I	Ready to Send
13	RXD	I	UART RX or I2C Data
14	CTS	O	Clear to Send
15	ANT_IN	I	Antenna RF input (50 ohm impedance)
16	TSYNC	I	Time aiding input strobe
17	DR_I2C_DIO	I/O	Baud Rate selection or I2C Data
18	LNA_DET/EN	I	External Interrupt Trigger 2
19	TM	O	UTC Time Mark Output
20	ECLK	I	ECLK is an input for frequency aiding application
21	GND21	GND	Ground (Corner Pad)
22	GND22	GND	Ground (Corner Pad)
23	GND23	GND	Ground (Corner Pad)
24	GND24	GND	Ground (Corner Pad)

* Wi2Wi reserves the right to change the above information.

1.2 Pin Configuration

The W2SG0021i is a 24 pin SMD device with a board down antenna connection. The pin configuration is presented below in Figure 1.

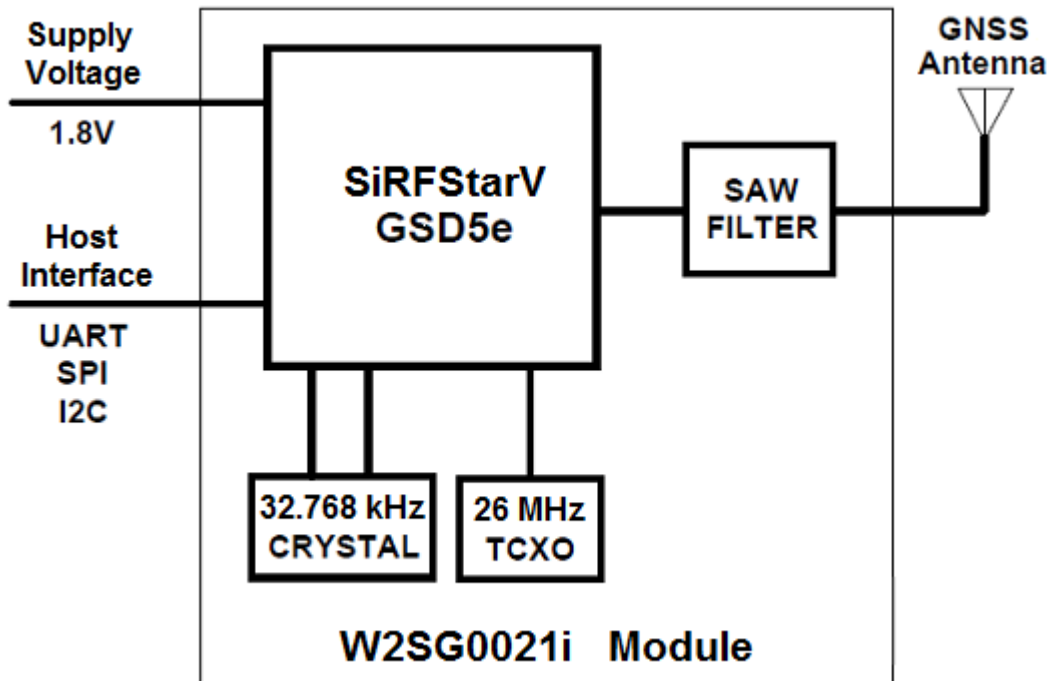
Figure 1: Pin Diagram



1.3 System Block Diagram

The System Block for the W2SG0021i is presented below in Figure 2.

Figure 2: System Block Diagram



- The W2SG0021i consists of an internal LNA, all required power regulation and clocking.
- The TTL UART Interface is accessible via Pin 11 and 13.

1.4 Power Supply Considerations

The W2SG0021i must be powered from a single 1.8V supply. The W2SG0021i does not support operation with separate voltage supply sources to different sections of the module. Customer designs with split voltage supply sources (for example, one for battery back-up supply and one for main current load), can be met by using a diode bridge combining the different sources into a single 1.8V supply to the W2SG0021i. The high current supply source can be enabled by the WAKEUP output pin; the low current back-up supply battery can be connected to one of the diode inputs. The supply controlled by WAKEUP must provide full power within 100 μ S of being enabled to prevent high current draw from the back-up source.

2 Specifications

2.1 Clock Frequency

The W2SG0021i features an internal clock and crystal; hence, it doesn't require any external clock sources.

Absolute Maximum Ratings:

The values presented below in Table 2 are those parameters beyond which permanent damage could result. These values *do not* imply functional operation and should be considered as stress ratings only.

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Input Voltage	V_{DD}	5.5	V
RF Input	RF_{IN}	10	dBm
Case Temperature	T_{CASE}		°C
Lead Temperature (Soldering, 10sec)	T_{MFG}	260	°C
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_S	NA to +150	°C

2.2 Interfaces

Table 3 below shows the pin configuration for CTS (Pin 14) and RTS (Pin 12) for the selection of host interfaces.

Table 3: Host Interface Selection

Host Interface	CTS (Pin 14)	RTS (Pin 12)
UART	Pull-Up	Floating
Slave SPI	Floating	Floating
Multi-Master I ² C	Floating	Pull-Down

2.2.1 Host UART Interface

The TTL UART Interface (Pins 11 and 13) has a baud rate 4800 BAUD. Protocol options for the W2SG0021i are NMEA and OSPTM (SiRF BINARYTM).

2.2.2 Host I²C Interface

The TTL I²C Interface (Pins 11 and 13) has a speed range of 400 kbps. The default values for the I²C interface are: Rx: 0x60, Tx: 0x62

Operating mode is Multi-Master: The Transmit side operates as a master by seizing the I²C bus when detected idle, the Receive side operates as a slave when another master seizes the I²C bus and transmits to the module address. The I²C module implements the I²C bus standard contention resolution mechanism.

2.2.3 Host Slave SPI

The Slave SPI (SSPI) is a 4-wire slave mode SPI port. The highest clock rate for Slave SPI is 6.840320 MHz and supports both SPI and Micro-wire formats. The transmitter and receiver have individual firmware-defined 2-byte idle patterns of 0xa7 & 0xb4. SPI detects synchronization errors and is reset by software.

The 4 SPI pins are:

- SSPI_DO: slave SPI data output (MISO)
- SSPI_DI: slave SPI data input (MOSI)
- SSPI_CLK: slave SPI clock input (CLK)
- SSPI_SS_N: slave SPI chip select (CS#) active low

2.3 Master Mode I²C Interface [Dead Reckoning (DR) I²C Interface]

The W2SG0021i master mode I²C interface provides support for dead reckoning (DR). The master mode port has 2 pins: DR_I2C_CLK (Pin 1) and DR_I2C_DIO (Pin 17). Both pins are pseudo open-drain and require pull-up resistors on the external bus. Dead reckoning applications support the DR I²C interface. The I²C interface supports required sensor instruments such as gyros, accelerometers, compasses or other sensors that can operate with an I²C bus. DR I²C interface supports common sensor formats (accelerometer, gyro, magnetometer, altimeter, etc.). Typical data lengths are usually several bytes (command + in/out data). Standard I²C bus has a maximum data rate of 400 kbps and a minimum data rate of 100 kbps.

3 Specific Pin Functions

The pins related to special features of the W2SG0021i, which may or may not be used depending on a customer's design.

3.1 Baud Rate Selection

DR_I2C_CLK (Pin 1) and DR_I2C_DIO (Pin 17) can be used to configure the W2SG0021i module to output NMEA at standard baud rates, if you are not using I2C or SPI flash devices on these pins. Table 4 below lists the settings for DR_I2C_CLK and DR_I2C_DIO to configure the baud rate at start-up. After start-up, these pins can be released for other purposes.

Table 4: Pin Configuration for Baud Rate Selection at Start-up

DR_I2C_CLK (Pin 1)	DR_I2C_DIO (Pin 17)	Protocol	Baud Rate
High	High	NMEA	4800
Low	High	NMEA	9600
High	Low	NMEA	38400
Low	Low	OSP	115200

Important Note:

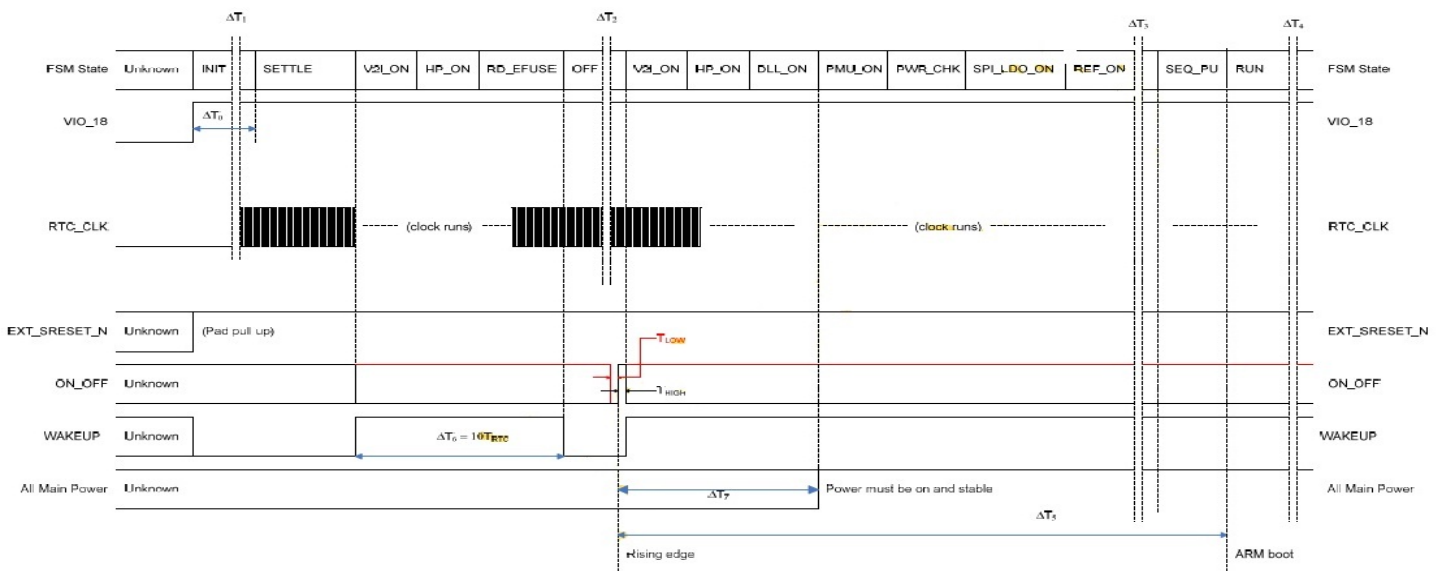
This flexibility is not available if any MEMS or non-volatile memory devices are attached to the auxiliary serial bus. The internal software default baud rate is 4800 bps, but this can be modified using the HW configuration as shown in Table 4 (Refer to the Baud Rate Selection App Note).

Failure to tie DR_I2C_CLK and DR_I2C_DIO high or low in the absence of both SPI flash and EEPROM causes an increase in standby and hibernate current, and also causes the start-up configuration of the UART interface to be indeterminate.

3.2 ON/OFF

After power up, the W2SG0021i is in a hibernate state awaiting a pulse on the ON/OFF (Pin 9) to put it into a fully active state. To enable the W2SG0021i a positive pulse for two RTC ticks (62 μ s) must be applied. To place the module back into a hibernate state, the same pulse needs to be applied to the ON/OFF signal after the Receiver has stabilized after a Fix (Stabilization can be up to 18 minutes depending on weather conditions). **This can be verified with a message ID 18, called “OK to Send”, that comes out when the receiver is receptive to commands.** Figure 3 shows the internal state power up sequence of the SiRFstarV™ inside the W2SG0021i, many of the signals listed are not accessible outside of the module, they are provided as reference only.

Figure 3: Power on Sequence



3.3 WAKEUP

The WAKEUP (Pin 7) is an output from the W2SG0021i used to enable an external PMIC (Power Management Integrated Circuit). A “Low” on this output indicates that the W2SG0021i is in one of its low-power states (Hibernate or Standby mode) and requires no more than 60 μ A of current on the 1.8V power rail. A “High” on this output indicates that the W2SG0021i is in operational mode requiring an external regulator to provide enough current for normal operation of the W2SG0021i module.

3.4 EIT

The EIT (Pin 8) is an external, level-sensitive interrupt trigger to the module’s internal ARM processor via the interrupt controller module. The EIT pin is also configurable as an edge-sensitive input.

This pin can be used as a source of a level-sensitive interrupt to wake-up the W2SG0021i module from Standby and Hibernate low-power modes. This function allows external sensors, e.g. gyro, accelerometer, compass, etc., to provide an interrupt when a change of state is detected.

This pin can be left floating or unconnected, no external interrupt trigger is required.

3.5 TM

The Time Mark (Pin 19) functions as follows: the Time Mark output provides a one pulse-per second (1 PPS) signal to the customer’s application processor. When the receiver provides a valid navigation solution which consists of five satellite vehicles, the rising edge of each TMARK pulse is synchronized with the UTC one second epochs to within ± 1 microsecond. The receiver software produces a binary format data message containing the UTC time associated with each time mark pulse. This signal is a positive logic, buffered CMOS level output pulse that transitions from a logic “low” to logic “high” at a 1 Hz rate. The TMARK output pulse rise time is typically less than 2 nanoseconds and the pulse duration is typically 200 milliseconds.

Patch Option:

A patch exists that allows the Time Mark to output the 1 PPS with only four satellite vehicles instead of the default of five satellite vehicles. This patch can be downloaded from the Wi2Wi Extranet and implemented with the GPS patch manager that will run on Windows 7 and Linux operating systems. Please register at www.wi2wi.com to download from the extranet site.

3.6 SRESET_N

The SRESET_N (Pin 10) is an external reset pin and is only used in case of malfunction or catastrophic crash, to force the SiRFstarV chipset to restart. To perform an external system reset, pull this pin low for ≥ 20 μ s when the supply voltage is present. This pin can be left floating or unconnected if you’re not controlling the reset function externally, because this pin is internally pulled to a weak-high.

3.7 TCXO_REQ

If the reference TCXO is not shared with another system, then TCXO_REQ (Pin 2) must be left floating or unconnected. Then, a weak internal pull-up will default this pin to logic high, when the module is enabled via the ON/OFF pin.

3.8 RTC_XI

The RTC crystal (32.768 KHz) is provided internally within the W2SG0021i module itself. Hence, RTC_XI (Pin 3) can be left floating or unconnected.

3.9 LNA_DET/EN

The LNA_DET/EN (Pin 18) is used to select the gain mode of the internal LNA.

- If an external LNA is used, pull this pin low – this puts the internal LNA into low gain mode.
- If no external LNA is used, pull this pin high or leave it floating or unconnected – this puts the internal LNA into high gain mode.

For e.g., it is left floating by default on our reference schematic, as our evaluation board has an integrated passive chip antenna onboard.

3.10 TSYNC and ECLK

TSYNC (Pin 16) and ECLK (Pin 20) are input pins for external time aiding and frequency aiding respectively. These are only used to improve the GNSS reference clock accuracy from an external source such a cellular modem or application processor. If not needed, these pins can be left floating or unconnected.

3.11 Auto Start

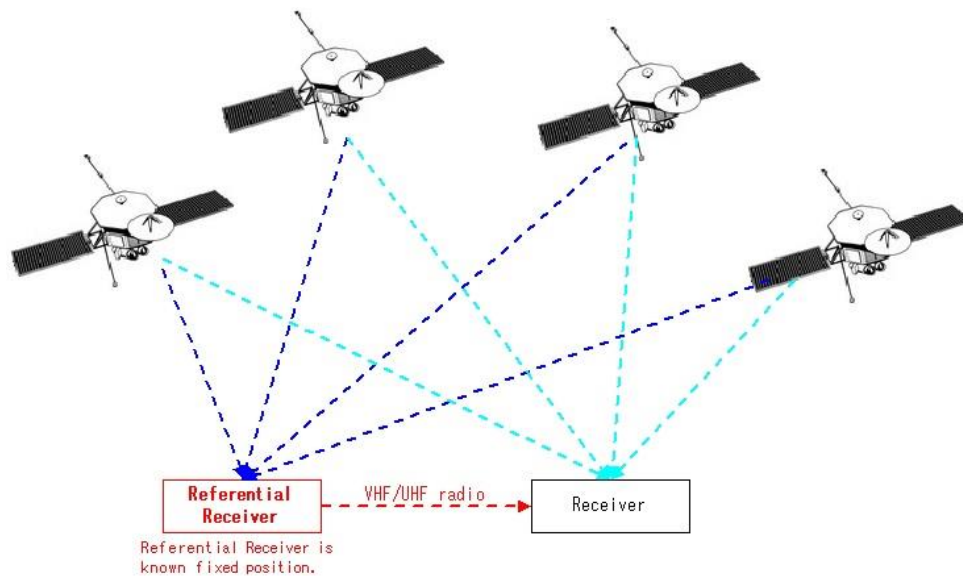
By connecting the WAKEUP (Pin 7) to the ON/OFF (Pin 9), the module will automatically turn ON upon power up. This will enable the customer to auto-enable or auto-wakeup the module. But, to put the module into sleep mode, it would require that this connection is not made and that a positive going pulse is initiated to put the module into a hibernate state.

4 WAAS with SBAS or Wide Area Differential GPS

4.1 Differential GPS

Differential GPS (DGPS) is traditionally used with the fix of three to four satellites and the secondary fix from ground based GPS receiver based stations that retransmit the secondary fix via VHF/UHF and occasionally FM. DGPS can achieve positional accuracies of between 60 cm ~ 10 cm/s. See Figure 4.

Figure 4: Traditional DGPS System



DGPS requires at least two antennas, one for the NavStar L1 CA signal from the satellite and one antenna for the secondary fix from the VHF/UHF/FM transmitter. Also a secondary application processor is used to perform “Mixing” calculations between the two fixes. This increases the size and the expenses of the system.

4.2 Wide Area DGPS or WAAS

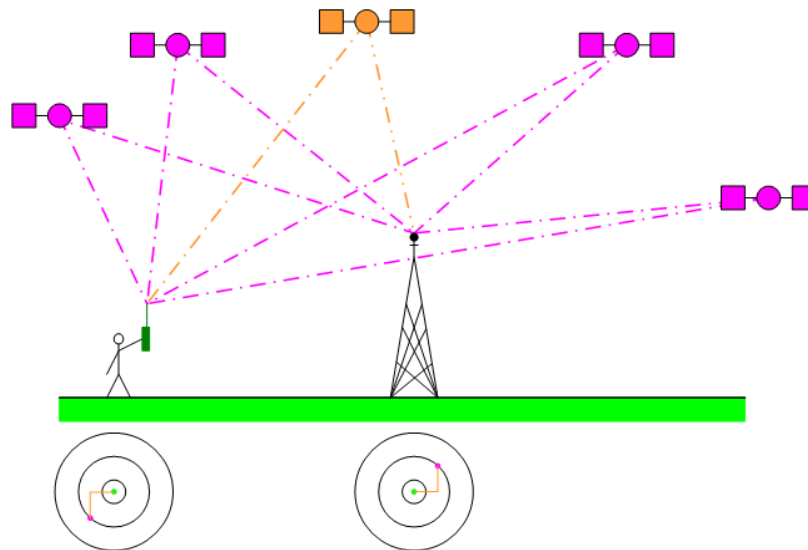
Wide Area DGPS or WAAS (Wide Area Augmentation System) uses the same concept but eliminates the need for the secondary RF signal. It accomplishes this by reusing the already orbiting satellites to re-broadcast other secondary fixes that have been established by ground based master stations in North America and Hawaii, to measure small variations in the GPS satellites' signals in the western Hemisphere. Measurements from the reference stations are routed to master stations, which queue the received Deviation Correction (DC) and send the correction messages to geostationary WAAS satellites in a timely manner (every 5 seconds or better). These master stations rebroadcast the secondary fix to the NavStar satellites which broadcast the secondary fix on unused channel space. This enables a GPS receiver to utilize the same antenna to reprocess both fixes internal to it also eliminating the need for a secondary

application processor. WAAS enables a GPS receiver to provide positional accuracy to 300 cm ~ 200 cm. Of course a GPS receiver utilizing WAAS will need an expanded offering of GPS receiver channels to effectively use this feature like the W2SG0021i which has 48 channels available for this function.

As noted this system was originally developed for the U.S. and Northern Hemisphere Geography. As GPS became ubiquitous in technology use throughout the world, similar systems called generically as Satellite-Based Augmentation System (SBAS). A SBAS is a system that supports wide-area or regional augmentation through the use of additional satellite-broadcast messages. Such systems are commonly composed of multiple ground stations, located at accurately-surveyed points. The ground stations take measurements of one or more of the GNSS satellites, the satellite signals, or other environmental factors which may impact the signal received by the users. Using these measurements, information messages are created and sent to one or more satellites for broadcast to the end users.

While SBAS designs and implementations may vary widely, with SBAS being a general term referring to any such satellite-based augmentation system, under the International Civil Aviation Organization (ICAO) rules a SBAS must transmit a specific message format and frequency which matches the design of the United States Wide Area Augmentation System.

Figure 5: SBAS Example System



Some examples of these are (GPS Aided GEO Augmented Navigation) GAGAN developed for the Indian Sub-Continent, European Geostationary Navigation Overlay Service (EGNOS) developed for the European Union, and the Japanese Multi-functional Satellite Augmentation System (MSAS), respectively.

4.3 How do we enable WAAS-SBAS on the W2SG0021i?

WAAS-SBAS is enabled by issuing Message ID 133, (MID 133) is supported in One Socket Protocol (Formerly SiRF™ Binary Protocol mode), and then the accuracy improves to 300 cm ~ 100 cm with it enabled, depending on Open Sky Conditions (Multi-Path interference). With MID 133 not enabled, the accuracy is near 1500 cm.

5 Electrical/RF Characteristics: Operating

Table 5 below presents the normal limits of operation for the W2SG0021i. Operations of the W2SG0021i beyond the limits of these tables are not recommended and may result in permanent damage of the device. Unless otherwise specified, operating conditions are over $T_A = -30^{\circ}\text{C}$ to $+85^{\circ}\text{C}$. Typical is defined as $T_A = +25^{\circ}\text{C}$.

Table 5: Operating Electrical Characteristics

Parameter ¹	Symbol	Min.	Typ.	Max.	Units
Power Supply (V_{CC})					
Power Supply Voltage	V_{CC}	1.71	1.80	1.89	V
I/O Supply Voltage	V_{IO}	1.71	1.80	1.89	V
Power Supply Ripple	V_{RIP}			100	mV
I/O Input Current	I_{IO}		1.5	2.0	mA
Current Consumption (I_{CC})					
Acquisition Mode Current	I_{CC_ACQ}	40	44	50	mA
Tracking Mode Current	I_{CC_TR}	30	34	40	mA
Power Save Mode Current	I_{CC_PS}	25	27	30	μA
UART Interface (TX, RX)					
Input Pin Voltage	V_{RX}		1.8	3.6	V
Output Pin Voltage	V_{TX}		1.8		V
GPS Enable (GPS_ON/OFF)					
Input Pin Low Voltage	V_{IL}	0		0.45	V
Input Pin High Voltage	V_{IH}	1.35	1.8	3.6	V
RF Input					
Input Impedance	R_{ANT}		50		Ω
Operating Frequency	F_{OPR}		1.575		GHz
RF Characteristics					
Power In @ 1.5745 GHz	P_{IN}	-157	-131	-10	dBm
Noise Figure	NF		3.0		dB
Input IP2 ($f_1=849\text{MHz}$, $f_2=2424\text{MHz}$) -30dBm in	IIP2		-5		dBm
Input IP3 ($f_1=1574.5\text{MHz}$, $f_2=1575.5\text{MHz}$) -30dBm in	IIP3		-2		dBm
Input Return Loss	RL_{IN}		-10.0		dB
Input VWR	VWR_{IN}		1.50:1	1.8:1	
Reverse Isolation	ISL		-28		dB
Stability (100 -10000 MHz)					
Receiver Sensitivity:					
Signal Acquisition @ 31dBHz	P_{ACQ}		-148		dBm
Signal Tracking	P_{TR}		-163		dBm

Notes:

¹ All parameters are at $T_A = 25^{\circ}\text{C}$, unless otherwise specified.

² Defined as peak current drawn during initial acquisition operation of GPS Receiver.

6 Performance

6.1 Acquisition Time

The average Time To First Fix (TTFF) for the W2SG0021i when integrated into the evaluation kit is presented in Table 6 below:

Table 6: Average Time to First Fix

Parameter ¹	Symbol	Min	Typ.	Max.	Units
Hot Start @ -130 dBm	TTFF _{HOT}	-	< 1.0	-	s
Warm Start @ -130 dBm	TTFF _{WARM}	-	26	-	s
Cold Start @ -130 dBm	TTFF _{COLD}	-	28	-	s

Notes:

¹ Stationary receiver, unless otherwise specified.

² All parameters are at T_A = 25°C, unless otherwise specified.

6.2 Position Accuracy

Table 7 below presents the Positional Accuracy for the W2SG0021i when integrated into the evaluation kit.

Table 7: Positional Accuracy

Parameter ¹	Typ.	Units
Horizontal Position Accuracy: CEP (50%)	3	m
Horizontal Position Accuracy: 2dRMS (95%)	12	m
Vertical Position Accuracy: CEP (50%)	3	m
Vertical Position Accuracy: 2dRMS (95%)	12	m
Horizontal Velocity Accuracy: Deviation	-	m/s
Vertical Velocity Accuracy: Deviation	-	m/s

Notes:

¹ Stationary receiver, Open Sky at -130 dBm, unless otherwise specified.

² All parameters are at T_A = 25°C, unless otherwise specified.

6.3 Environmental Characteristics

Table 8 establishes the environmental limits for operational use of the W2SG0021i.

Table 8: Environmental Characteristics

Parameter	Symbol	Min	Typ.	Max.	Units
Storage Temperature	T _{STR}	NA	-	+150	°C
Operating Temperature	T _{OPR}	-40	+25	+85	°C
Humidity		5	-	95	%/Non-condensing
Altitude		-	-	60,000/18,288	ft/m
Acceleration		-	-	6.0	g
Velocity				< 1,000	knots

6.4 Current and Power Consumption

Table 9 shows the current and power consumption values in different modes of operation for W2SG0021i.

Table 9: Current and Power Consumption

Mode of Operation	Current		Units	Power @ 1.8V		Units
	Typ	Max		Typ	Max	
Acquisition Mode	50	63	mA	90	114	mW
Tracking Mode	33	48	mA	60	87	mW
Hibernate Mode / Power Save Mode	10	14	µA	18	26.1	µW

6.4.1 Internal LNA Gain

The W2SG0021i is provided with an internal LNA amplifier with two selectable gain levels. In general, the high gain mode is intended for use with passive antennas, while the low gain mode is used when there is an external LNA as part of the RF front end (e.g. active antenna).

Note: By default, the internal LNA is configured in high gain mode.

The internal LNA must be configured in low gain mode, when an active antenna with an external LNA has to be used. To change the internal LNA to low gain mode, use the following steps:

1. Switch GPS Communication Protocol from NMEA to OSP mode.
2. Send Tracker Configuration Message (OSP MID 178, 02) - (Disable Internal LNA and drive GPS_EXT-LNA_EN signal):

**A0 A2 00 39 B2 02 00 F9 C5 68 03 FF 00 00 0B B8 00 01 77 FA 01 01 03 FC 03 FC 00
04 00 00 00 00 00 7C 00 00 00 00 00 00 00 00 00 00 00 00 00 01 C2 00 00 00 62 00 60
01 01 01 F4 2A 01 0B 38 B0 B3**

3. Wait for SiRFstarV ACK: **A0 A2 00 03 0B B2 00 00 BD B0 B3**
4. Perform a Hot Start reset; Tracker Configuration setting requests in message (OSP MID 178, 02) will apply after performing this reset.
5. Wait for SiRFstarV ACK: **A0 A2 00 03 0B 80 00 00 8B B0 B3**
6. Switch GPS Communication Protocol back to NMEA mode.

6.4.2 Maximum RF Gain

- When internal LNA is in high gain mode, a passive antenna acts as input. Total RF gain (sum of internal LNA gain, cable and filter losses) of ≤ 5 dB is considered acceptable.
- When internal LNA is in low gain mode, an active antenna acts as input. Total RF gain (sum of external antenna gain, internal LNA gain, cable and filter losses) of 14 to 24 dB is considered acceptable.

7 Antenna

The W2SG0021i module incorporates an integrated LNA which allows operation with either an onboard passive chip antenna (dual band GPS/GLONASS) or an external active antenna (tri-band GPS/GLONASS/BeiDou).

The antenna configuration for W2SG0021i evaluation board is as below:

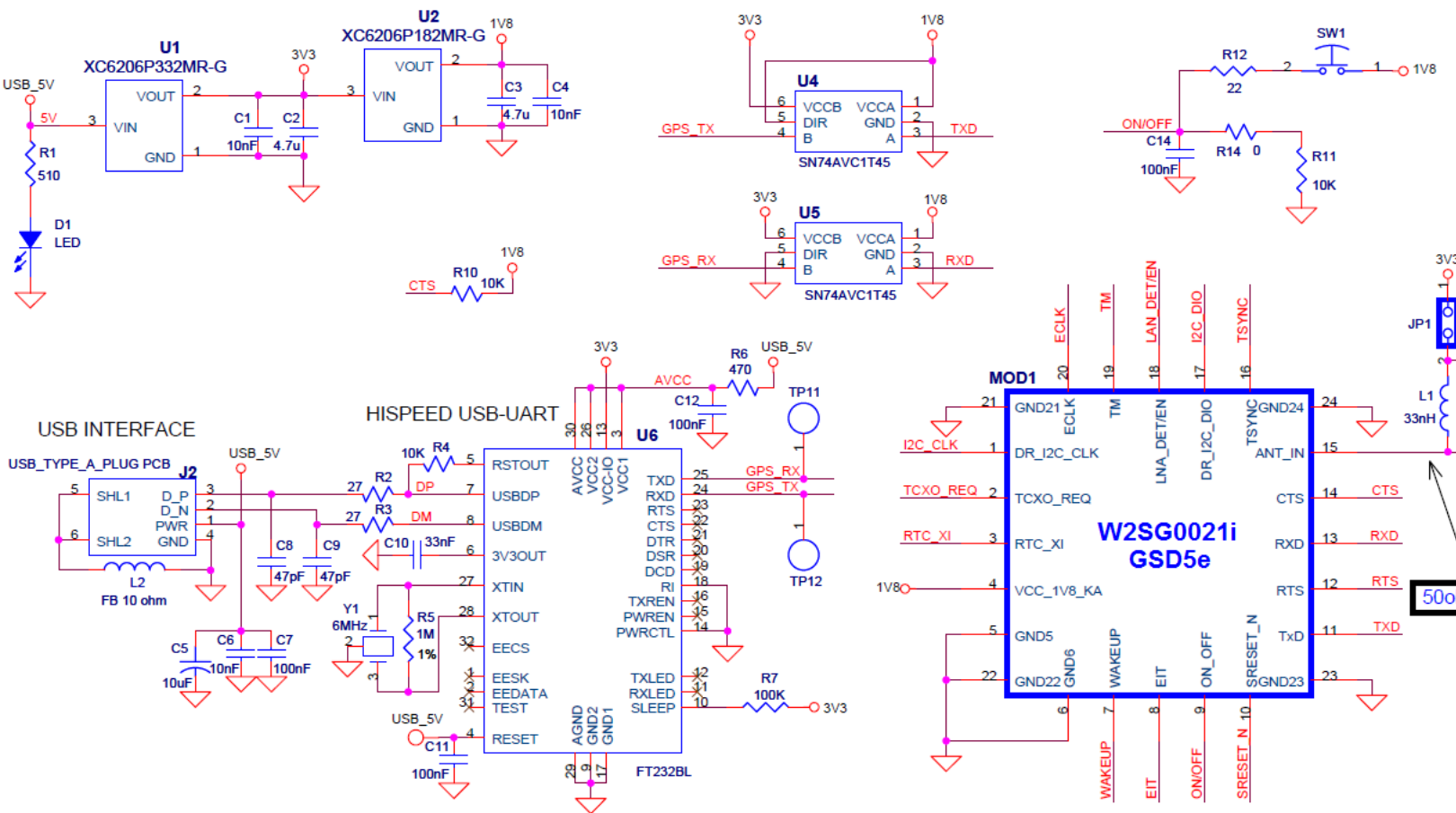
- Onboard Passive Chip Antenna: **JP1 open**, R15 open, R17 connected
- External Active Antenna: **JP1 connected**, R15 connected, R17 open

Note that only one antenna can be used at any given time, either the onboard passive chip antenna or the external active antenna. Refer to the app notes for antenna configuration for further details about appropriate antenna selection.

8 Reference Schematic

Figure 6 shows the reference schematic for using the W2SG0021i module.

Figure 6: Reference Schematic



Note: Antenna selection is based on the following configuration (Refer App Notes as well):

- Onboard Passive Chip Antenna: **JP1 open**, R15 open, R17 connected
- External Active Antenna: **JP1 connected**, R15 connected, R17 open

9 Development Support

The W2SG0021i module is embedded with the latest software. This software is optimized to work in very weak signal environments to improve navigation availability and accuracy.

To enable performance testing, Wi2Wi provides an evaluation kit, along with the CSR's SiRFLive software. SiRFLive is a PC tool that provides real-time monitoring of an attached GPS/GNSS receiver's operation such as tracking/acquisition of satellites, observed signal strength, and current position in terms of latitude, longitude and elevation.

10 Mechanical Information

10.1 Mechanical Specification

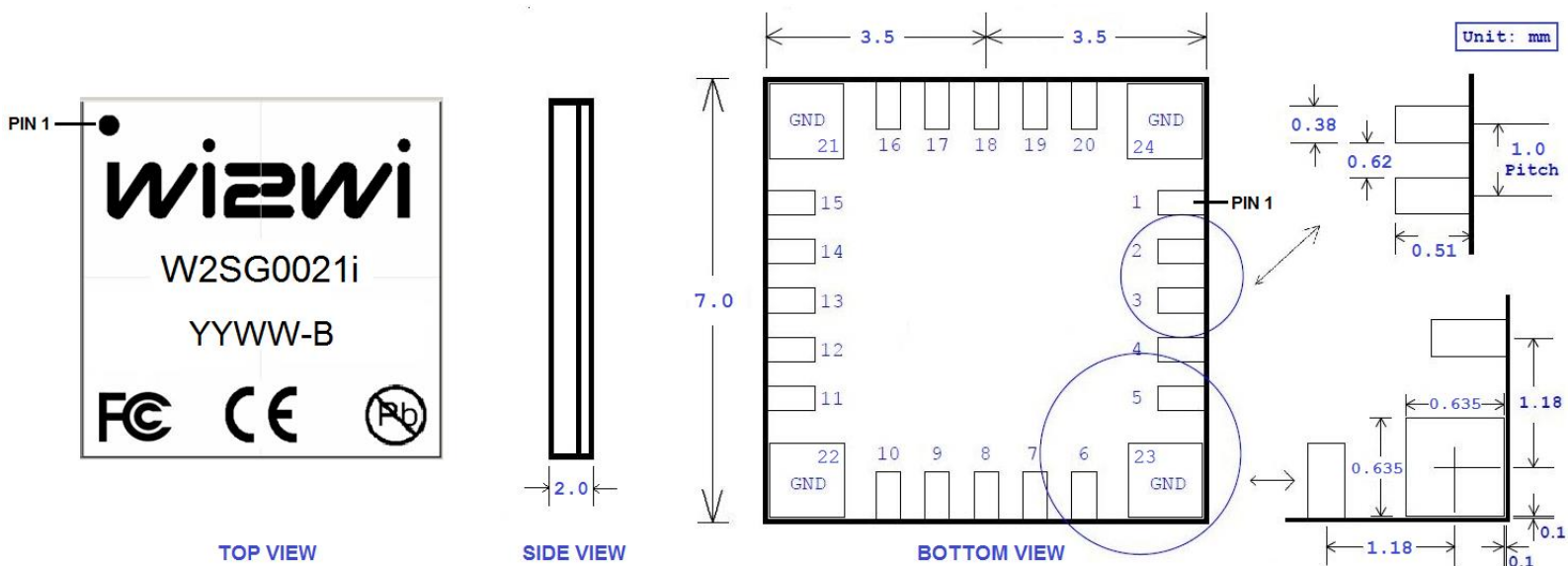
The overall dimension of the W2SG0021i module is 7 mm x 7 mm x 2 mm, including the shield. Figure 7 shows detailed dimensions of the W2SG0021i module. It is a Surface Mount Device (SMD) type module. All measurements are in mm, and are not to scale.

YY indicates Year

WW indicates Work Week

Note: Refer to Ordering Information in Section 11.

Figure 7: Marking and Mechanical Dimensions: W2SG0021i



10.2 Storage and Baking Instructions

W2SG0021i module is qualified as moisture sensitivity level MSL1 package, in accordance with JEDEC J-STD-020 standard.

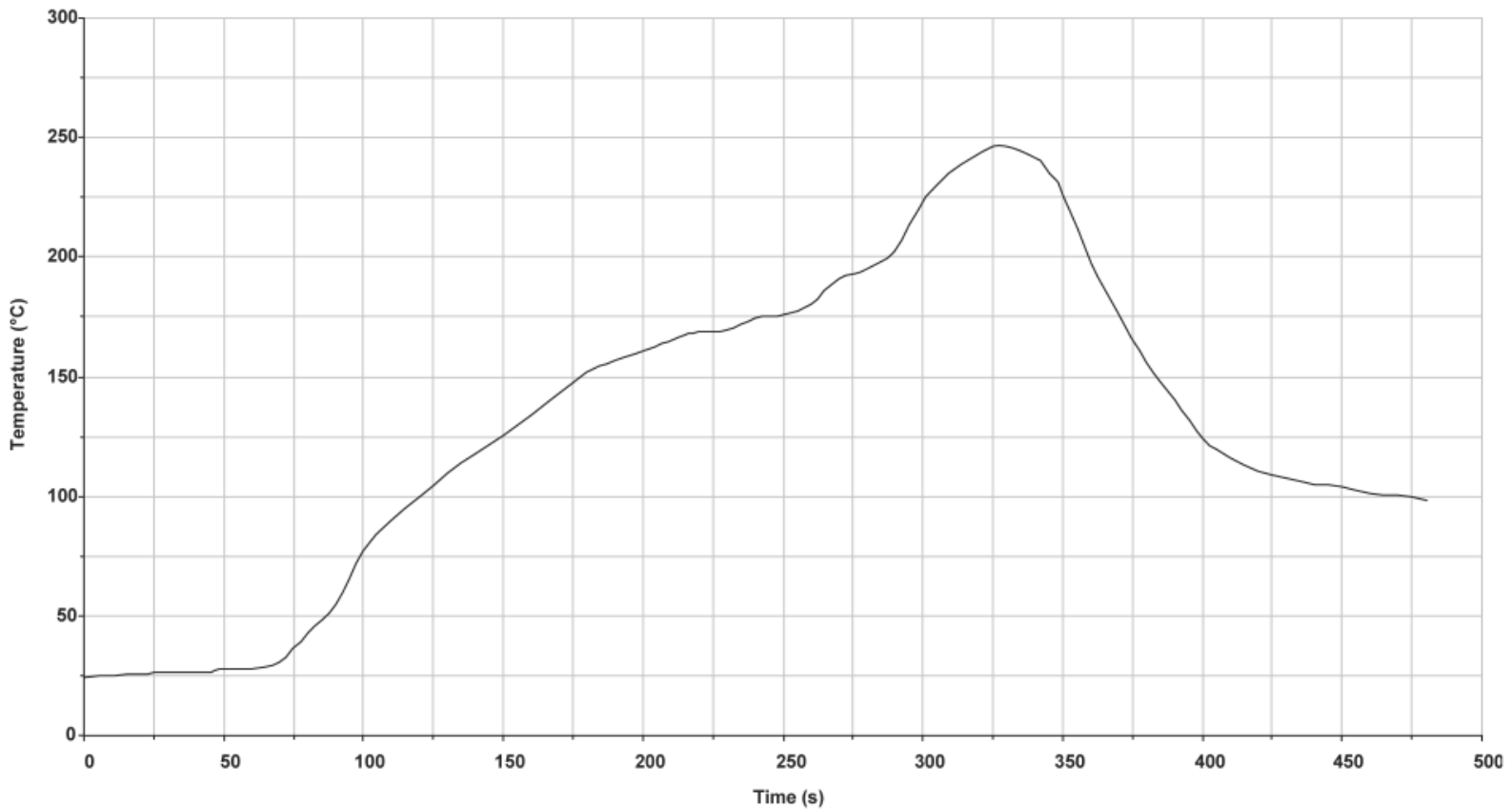
MSL1 indicates that there are no special dry pack requirements or time limits from opening of static bag to reflow for floor conditions of $\leq 30^{\circ}\text{C}$ and 85% RH

10.3 Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a setup for each application. The data here is given only for guidance on solder re-flow. There are four zones:

- **Preheat Zone:** This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
- **Equilibrium Zone:** This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimize the out gassing of the flux.
- **Reflow Zone:** The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
- **Cooling Zone:** The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

Figure 8: Typical Lead-free Reflow Solder Profile



Key features of the profile:

- Initial ramp = 1-2.5°C/sec to 175°C ± 25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to maximum temperature (245°C) = 3°C/sec max.
- Time above liquidus temperature (217°C) = 45-90 seconds
- Device absolute maximum reflow temperature = 260°C

11 Ordering Information

Table 10: Ordering Information for Modules

Part Order Number	Architecture	Satellite Systems Supported Concurrently	Boot-up Method	Default Boot-up Baud Rate	Packaging Method
W2SG0021i-T	CSR SiRFstarV GSD5e	GPS, GLONASS, QZSS, SBAS	Internal ROM based	4800 bps over NMEA	Tray
W2SG0021i-TR	CSR SiRFstarV GSD5e	GPS, GLONASS, QZSS, SBAS	Internal ROM based	4800 bps over NMEA	Tape & Reel

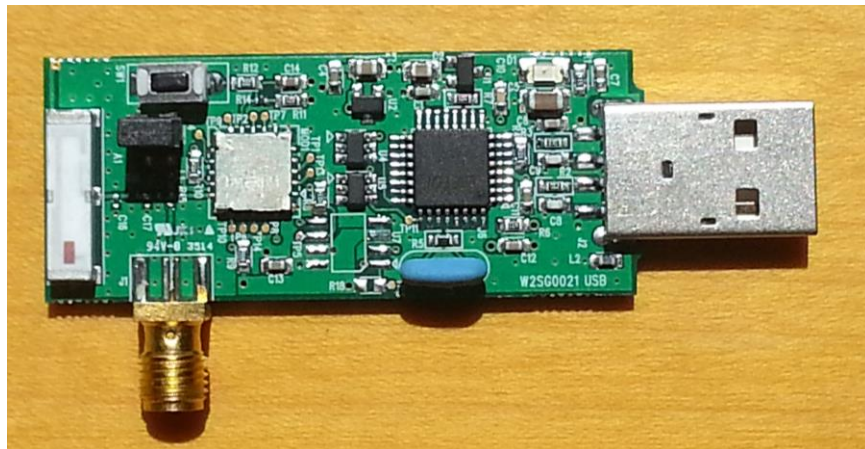
Table 11: Ordering Information for Evaluation Kits

Part Order Number	Architecture	Contents of the Evaluation Kit	Boot-up Method	Default Boot-up Baud Rate	Packaging Method
W2SG0021i EVK	CSR SiRFstarV GSD5e	W2SG0021i Evaluation Board, Tri-band Active Antenna, Evaluation CD with App Notes, etc.	Internal ROM based	4800 bps over NMEA	Box

All our evaluation kits are designed to provide a quick demonstration of the GNSS receiver module, with the customer's host processor.

This kit consists of the W2SG0021i evaluation board which has concurrent support for GPS, GLONASS, QZSS and SBAS systems. This module boots up from the internal ROM and the default baud rate = 4800 bps over NMEA.

Figure 9: W2SG0021i USB Dongle Evaluation Board



Each evaluation kit package consists of:

- USB Dongle Evaluation Board with onboard dual-band GPS/GLONASS passive chip antenna
- A tri-band external active antenna: GPS/GLONASS/BeiDou
- Evaluation CD with Application Notes, Datasheet, Product Brief, Reference Schematic, Quick Start Guide, SiRFLive software and other supporting documents

12 Disclaimers

Wi2Wi, Inc. PRODUCTS ARE NOT AUTHORISED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE MANAGING DIRECTOR OF Wi2Wi, Inc.

The definitions used herein are:

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Wi2Wi does not assume responsibility for use of any of the circuitry described, no circuit patent licenses are implied and Wi2Wi reserves the right at any time to change without notice said circuitry and specifications.

12.1 Datasheet Status

Wi2Wi, Inc. reserves the right to change the specification without prior notice in order to improve the design and supply the best possible product. Updated information, firmware and release notes will be made available on www.wi2wi.com. Please check with Wi2Wi Inc. for the most recent data before initiating or completing a design.

13 Certifications

The W2SG0021i module complies with the following standards when integrated with the Evaluation Kit:

EMC/Immunity

- FCC Part 15 Chapter B (USA)
- IC Canada (Canada)
- CE (Europe)

14 References

14.1 Specifications

- System Specification, SiRFstarV™ GSD5e WLCSP, Issue 2, CS-229581-DSP2
- NMEA Issue 5, CS-129435-UGP5
- OSP Issue 15, CS-129291-DCP15
- FAA WAAS Specification FAA-E 2892b

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