



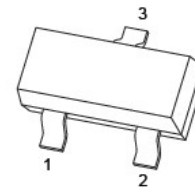
WG7002

## Features:

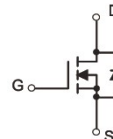
- High density cell design for low RDS(ON)
- Voltage controlled small signal switch
- Rugged and reliable
- High saturation current capability



1. GATE
2. SOURCE
3. DRAIN



Equivalent Circuit


**Maximum Ratings & Thermal Characteristics** (Ratings at 25°C ambient temperature unless otherwise specified.)

Parameters	Symbol	Value	Unit
Drain-Source Voltage	V <sub>DS</sub>	60	V
Gate-Source Voltage	V <sub>GS</sub>	±20	V
Continuous Drain Current	I <sub>D</sub>	340	mA
Power Dissipation	P <sub>D</sub>	350	mW
Junction Temperature	T <sub>j</sub>	150	°C
Storage Temperature	T <sub>stg</sub>	-50-+150	°C
Thermal Resistance From Junction to Ambient	R <sub>θJA</sub>	357	°C/W

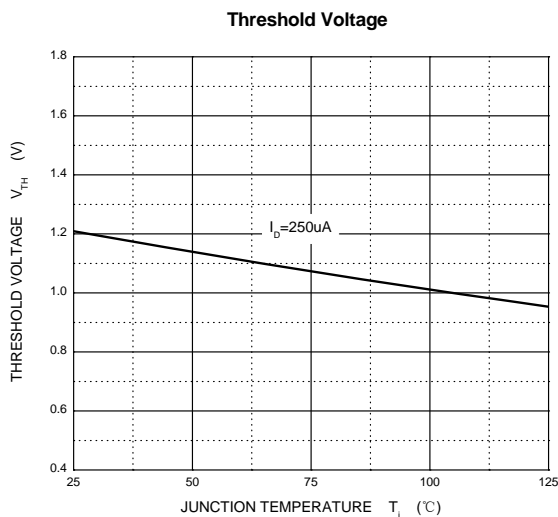
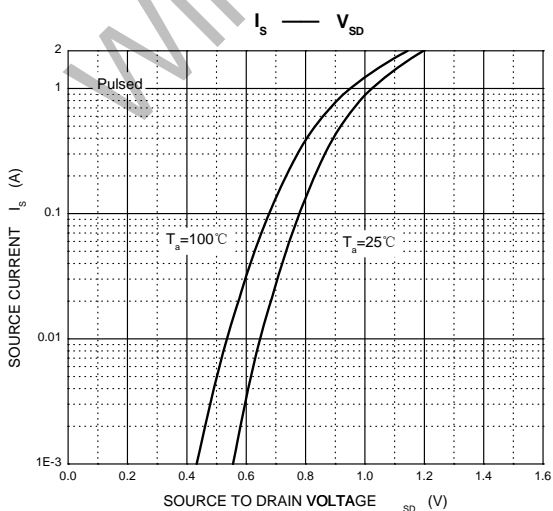
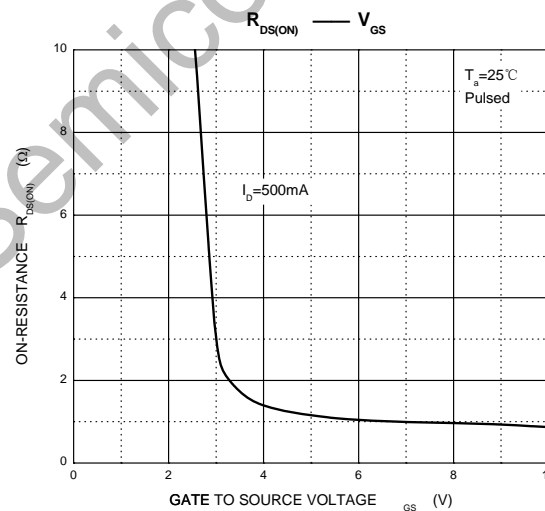
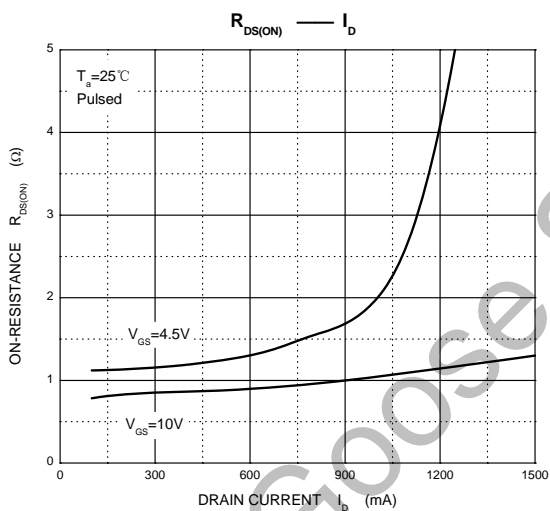
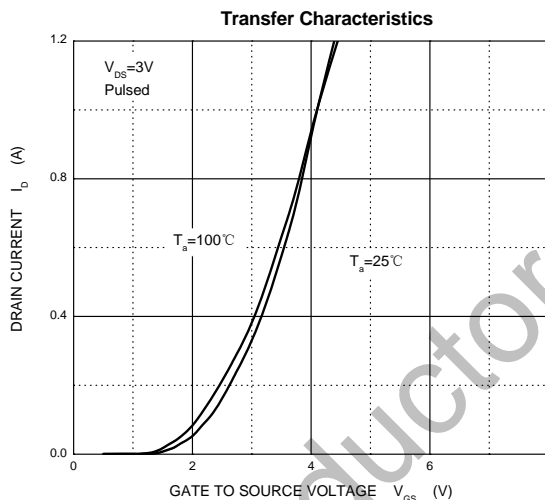
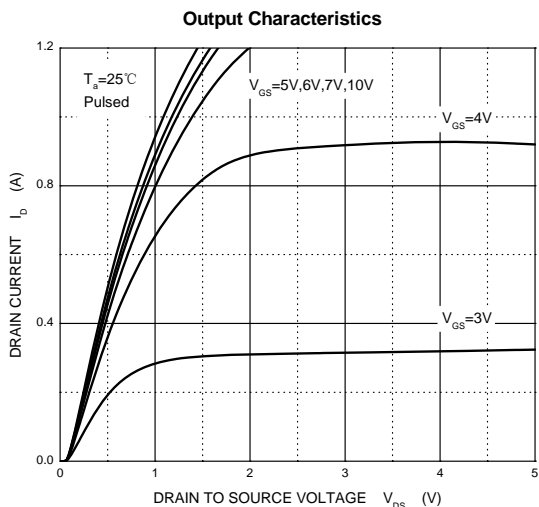
**Electrical Characteristics** (Ratings at 25°C ambient temperature unless otherwise specified).

Parameter	Symbols	Test Condition	Limits			Unit
			Min	Typ	Max	
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	60			V
Gate-Threshold voltage*	V <sub>th(GS)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =1mA	1	1.3	2.5	V
Gate-body Leakage	I <sub>GSS1</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±20V			±10	uA
	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±10V			±200	nA
	I <sub>GSS</sub>	V <sub>DS</sub> =0V, V <sub>GS</sub> =±5V			±100	nA
Zero Gate Voltage Drain current	I <sub>DSS</sub>	V <sub>DS</sub> =48V, V <sub>GS</sub> =0V			1	uA
Drain-Source On-Resistance*	R <sub>DS(ON)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =500mA		0.9	5	Ω
		V <sub>GS</sub> =4.5V, I <sub>C</sub> =200mA		1.1	5.3	
Diode Forward voltage	V <sub>SD</sub>	I <sub>S</sub> =300mA, V <sub>GS</sub> =0V			1.50	V
Input capacitance**	C <sub>iss</sub>	V <sub>DS</sub> =10V, V <sub>GS</sub> =0V, f=1MHz			40	pF
Output capacitance**	C <sub>oss</sub>				30	
Reverse Transfer capacitance**	C <sub>rss</sub>				10	
<b>SWITCHING TIME</b>						
Turn-on Time**	t <sub>d(on)</sub>	V <sub>DD</sub> =50V, R <sub>L</sub> =250Ω, V <sub>GS</sub> =10V, R <sub>GS</sub> =50Ω, R <sub>G</sub> =50Ω			10	ns
Turn-off Time**	t <sub>d(off)</sub>				15	
Reverse recovery Time	t <sub>rr</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =300mA, V <sub>R</sub> =25V, Dis/dt=-100a/uS		30		ns
<b>GATE-SOURCE ZENER DIODE</b>						
Gate-Source Breakdown Voltage	BV <sub>GSO</sub>	I <sub>GS</sub> =±1mA(Open Drain)	±21.5		±30	V

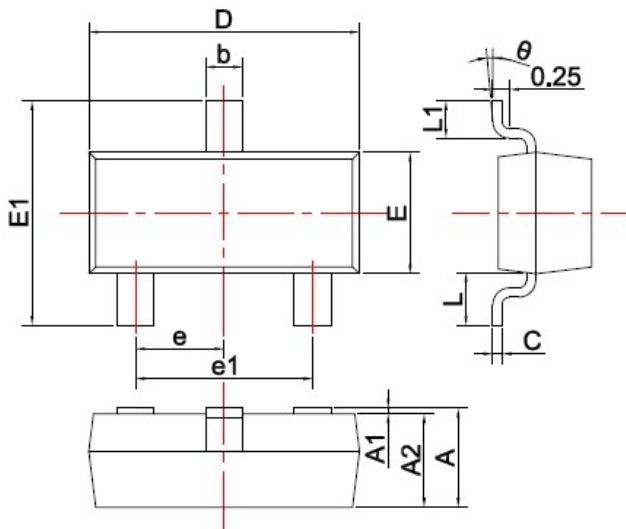
Notes: \* Pulse Test: Pulse Width ≤300us, Duty Cycle≤2%.

\*\* These parameters have on way to verify.

Typical characteristics



SOT-23 PACKAGE OUTLINE Plastic surface mounted package

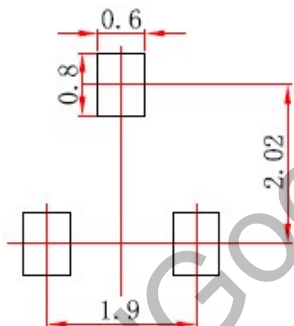


SYMBOL	DIMENSIONS	
	MIN.	MAX.
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
c	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950TYP	
e1	1.800	2.000
L	0.550REF	
L1	0.300	0.500
θ	0°	8°

Unit: mm

Precautions: PCB Design

Recommended land dimensions for SOT-23 diode. Electrode patterns for PCBs



Note:

1. Controlling dimension: in millimeters.
2. General tolerance: ± 0.05mm.
3. The pad layout is for reference purposes only.

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