Features:

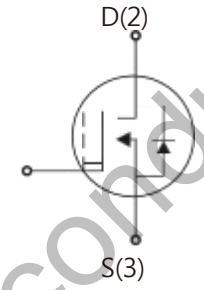
- ☐ Ultra Low RDS(ON) = 600mΩ @ VGS = 10V.
- ☐ Ultra Low Gate Charge, Qg=18.4nC typ.
- ☐ Fast switching capability
- ☐ Robust design with better EAS performance
- ☐ EMI Improved Design (*SnowMOS*^{TM} Gen.2)
- ☐ VDSS=650 V,ID=7.3A
- ☐ 100% Avalanche Tested

Application

- ☐ TV Power
- ☐ High Performance Charger / Adapter
- ☐ LED Lighting Power

TO-220F

RoHS COMPLIANT



1.Gate (G)
2.Drain (D)
3.Source (S)

Absolute Maximum Ratings

Drain-Source Voltage (Note2)		VDSS	650	V
Gate-Source Voltage		VGSS	±30	V
Continuous Drain Current	TC=25ºC	ID	7.3	A
	TC=25ºC (Note 3, D=75%)		8.4	
	TC=125ºC		3.3	
Pulsed Drain Current (Note 4)		IDM	24.0	A
Avalanche Energy, Single Pulse (Note 5)		EAS	105	mJ
Avalanche Energy, Repetitive (Note 4)		EAR	0.15	mJ
Avalanche Current, Repetitive (Note 4)		IAR	1.3	A
Continuous Diode Forward Current		IS	7.3	A
Diode Pulse Current		IS.PULSE	24.0	A
Operating Junction Temperature		TJ	150	ºC
Storage Temperature		TSTG	-55 to 150	ºC
Lead Temperature (Soldering, 10 sec)		TLEAD	260	ºC

Note:

1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. For voltage spike during switching.
3. Limited by TJ_MAX, Maximum duty cycle D=0.75
4. Repetitive Rating: Pulse width limited by maximum junction temperature
5. IAS = 1.3A, VDD = 60V, RG = 25Ω, Starting TJ = 25°C

Thermal characteristics

Parameter		Symbol	Min	Typ	Max	Unit
Thermal resistance, Junction-to-Case	TO-252	RthJC			2.13	℃ /W
Thermal resistance, Junction-to-Ambient	TO-252	RthJA			60	℃ /W

Electrical Characteristics TJ = 25℃, unless otherwise specified.

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics							
Drain-Source Breakdown Voltage		BVDSS	VGS=0V, ID=250uA	650			V
Zero Gate Voltage Drain Current		IDSS	VDS=650V, VGS=0V			1	uA
Gate-Body Leakage Current	Forward	IGSSF	VGS=30V, VDS=0V			100	nA
	Reverse	IGSSR	VGS=-30V, VDS=0V			-100	
Gate Threshold Voltage		VGS(TH)	VDS=VGS, ID=250uA	2.7	3.6	4.5	V
Static Drain-Source On-Resistance		RDS(ON)	VGS=10V, ID=4.0A		510	600	mΩ
Gate Resistance		RG	f=1MHz, Open Drain		8.9		Ω
Dynamic Characteristics							
Input Capacitance		CISS	VDS=50V, VGS=0V, f=1MHz		356		pF
Output Capacitance		COSS			31.8		
Reverse Transfer Capacitance		CRSS			18.7		
Effective output capacitance, energy related NOTE6		CO(er)	VGS=0V, VDS=0 ...480V		16		pF
Effective output capacitance, time related NOTE7		CO(tr)			72		
Turn-on Delay Time		td(on)	VDD=400V, ID=4.0A RG=10Ω, VGS=10V		10		ns
Rise Time		tr			12		
Turn-off Delay Time		td(off)			36		
Fall Time		tf			14		
Gate Charge Characteristics							
Gate to Source Charge		Qgs	VDD=480V, ID=4.0A VGS=0 to 10V		4.2		nC
Gate to Drain Charge		Qgd			9.1		
Gate Charge Total		Qg			18.4		
Gate Plateau Voltage		Vplateau			5.9		V
Reverse Diode Characteristics							
Drain-Source Diode Forward Voltage		VSD	VGS=0V, ISD=4.0A		0.84	1.1	V
Reverse Recovery Time		trr	VR=400V, IF=4.0A dIF/dt=100A/us		206		ns
Reverse Recovery Charge		Qrr			1.63		uC
Peak Reverse Recovery Current		Irrm			15.8		A

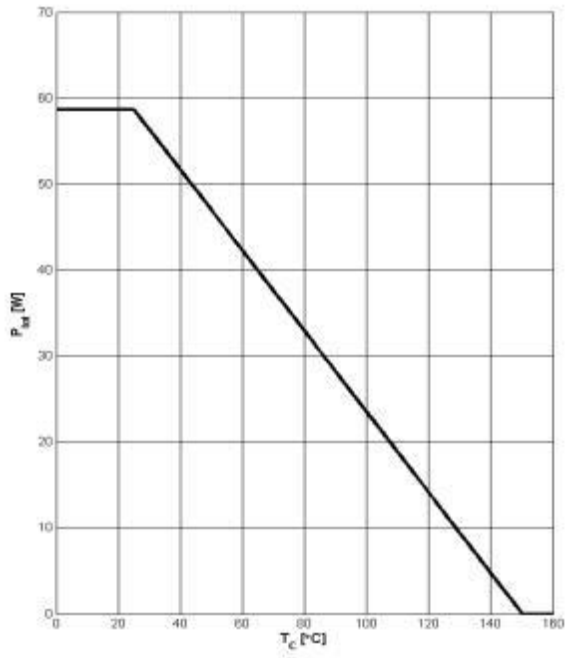
Note:

6. CO(er) is a fixed capacitance that gives the same stored energy as COSS while VDS is rising from 0 to 480V

7. CO (tr) is a fixed capacitance that gives the same charging time as COSS while VDS is rising from 0 to 480 V

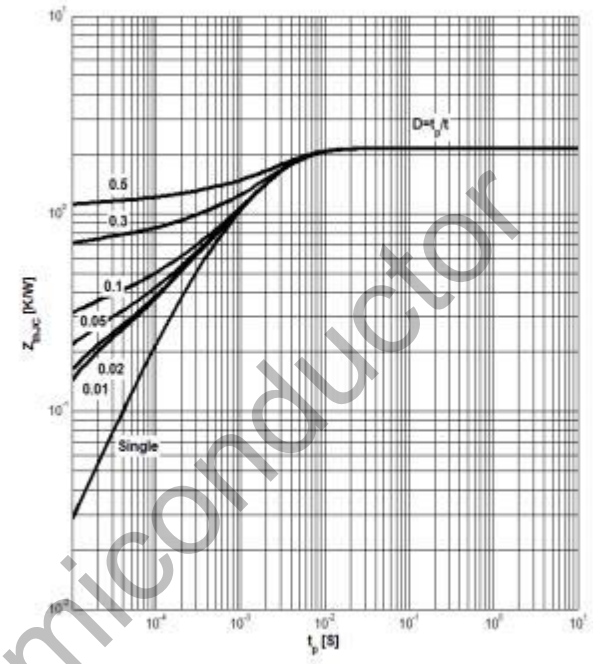
Typical Performance Characteristics

Figure 3: Power Dissipation



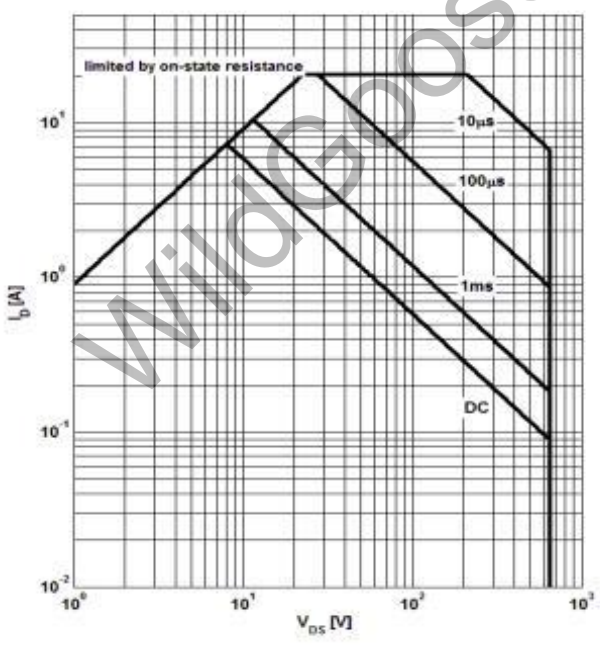
$P_{tot} = f(T_c)$

Figure 4: Max. Transient Thermal Impedance



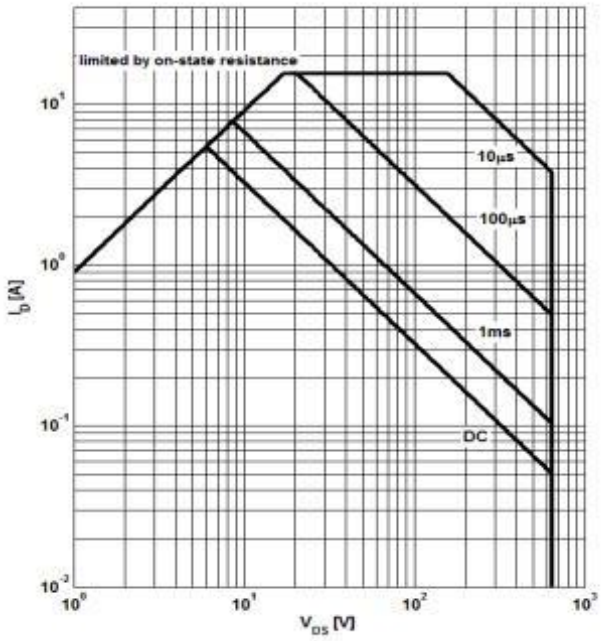
$Z(_{thJC}) = f(t_p)$; parameter: $D = t_p/T$

Figure 5: Safe Operating Area



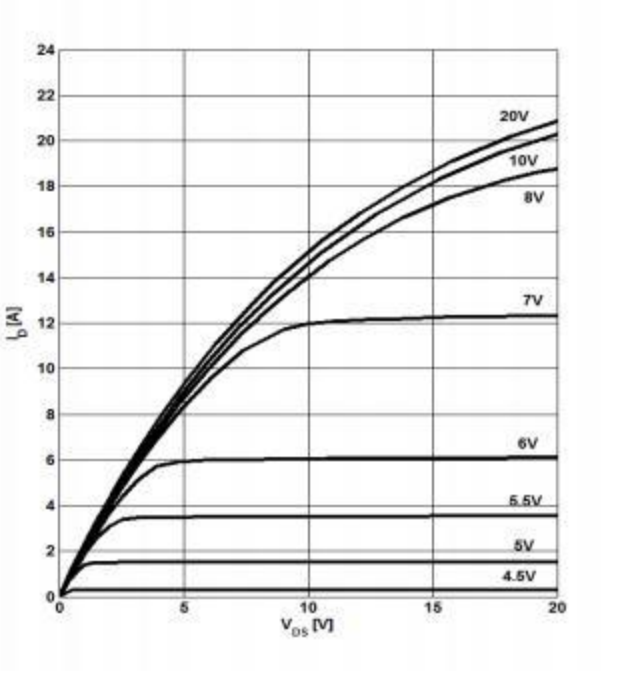
$I_D = f(V_{DS})$; T_c= 25ºC; V_{GS}>7V; parameter t_p

Figure 6: Safe Operating Area



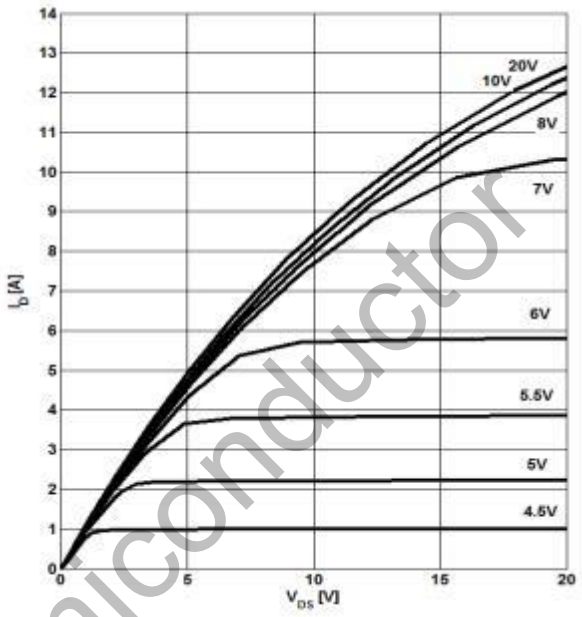
$I_D = f(V_{DS})$; T_c= 80ºC; V_{GS}>7V; parameter t_p

Figure 7: Typ. Output Characteristics



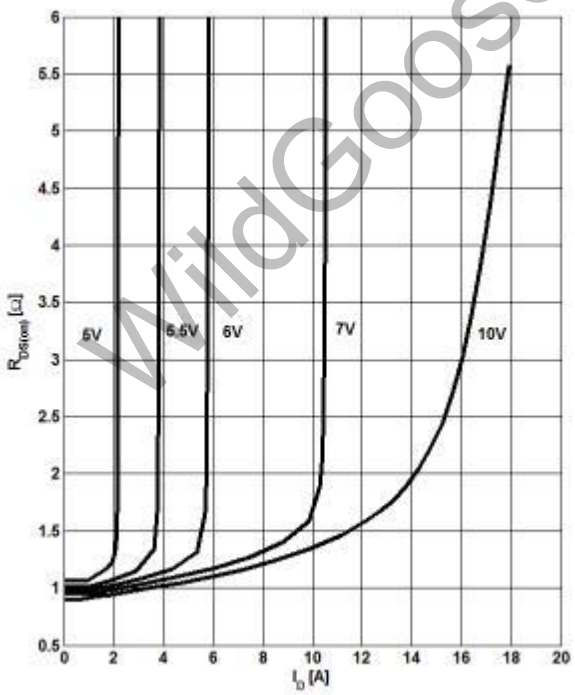
ID = f(VDS); Tj= 25ºC; parameter: VGS

Figure 8: Typ. Output Characteristics



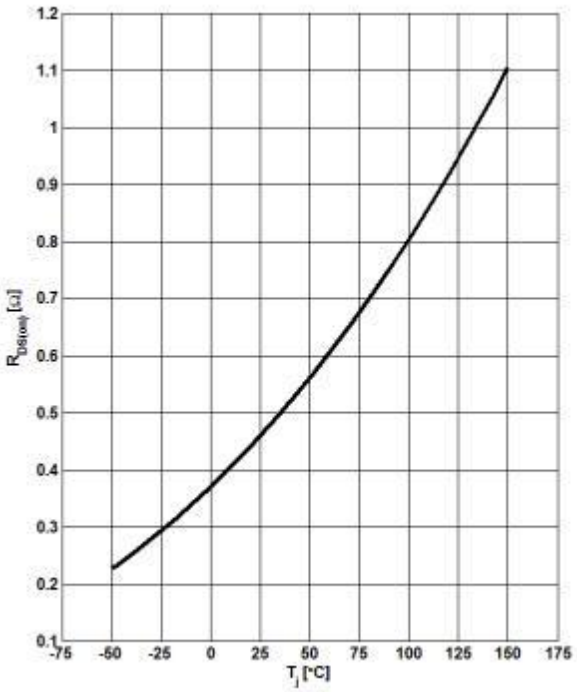
ID = f(VDS); Tj= 125ºC; parameter: VGS

Figure 9: Typ. Drain-Source On-State Resistance



RDS(ON) =f(ID); Tj=125ºC; parameter: VGS

Figure 10: Typ. Drain-Source On-State Resistance



RDS(ON)=f(Tj); ID=4.0A; VGS=10V

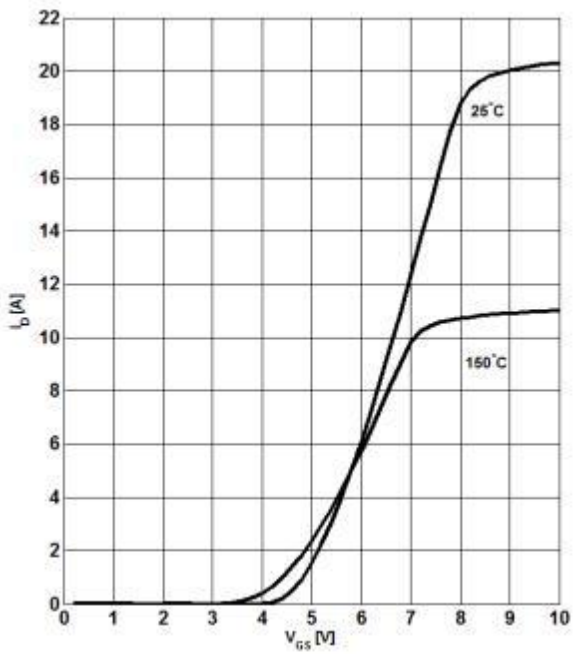
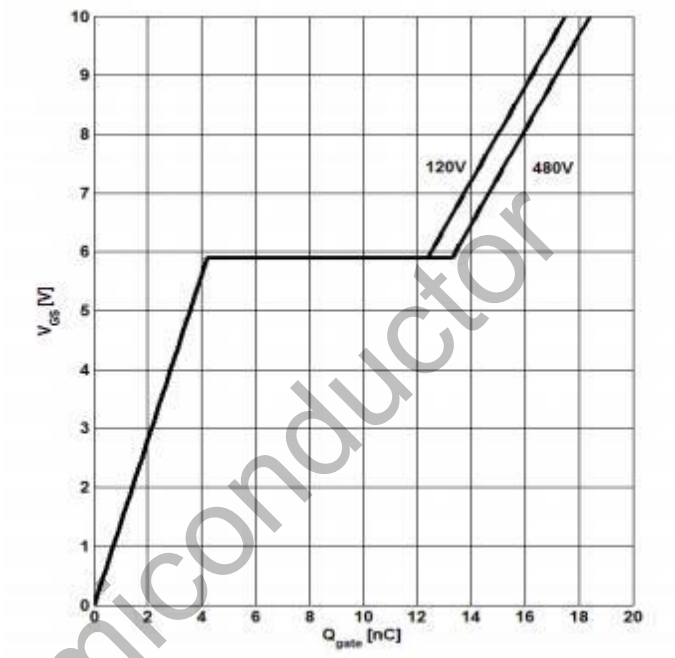
Figure 11: Typ. Transfer Characteristics	Figure 12: Typ. Gate Charge
	
ID = f(VGS); VDS = 20V	VGS= f(Qgate), ID=4.0A pulsed

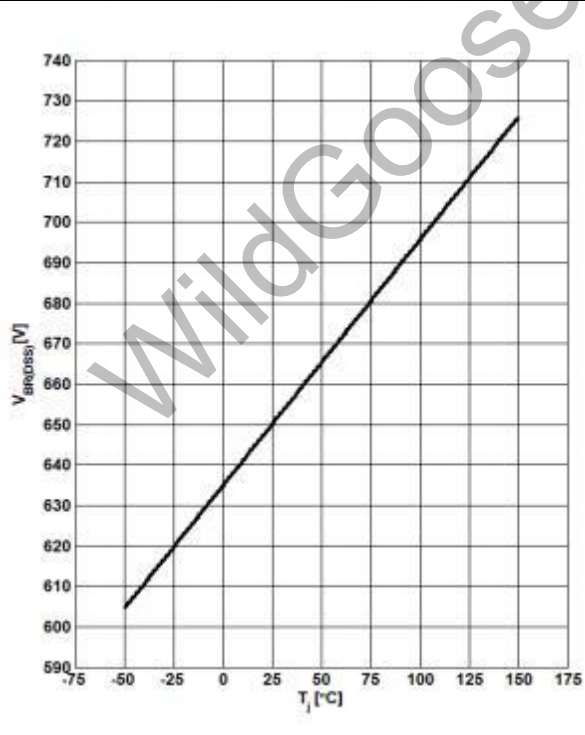
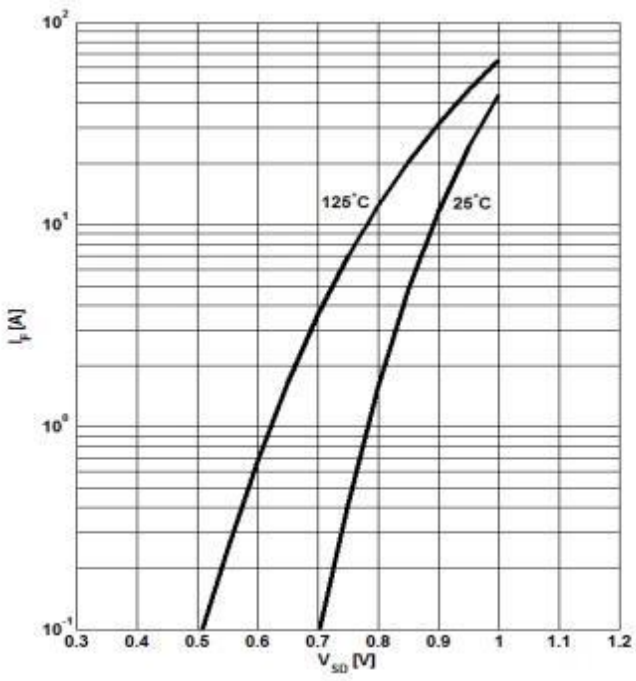
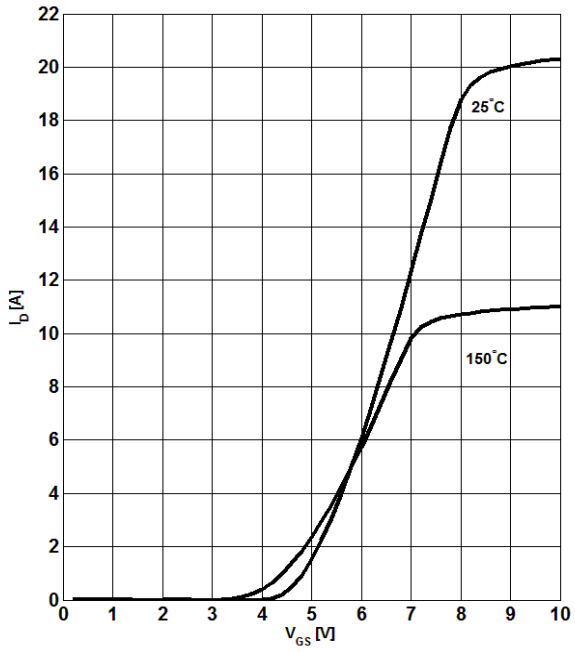
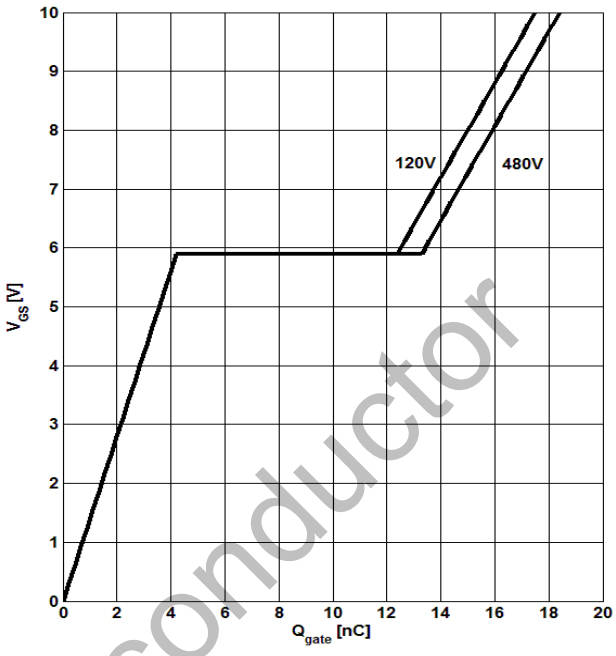
Figure 13: Drain-Source Breakdown Voltage	Figure 14: Forward Characteristics ofReverse Diode
	
VBR(DSS)=f(Tj); ID=1mA	IF=f(VSD); parameter: Tj

Figure 11: Typ. Transfer Characteristics



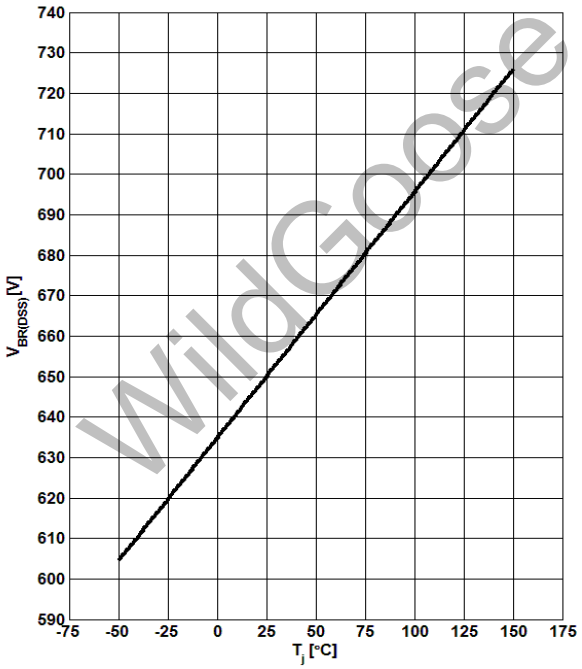
$I_D = f(V_{GS})$; $V_{DS} = 20V$

Figure 12: Typ. Gate Charge



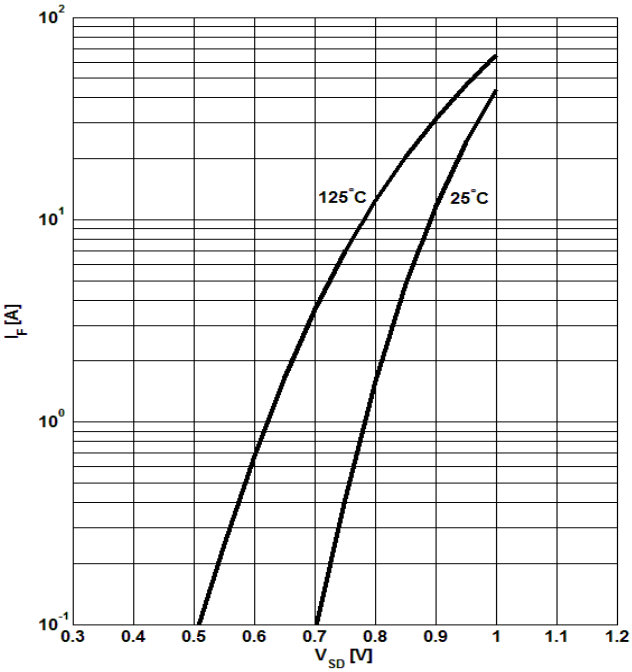
$V_{GS}= f(Q_{gate})$, I_D=4.0A pulsed

Figure 13: Drain-Source Breakdown Voltage



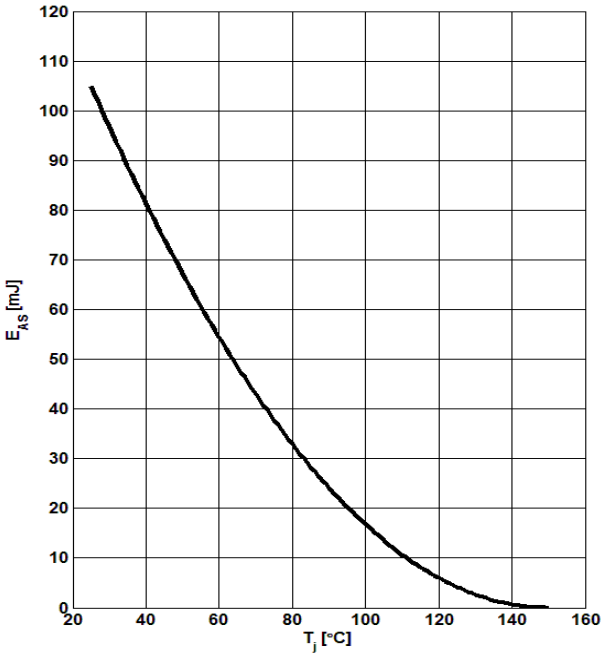
$V_{BR(DSS)}=f(T_j)$; I_D=1mA

Figure 14: Forward Characteristics of Reverse Diode



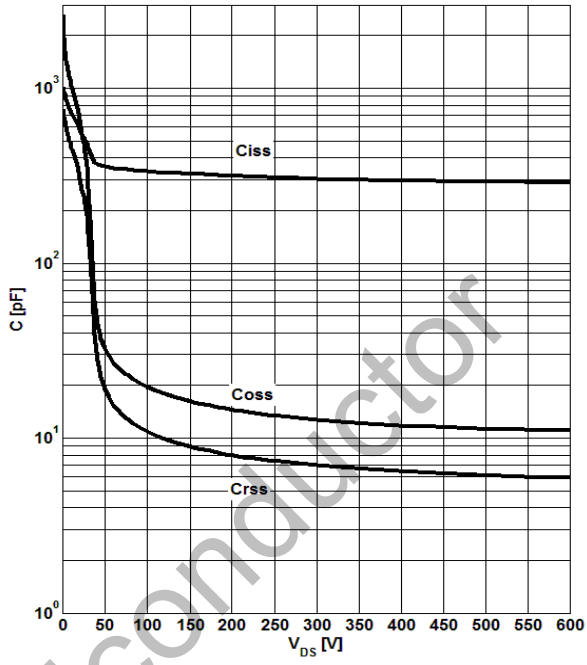
$I_F=f(V_{SD})$; parameter: T_j

Figure 15: Avalanche Energy



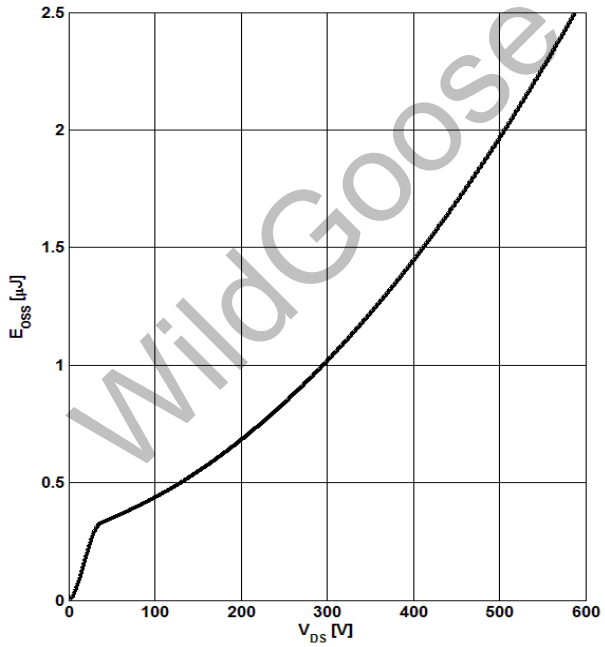
$E_{AS}=f(T_j)$; I_D=1.3A; V_{DD}=60V

Figure 16: Typ. Capacitances



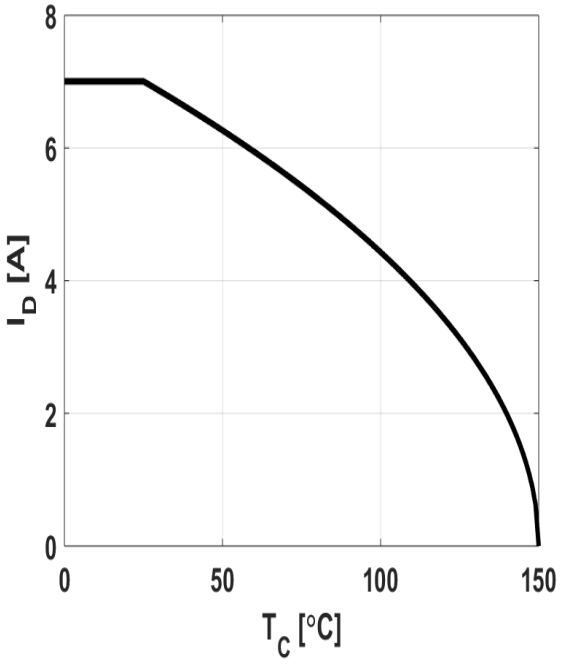
$C=f(V_{DS})$; V_{GS}=0; f=1MHz

Figure 17: C_{OSS} Stored Energy



$E_{OSS}=f(V_{DS})$

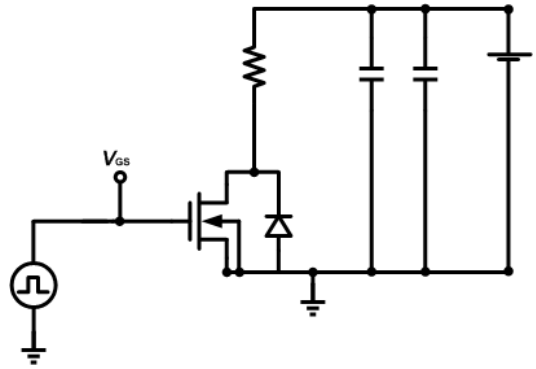
Figure 18: Drain current

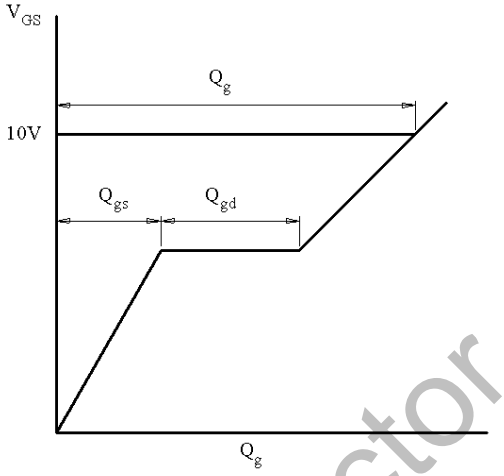


$I_D=f(T_C)$

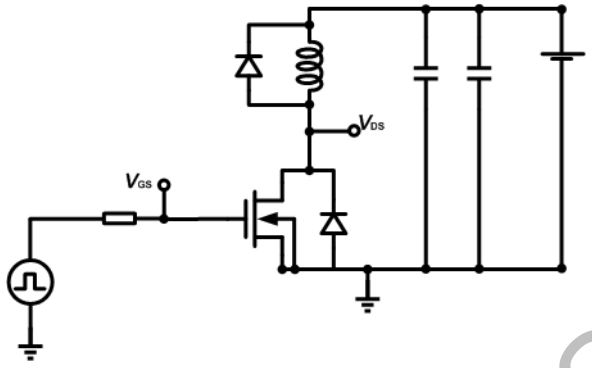
Test Circuits

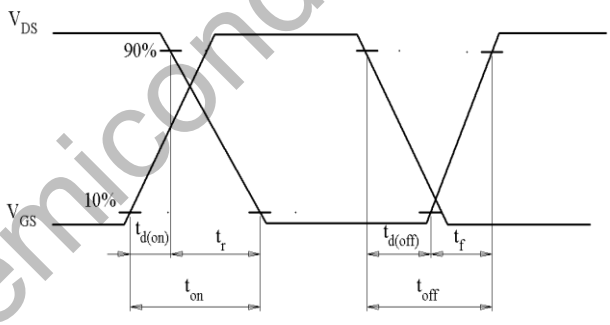
1. Gate Charge Test Circuit & Waveform



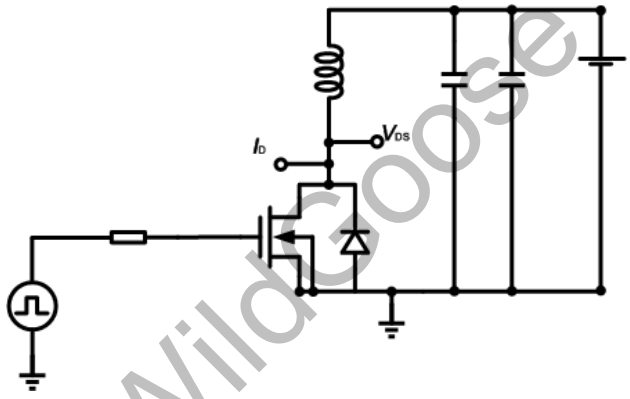


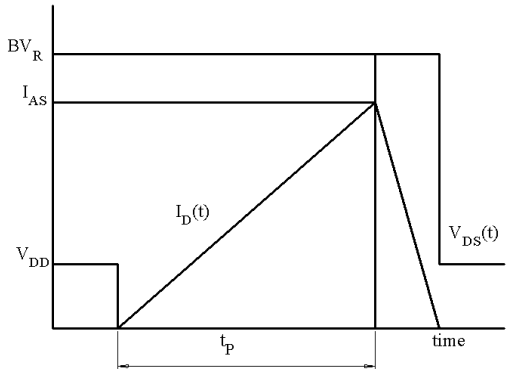
2. Switch Time Test Circuit



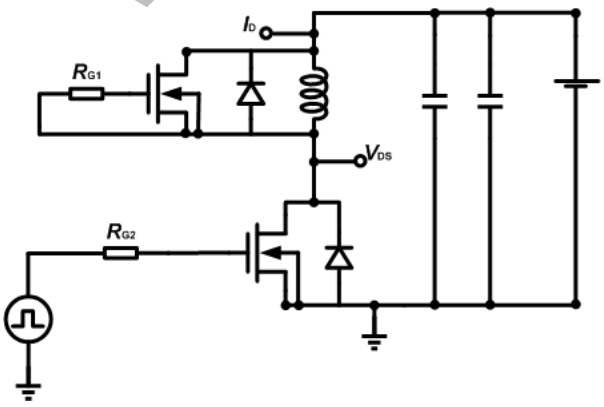


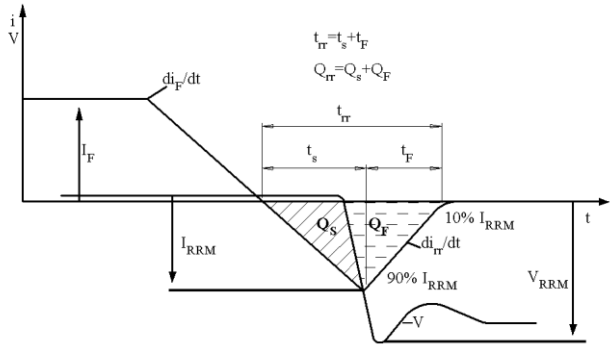
3. Unclaimed Inductive Switching Test Circuit & Waveforms





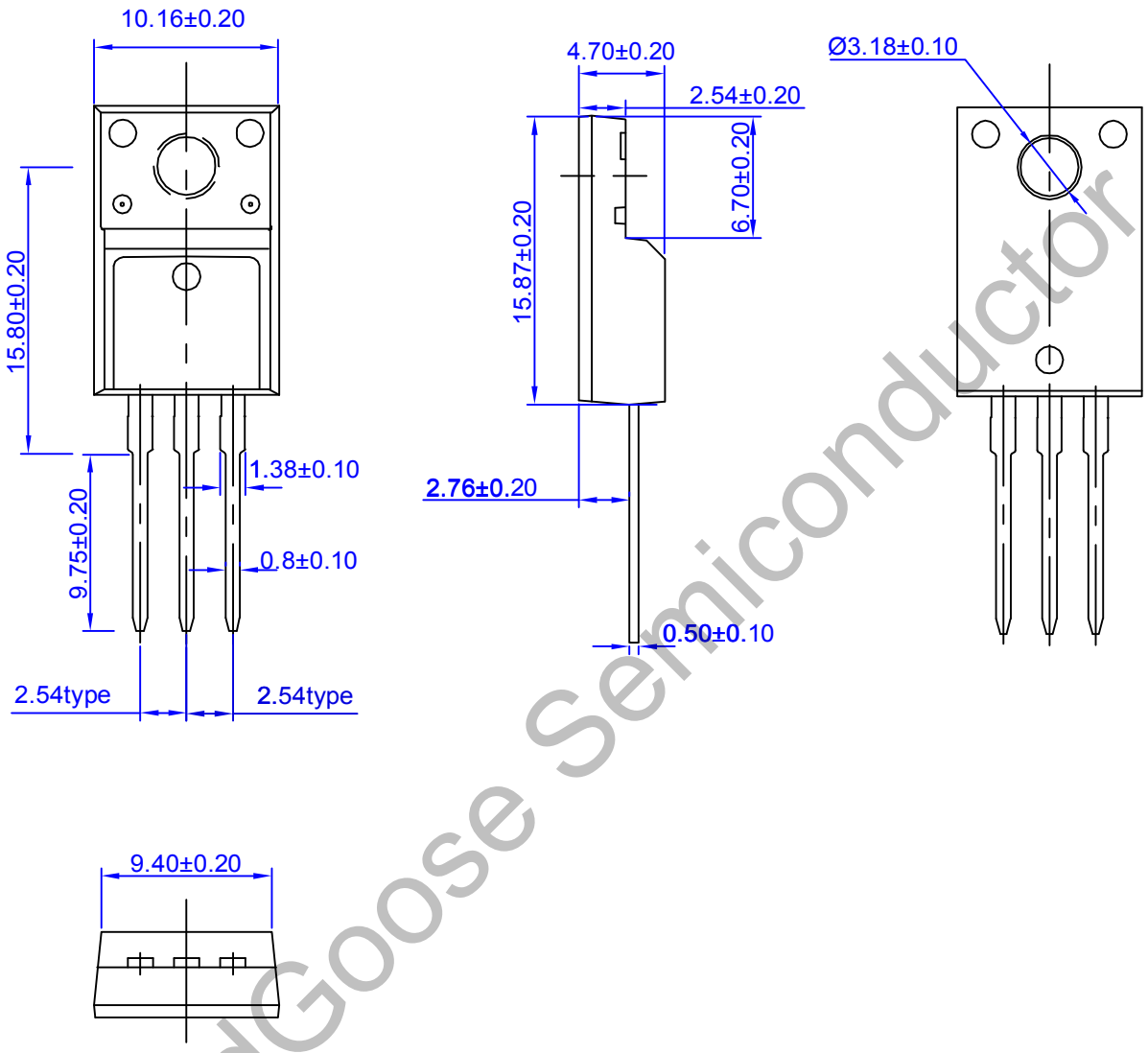
4. Test Circuit and Waveform for Diode Characteristics





Package Dimension

TO-220F



技术要求：

1.图中所指亚光面对应表面粗糙度Ra0.8，
光面对应表面粗糙度为Ra0.2

2.上、下塑封体错位≤0.1；塑封体中心与引线框架中心错位≤0.1

3.塑封体外形未注棱边R0.2

4.未标注公差±0.15

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