

## WD1038DH

**High Efficiency 5V, 3A continuous, 1.5MHz Synchronous Step-Down Regulator**

### Descriptions

WD1038DH is a high efficiency 1.5MHz synchronous step-Down DC/DC regulator capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.7V to 5.5V and integrate main switch and synchronous switch with very low  $R_{DS(on)}$  to minimize the conduction loss.

WD1038DH also provides over temperature protection (OTP), under-voltage lockout (UVLO),  $V_{out}$  short protection.

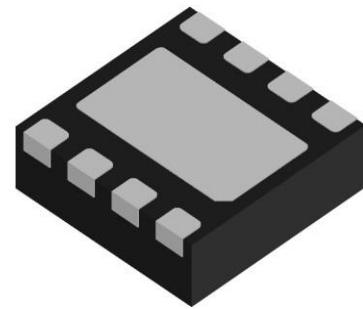
The WD1038DH is available in the DFN2x2-8L package. Standard product is Pb-Free and Halogen-Free.

### Features

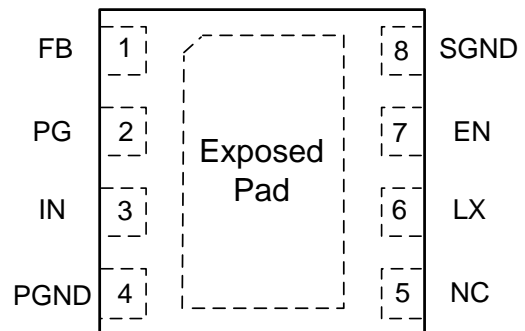
- Low  $R_{dson}$  internal Switches (top/bottom): 80/70m $\Omega$
- 2.7-5.5V input voltage range
- 3A continuous load current capability
- 1.5MHz switching frequency minimizes the external components
- 35uA low quiescent current
- Internal soft-start limits the inrush current
- Peak Current Mode Control
- 100% Duty-Cycle Mode
- Power-Good Output

### Applications

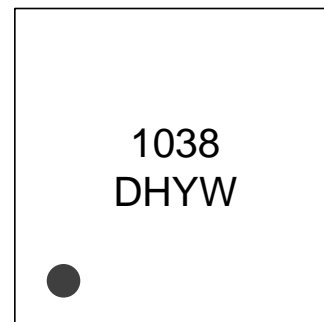
- Smart Phones
- TV
- Set Top Box and OTT box
- Access Point Router



**DFN2x2-8L Package**



**Pin configuration (Top view)**



**1038** = Device Code  
**DH** = Special code  
**Y** = Year Code  
**W** = Week Code  
**Marking**

### Order information

Device	Package	Shipping
WD1038DH-8/TR	DFN2x2-8L	3000/Reel&Tape

[Http://:www.sh-willsemi.com](http://www.sh-willsemi.com)

## Typical Applications

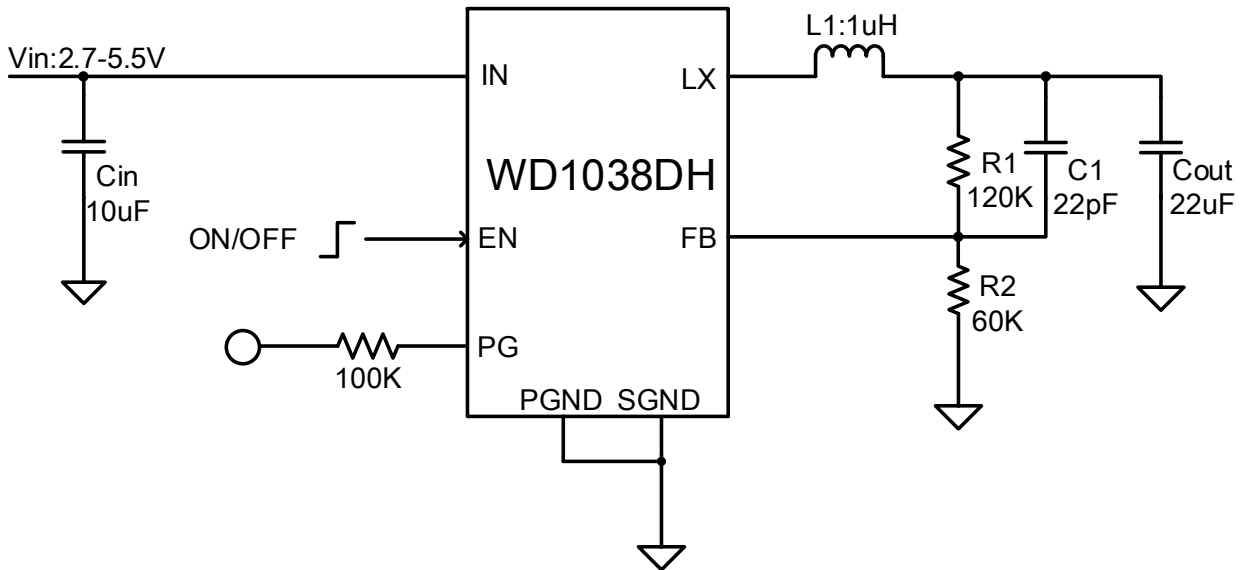


Fig1 Schematic Diagram

## Pin Descriptions

Pin Name	Pin Number	Pin Description
FB	1	Feedback pin. Connected to the feedback resistor for adjustable version or VOUT for fix output version.
PG	2	Power good indicator. The output of this pin is an open-drain with external pull-up resistor. PG is pulled up when the FB voltage is within 90%, otherwise it is LOW.
IN	3	Input pin. Decouple this pin to GND with at least 10uF ceramic Cap.
PGND	4	Power Ground.
NC	5	No Internal Connection.
LX	6	Inductor pin.
EN	7	Enable Control. Pull high to turn on. Do not leave it floating .
SGND	8	Signal Ground.
Exposed Pad		The exposed pad must be soldered to a large PCB and connected to PGND for maximum power dissipation.

**Absolute Maximum Ratings <sup>(1)</sup>**

Parameter	MIN	MAX	Unit
Power Supply VCC	-0.3	6.5	V
Others Pins	-0.3	VCC+0.6	V
Power Dissipation, P <sub>D</sub> @ T <sub>A</sub> =25°C, DFN2X2-8L		2.19	W
Package Thermal Resistance T <sub>JA</sub>		50	°C/W
Package Thermal Resistance T <sub>JC</sub>		8	°C/W
Junction Temperature T <sub>J</sub>		150	°C
Lead Temperature (Soldering, 10 sec)		260	°C
Storage Temperature Range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**Recommended Operating Conditions**

Parameter	MIN	MAX	Unit
Power Supply VCC	2.7	5.5	V
Junction temperature T <sub>J</sub>	-40	125	°C
Ambient temperature T <sub>A</sub>	-40	85	°C

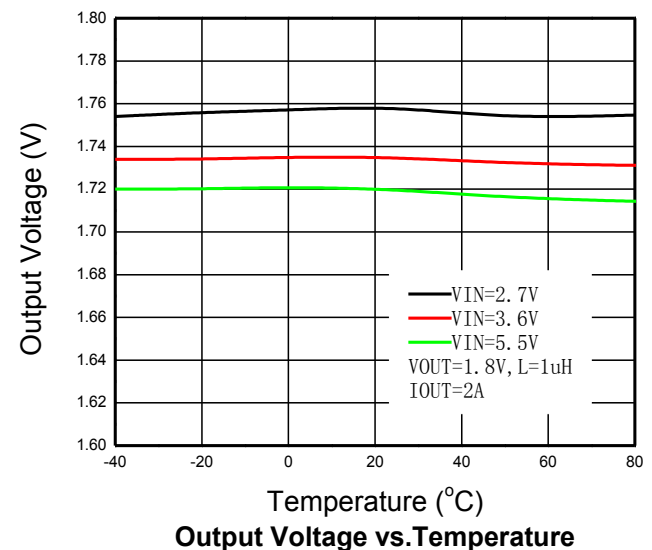
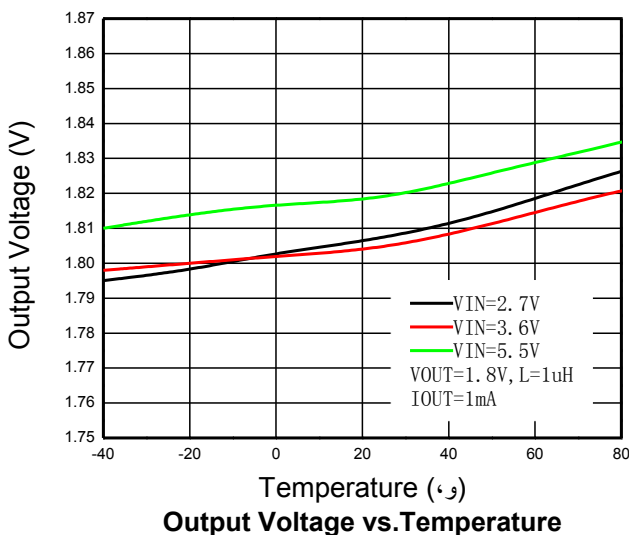
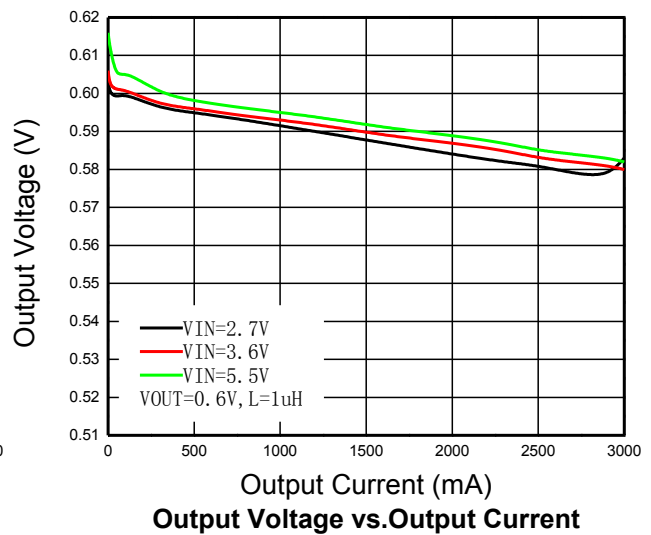
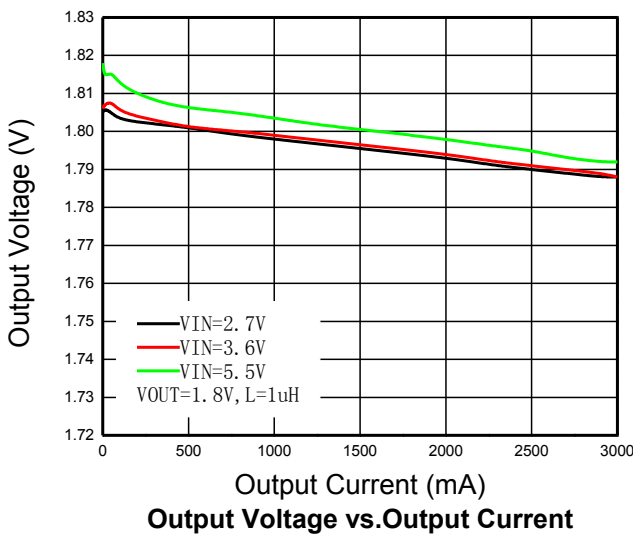
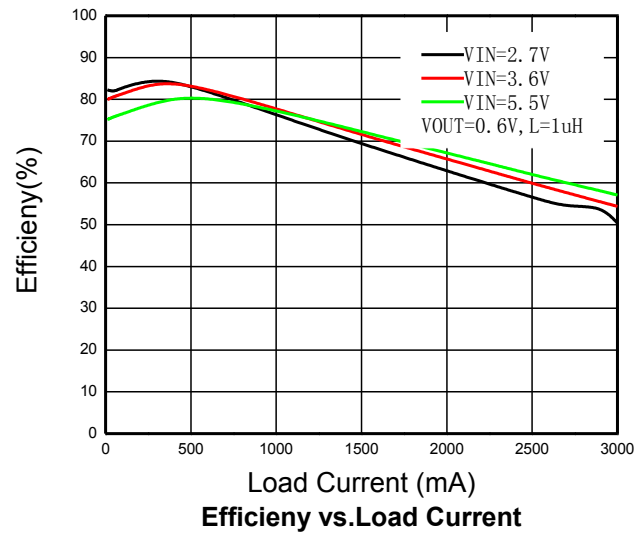
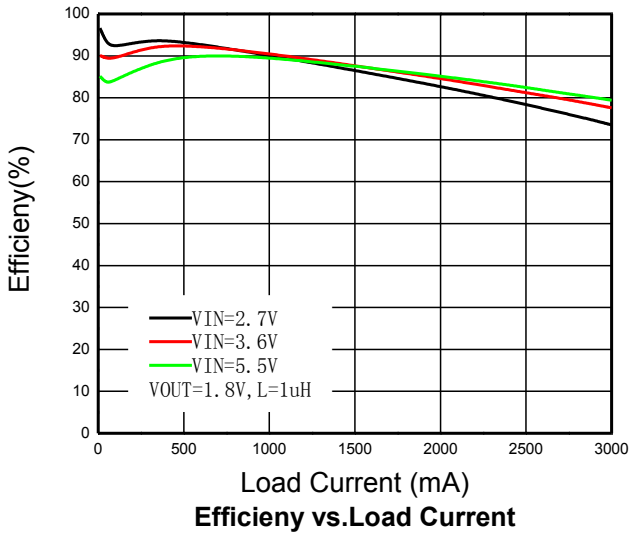
## Electronics Characteristics

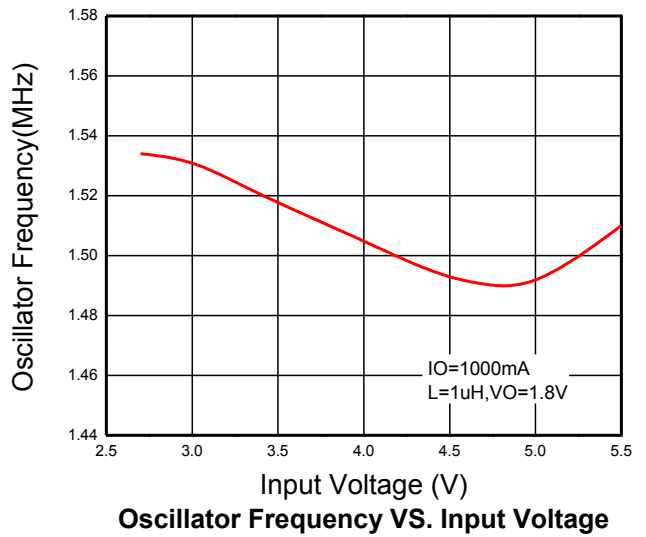
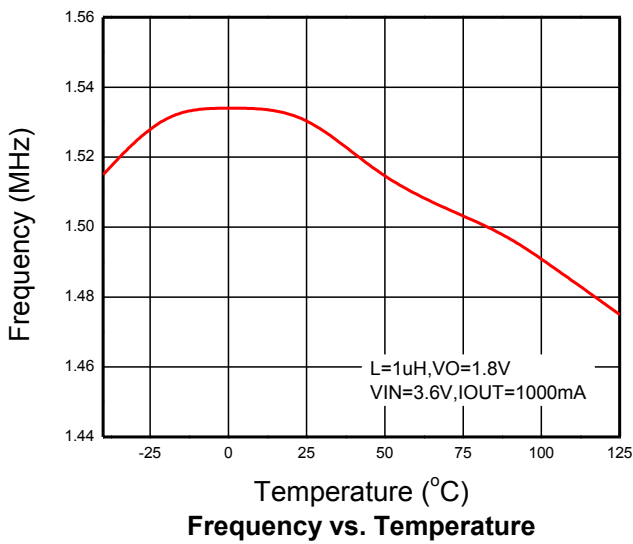
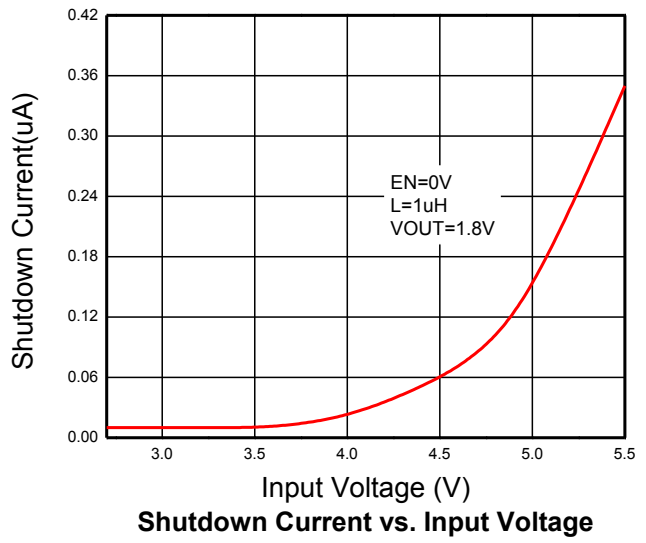
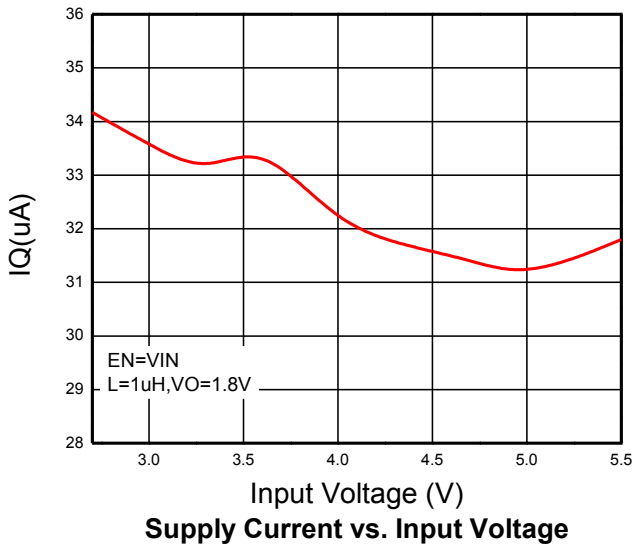
Unless otherwise specified: limits for typical values are for  $T_A = 25^\circ\text{C}$  and minimum and maximum limits apply over the operating ambient temperature range ( $-40^\circ\text{C} < T_A < 85^\circ\text{C}$ );  $V_{IN}=4.2\text{V}$ ,  $V_{out}=2.5\text{V}$ ,  $L1=1\mu\text{H}$ ,  $C_{out}=22\mu\text{F}$ .

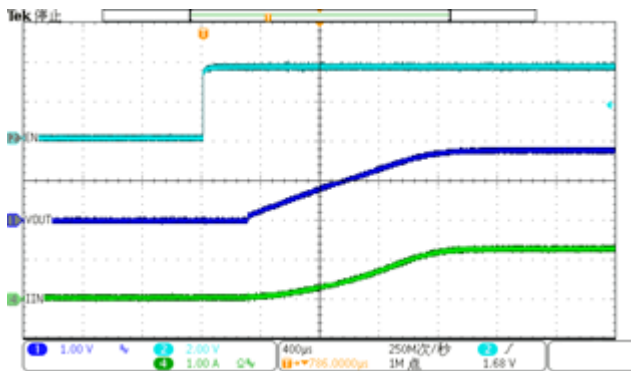
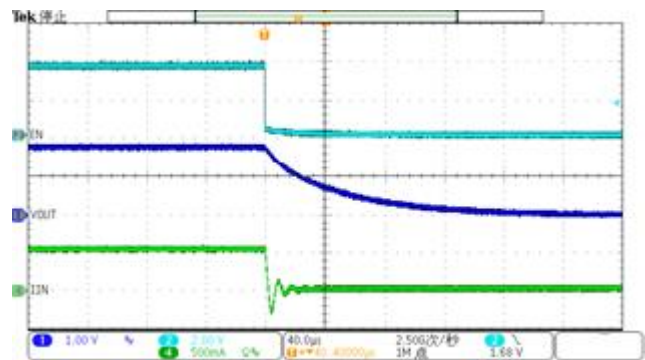
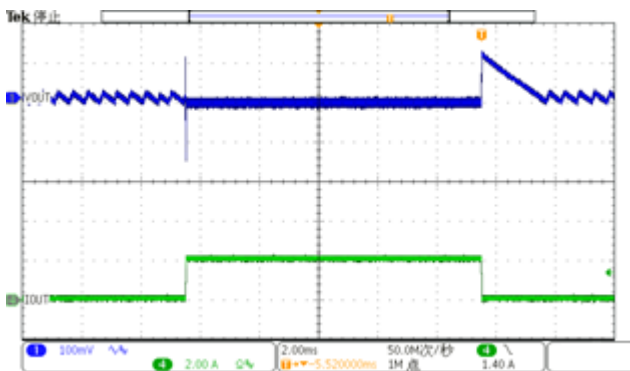
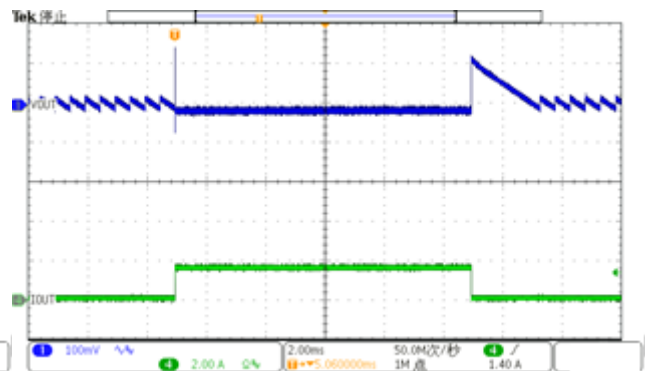
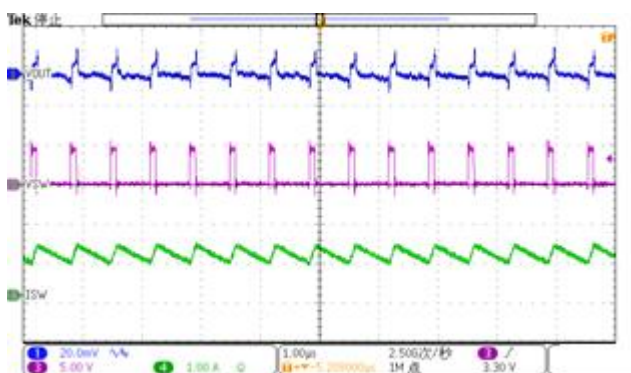
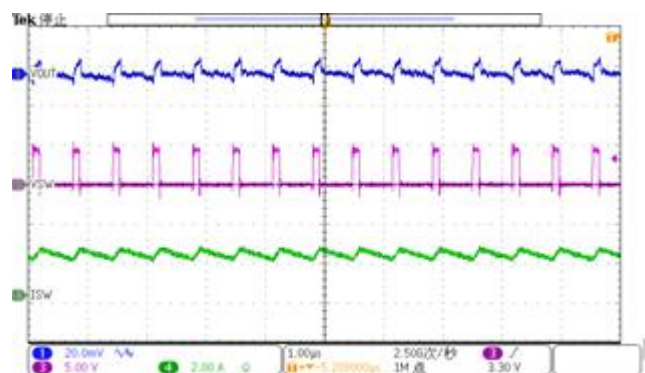
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Operation Voltage Range	$V_{IN}$		2.7		5.5	V
VIN Under Voltage	$V_{UVLO-H}$	$V_{IN}$ Rising		2.45		V
Lockout	$V_{UVLO-L}$	$V_{IN}$ Falling		2.35		V
Quiescent Current	$I_Q$	Switching		35		uA
		$V_{FB}=0.63\text{V}$ , Non Switching		27		
Shutdown Current	$I_{SD}$	$V_{EN} = \text{GND}$ , $V_{IN} = 3.6\text{V}$			1	$\mu\text{A}$
Feedback Reference	$V_{REF}$		0.588	0.6	0.612	V
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$			0.35		%/V
PFET Rdson	$R_{dson P}$			80		m $\Omega$
NFET Rdson	$R_{dson N}$			70		
PFET Current Limit	$I_{LIMT}$			4.5		A
Oscillator Frequency	$F_{OSC}$			1.5		MHz
Max Duty Cycle				100		%
Soft Start Time				800		$\mu\text{S}$
Power on delay time				25		$\mu\text{S}$
Input OVP shutdown	$V_{OVP}$	Rising		6.4		V
		Falling	5.7	6.1		V
Over Volatage Protection Blanking Time				20		$\mu\text{S}$
Thermal Shutdown				150		$^\circ\text{C}$
Thermal Shutdown Hysteresis				25		$^\circ\text{C}$
EN Input LOW Voltage	$V_{IL}$				0.4	V
EN Input HIGH Voltage	$V_{IH}$		1.4			V

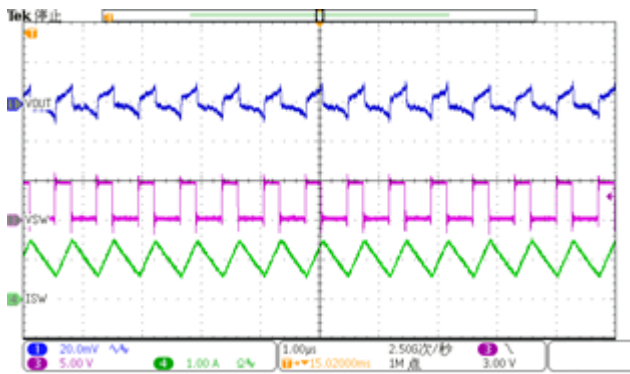
### Typical Characteristics

( $T_a=25^{\circ}\text{C}$ ,  $V_{IN}=5\text{V}$ ,  $V_{EN}=V_{IN}$ ,  $C_{IN}=10\mu\text{F}$ ,  $C_{OUT}=22\mu\text{F}$ ,  $L=1\mu\text{H}$ , unless otherwise noted)

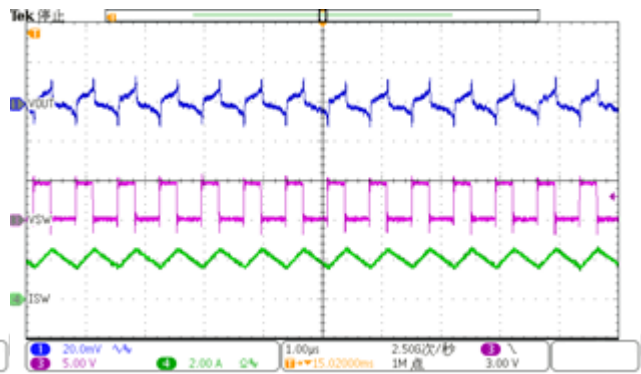




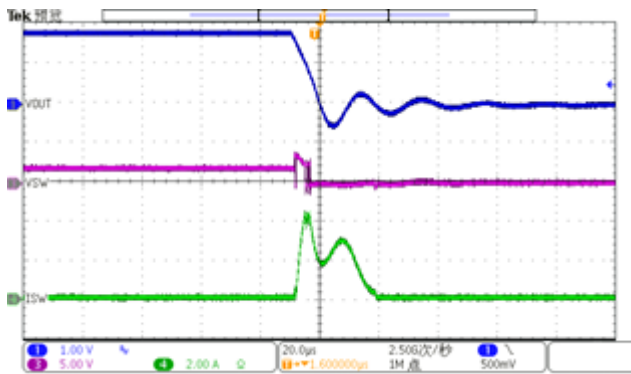

**VIN=3.6V, VO=1.8V, EN=3.6V, IO=2A, EN On**

**VIN=3.6V, VO=1.8V, EN=3.6V, IO=1A, EN Off**

**Load Transient Response  
VIN=5V, VO=1.8V, EN=3.6V, IO=1mA-2A**

**Load Transient Response  
VIN=5V, VO=0.6V, EN=5V, IO=1mA-2A**

**Ripple : VIN=5.0V, VO=0.6V, EN=3.6V IO=1A**

**Ripple : VIN=5.0V, VO=0.6V, EN=3.6V IO=2A**



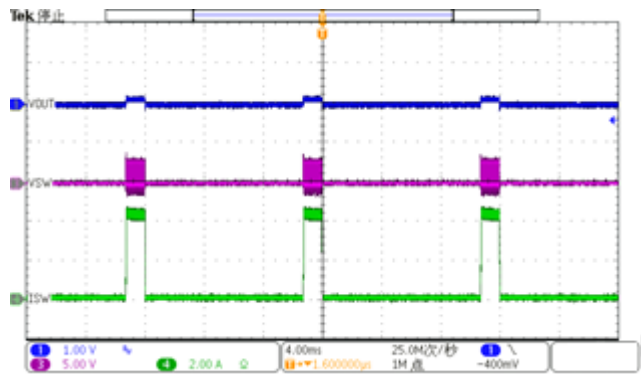
Ripple : VIN=5.0V, VO=1.8V, EN=3.6V IO=1A



Ripple : VIN=5.0V, VO=1.8V, EN=3.6V IO=2A



VIN=3.6V, VO=1.8V, EN=3.6V VOUT short





## Operation Information

WD1038DH is a high efficiency 1.5MHz synchronous Step-Down DC/DC regulator IC capable of delivering up to 3A output current. It can operate over a wide input voltage range from 2.7V to 5.5V and integrate main switch and synchronous switch with very low  $R_{DS(on)}$  to minimize the conduction loss.

## Application Information

Because of the high integration in the WD1038DH IC, the application circuit based on this regulator IC is rather simple. Only input capacitor  $C_{in}$ , output capacitor  $C_{out}$ , output inductor  $L$  and feedback resistors ( $R_H$  and  $R_L$ ) need to be selected for the targeted applications specifications.

### Feedback resistor dividers $R_H$ and $R_L$ :

Choose  $R_H$  and  $R_L$  to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose larger resistance values for both  $R_H$  and  $R_L$ . A value of between 100k $\Omega$  and 1M $\Omega$  is highly recommended for both resistors. If  $R_L = 120k\Omega$  is chosen, then  $R_H$  can be calculated to be:

$$R_H = \frac{(V_{out} - 0.6V) * R_L}{0.6V}$$

### Input capacitor $C_{IN}$ :

A Typical X7R or better grade ceramic capacitor with 10V rating and greater than 10uF capacitor is recommended. To minimize the potential noise problem, place this ceramic capacitor really close to the  $V_{IN}$  and GND pins. Care should be taken to minimize the loop area formed by  $C_{IN}$ , and  $V_{IN}/GND$  pins.

### Output inductor $L$ :

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired

ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{out}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX \times 40\%}}$$

Where  $F_{sw}$  is the switching frequency and  $I_{out,max}$  is the maximum load current.

2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{out}/V_{IN,MAX})}{2 * F_{SW} * L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with  $DCR < 25m\Omega$  to achieve a good overall efficiency.

### Inductor vs. Output Capacitor:

The ripple base control strategy need very little  $C_{OUT}$  to confirm stability. Too large inductor and  $C_{OUT}$  will lead to instability.

### Power good:

The WD1038DH has a power good output. The PG pin goes high impedance once the output is above 90% and below 110% of the nominal voltage, and is driven low once the output voltage falls below typically 85% or above 115% of the nominal voltage. The PG pin is an open-drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5 V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

### OCP and SCP protection :

With load current increasing, the PFET current will get higher till reach the current limit of PFET. The

PFET current limit will turn off the PFET till the next clock is coming. If the load current continues to increase, the output voltage will drop. When the output voltage falls below 30% of the regulation level, output short is detected and the IC will work in hiccup mode. During the hiccup, the regulator waits every 8 soft-start time before a soft-start. If at the time of soft-start finish, VOUT is still below 30% of the regulation level, the regulator will wait another 8 soft-start time before another soft-start. The hiccup reduces the power dissipation of the IC under short circuit conditions. If the hard short is removed, IC will go back to normal operation.

### Layout Consideration

The layout design of WD1038DH regulator is relatively simple. For the best efficiency and minimum noise problems, we should place the following components close to the IC: Cin, L, RH and

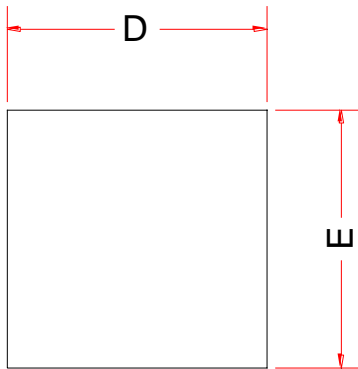
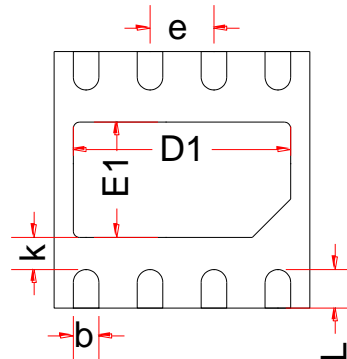
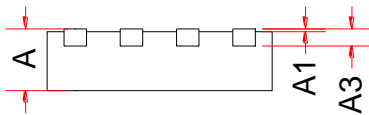
RL.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

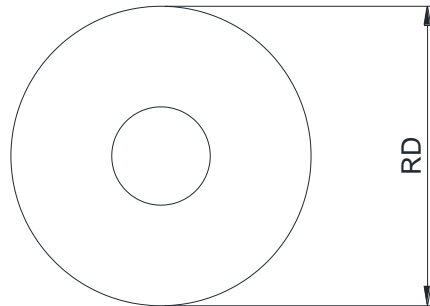
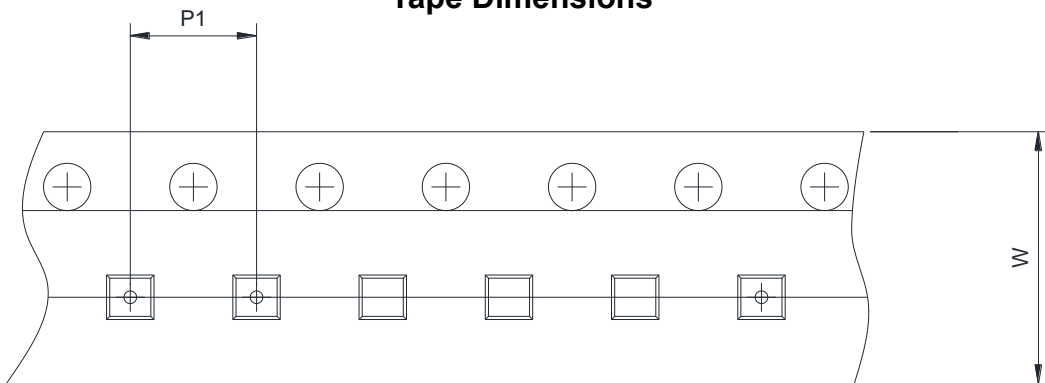
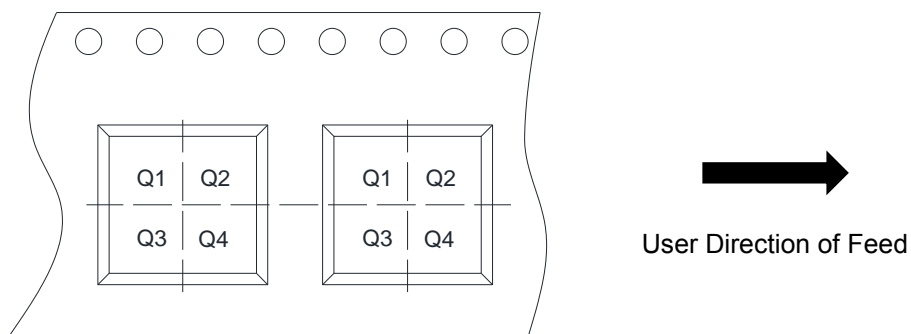
2) Cin must be close to Pins VIN and GND. The loop area formed by Cin and GND must be minimized. Cout must be close to the Chip, too.

3) The PCB copper area associated with SW pin must be minimized to avoid the potential noise problem.

4) The components RH and RL, and the trace connecting to the FB pin must NOT be adjacent to the SW net on the PCB layout to avoid the noise problem.

**PACKAGE OUTLINE DIMENSIONS**
**DFN2x2-8L**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.50	0.55	0.60
A1	0.00		0.05
A3	0.15Ref		
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D1	1.60	1.70	1.80
E1	0.80	0.90	1.00
k	0.20	-	-
b	0.15	0.20	0.25
e	0.50BSC		
L	0.25	0.30	0.35

**TAPE AND REEL INFORMATION**
**Reel Dimensions**

**Tape Dimensions**

**Quadrant Assignments For PIN1 Orientation In Tape**


RD	Reel Dimension	<input checked="" type="checkbox"/> 7inch	<input type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm	<input type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input checked="" type="checkbox"/> 4mm <input type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input type="checkbox"/> Q3 <input type="checkbox"/> Q4

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[ISL6421ERZ](#)