WL2868C

7-Channel LDO PMIC for Camera Applications

www.omnivision-group.com

Descriptions

The WL2868C is PMIC with 7 integrated LDOs, the PMIC has 2 low dropout LDOs for high current DVDD and 5 high PSRR LDOs for noise sensitive power rails. WL2868C has 5 independent input pins for the individual LDOs, VIN12 is for LDO1 and LDO2, VIN34 is for LDO3 and LDO4, VIN5 for LDO5, VIN6 for LDO6 and VIN7 for LDO7. WL2868C has a separate system input VSYS which is the bias pin for the LDOs.

The LDOs' output voltage and power up sequence can be set through the I2C interface. WL2868C also integrated the fault monitoring features with interrupt indication

The 7bit I2C address of the device is default to 0101 111 but can be reprogramed so as multiple devices can be connected to the same I2C bus.

WL2868C is available in 1.54x1.87mm^2 20 ball WCSP package. The device is Pb-free and halogen-free.

Features:

VIN12 input voltage :0.6 V~3 V

LDO1/2 output current :1200 mA

LDO1/2 output :0.496 V~1.512 V@8 mV/step

LDO1/2 dropout :80 mV@1.2 V,800 mA output

LDO1/2 PSRR :70 dB@f=1 KHz

VIN3-VIN7 input voltage:2.1 V~5.5 V

LDO3-LDO7 output current:400 mA

LDO3 to LDO7 output :1.504 V~3.544 V@8 mV/step

LDO3 to LDO7 dropout :80 mV@2.8 V,300 mA

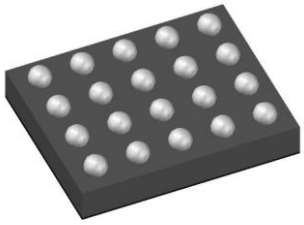
LDO3 to LDO7 PSRR :96 dB@f=1 KHz

Programmable VSYS UVLO

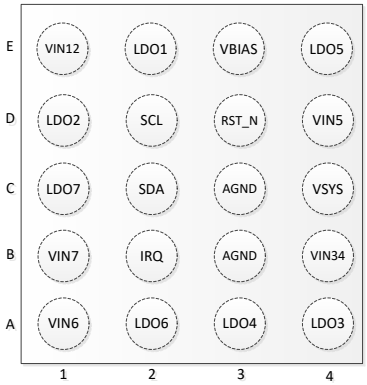
Fault Interrupt

Over temperature protection

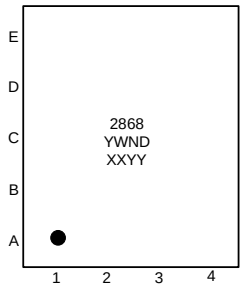
Programmable power up sequence



CSP-20L (Bottom View)



Pin Configuration (Top View)



Marking

2868 : Device Code

Y : Year Code (A~Z)

W : Week Code (A~z)

N : Order Number (A~Z)

D : Wafer Information

XXYY : Die Coordination

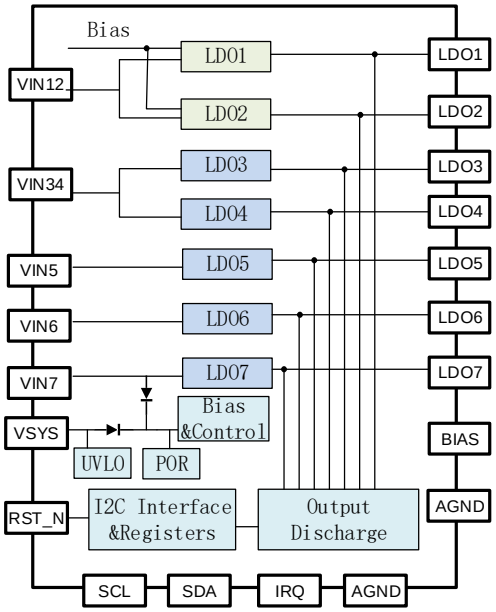
Order Information

Device	Package	Shipping
WL2868C-20/TR	CSP-20L	3000/Reel&Tape

Applications:

- Smart Phone
- IP Camera
- Camera Module

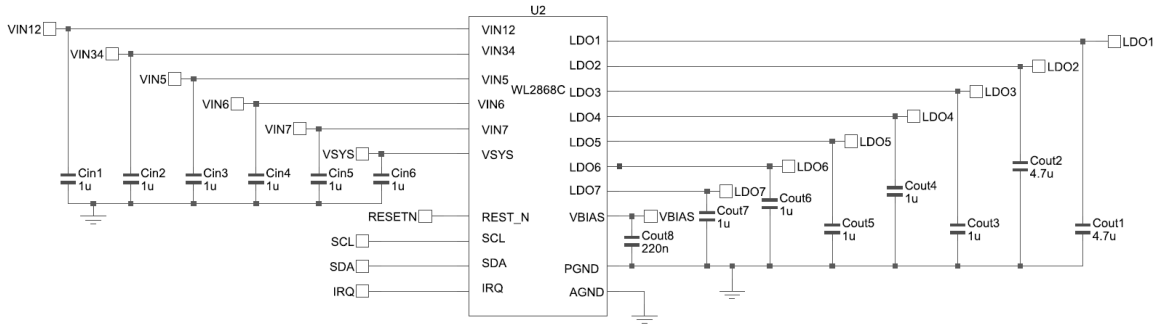
Block Diagram



PIN Descriptions

Pin No.	Symbol	Description
A1	VIN6	LDO6 input
A2	LDO6	LDO6 output
A3	LDO4	LDO4 output
A4	LDO3	LDO3 output
B1	VIN7	LDO7 input
B2	IRQ	Fault interrupt pin is active high indicating an interrupt event has occurred. This pin returns to low when all I2C interrupt bits equal 0
B3	AGND	Ground
B4	VIN34	LDO3 and LDO4 input
C1	LDO7	LDO7 output
C2	SDA	I2C data line
C3	AGND	Ground
C4	VSYS	VSYS input
D1	LDO2	LDO2 output
D2	SCL	I2C clock
D3	RST_N	RST_N pin is used to enable basic circuits necessary for controlling the PMIC. The pin has an internal 4MΩ (typ.) pull-down and should always be connected to a logic high or low.
D4	VIN5	LDO4 input
E1	VIN12	LDO1 and LDO2 input
E2	LDO1	LDO1 output
E3	VBIAS	Bias bypass pin. Connect a 0.1uF~0.47uF capacitor between this pin and analog ground.
E4	LDO5	LDO5 output

Typical Applications



Note: If use the 0201 package ceramic capacitors, change Cout3~Cout7 to 2.2uf /0201 /6.3V X5R ceramic type.

Absolute Maximum Ratings

Parameter		Value	Unit
VIN Range (VIN1 ,VIN2)		−0.3 ~ 3.0	V
VIN Range(V_{SYS})		−0.3 ~ 6.5	V
VIN Range (VIN34, VIN5,VIN6,VIN7)		−0.3 ~ 5.5	V
Control Pin(SCL, SDA, IRQ, RST_N)		−0.3 ~ V_{SYS} + 0.3	V
Current on Single Pin		1500	mA
Lead Temperature (10 S)		260	°C
Storage Temperature Range		-55 ~150	°C
Operating Junction Temperature Range		-40 ~150	°C
ESD Ratings	HBM	7000	V
	MM	300	V

These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability

Recommend Operating Ratings

Parameter	Value	Unit
VIN12 Operating Supply Voltage Range	0.6~3.0	V
VIN3 to VIN7 Operating Supply Voltage Range	2.1~V_{SYS}	V
VSYS	3.1 ~5.5	V
Operating Temperature Range	-40～85	°C
Thermal Resistance, $R_{\theta JA}$ (note)	148	°C/W

Note:

Surface mounted on FR4 Board using 1.5*1.5 $inch^2$ FR4 copper (1 $inch^2$/1 Oz)

Electrical Specification

(Minimum and maximum values are at VSYS = 3 to 5.5V; VIN12 = 0.5 to 3V & VIN12 >=VLDO1/2 + 200mV; VIN34/5/6/7 = 2.0 to 5.5V &VIN34/5/6/7 >=VLDO3/4/5/6/7 + 300mV respectively. TJ = -40°C to +125°C unless otherwise noted. Typical values are at T_A = 25°C; VSYS= 3.8V; VIN12 = 1.5V; VIN34 = VIN5 = VIN6 = VIN7 = 3.6V; VLDO1/2 = 1.2V, VLDO3/4/5/6/7 = 2.8V.)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Voltage Range	VSYS		3.1		5.5	V
	VIN34, VIN5, VIN6, VIN7		2.1		5.5	V
	VIN12		0.6		3.0	V
Output Voltage Accuracy	LDO1 & 2		-1.5		+1.5	%
	LDO3,4,5,6 & 7		-1.5		+1.5	%
VSYS Undervoltage Lockout Threshold	$VSYS_{UVLO}$	Rising	2.9	3.0	3.1	V
		Falling	2.75	2.85	2.95	V
V_{IN12} Undervoltage Lockout Threshold	$VIN12_{UVLO}$	Rising			0.6	V
		Falling	0.4			V
$V_{IN34567}$ Undervoltage Lockout Threshold	$VIN34567_{UVLO}$	Rising		1.9	2.1	V
		Falling	1.7	1.8		V
Supply Quiescent Current	I_{GND}	RST_N="1", All channels are OFF		45		μA
		LDO1 is "ON"		62		μA
		LDO1&2 are "ON"		80		μA
		LDO1,2&3 are "ON"		98		μA
		LDO1,2,3&4 are "ON"		115		μA
		LDO1,2,3,4&5 are "ON"		132		μA
		LDO1,2,3,4,5&6 are "ON"		150		μA
		LDO1,2,3,4,5,6&7 are "ON"		166		μA
		RST_N=5.5V, Disable IC Through I2C		2		μA
Supply Current Shutdown	I_{SD}	EN = GND, V_{IN} = 3.6V		2		μA

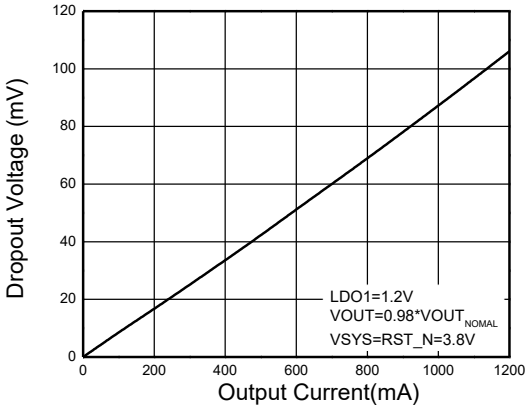
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Voltage Range	LDO1 & 2	When V_{OUT}+200mV<=V_{VIN12}, V_{SYS}>=3V & V_{SYS}>=V_{OUT}+1.5V	0.496		1.512	V
	LDO3 & 4	When V_{OUT}+200mV<=V_{VIN34} & V_{VIN34}>=2V, V_{SYS}>=3V & V_{SYS}>=V_{VIN34}	1.504		3.544	V
	LDO5	When V_{OUT}+200mV<=V_{VIN5} & V_{VIN5}>=2V, V_{SYS}>=3V & V_{SYS}>=V_{VIN5}				V
	LDO6	When V_{OUT}+200mV<=V_{VIN6} & V_{VIN6}>=2V, V_{SYS}>=3V & V_{SYS}>=V_{VIN6}				V
	LDO7	When V_{OUT}+200mV<=V_{VIN7} & V_{VIN7}>=2V. V_{SYS}>=3V				V
Dropout Voltage	LDO1 & 2	I_{OUT_Target}=1000mA, V_{OUT_Target} =1.2V, V_{SYS}=3.6V		90		mV
	LDO3,4,5,6 & 7	I_{OUT_Target}=300mA, V_{OUT_Target}=2.8V, V_{SYS}=3.6V		80		mV
Max Load Current	LDO1 & 2		1200			mA
	LDO3,4,5,6 & 7		400			mA
Line Regulation_VSYS	ΔVOUT1 & 2	V_{OUT}=1.2V ,I_{OUT}=1mA , V_{VIN12}=1.5V ,V_{SYS}=3.5V~5.5 V		0.5		mV
	ΔVOUT3,4,5,6 & 7	V_{OUT}=2.8V ,I_{OUT}=1mA , V_{VIN_Target}=3.3V , V_{SYS}=3.5V~5.5V		0.1		
Line Regulation_VIN	ΔVOUT1 & 2	V_{SYS}=5.5V,V_{OUT}=1.2V, I_{OUT}=1mA ,V_{VIN12}=1.5V~3V		0.1		mV
	ΔVOUT3,4,5,6 & 7	V_{SYS}=5.5V,V_{OUT_Target}=2.8V, I_{OUT}=1mA , V_{VIN_Target}=3.3V~5.5V		0.1		
Load Regulation	ΔVOUT1 & 2	I_{OUT_Target}=1mA ~ 1000mA		6		mV
	ΔVOUT3,4,5,6 & 7	I_{OUT_Target}=1mA ~ 250mA		3		

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output Current Limit	LDO1 & 2	V_{OUT}=90%$V_{OUT(NOM)}$	1200	1600	2000	mA
	LDO3,4,5,6 & 7		400	550	700	
Short Circuit Current	LDO1 & 2	V_{OUT}=90%$V_{OUT(NOM)}$	380	420	460	mA
	LDO3,4,5,6 & 7		150	200	250	
Turn-On Time	LDO1 & 2	V_{OUT_Target}=1.2V, C_{OUT_Target}=4.7uF, From assertion of Enable Signal to V_{OUT} start ramp up		25		uS
	LDO3,4,5,6 & 7	V_{OUT_Target}=2.8V, C_{OUT_Target}=1uF, From assertion of Enable Signal to V_{OUT} start ramp up		25		uS
Soft Start Time	LDO1 & 2	V_{OUT_Target}=1.2V, C_{OUT_Target}=4.7uF, V_{OUT} from 0 to 95% V_{OUT}		60		uS
	LDO3,4,5,6 & 7	V_{OUT_Target}=2.8V, C_{OUT_Target}=1uF, V_{OUT} from 0 to 95% V_{OUT}		80		uS
Output Noise	LDO1 & 2	f=10Hz to 100kHz, I_{OUT_Target}=1mA		20		uVrms
	LDO3,4,5,6 & 7	f=10Hz to 100kHz, I_{OUT_Target}=1mA		14		uVrms
Power Supply Rejection Ratio	LDO1 & 2 (V_{SYS} to V_{OUT}) V_{VIN12}=1.5V, V_{SYS}=3.8V+0.2V_{PP}, V_{OUT_Target}=1.2V, I_{OUT_Target}=150mA, C_{IN_Target}=1uF, C_{OUT_Target}=4.7uF	f=100 Hz		75		dB
		f=1kHz		70		dB
		f=10 kHz		65		dB
		f=100 kHz		45		dB
		f=1MHz		25		dB
	LDO1 & 2 (V_{VIN12} to V_{OUT}),V_{VIN12}=1.5V+0.2V_{PP}, V_{SYS}=3.8V, V_{OUT_Target}=1.2V, I_{OUT_Target}=150mA, C_{IN_Target}=1uF, C_{OUT_Target}=4.7uF	f=100 Hz		70		dB
		f=1kHz		70		dB
		f=10 kHz		65		dB
		f=100 kHz		50		dB
		f=1MHz		42		dB
	LDO3,4,5,6 & 7 (V_{SYS} to V_{OUT}) V_{VIN12}=1.5V,V_{IN_Target}=3.6, V_{SYS}=3.8V+0.2V_{PP}, V_{OUT_Target} =2.8V, I_{OUT_Target}=100mA, C_{IN_Target}=1.0uF, C_{OUT_Target}=1.0uF	f=100 Hz		75		dB
		f=1kHz		96		dB
		f=10 kHz		98		dB
		f=100 kHz		75		dB
		f=1MHz		56		dB

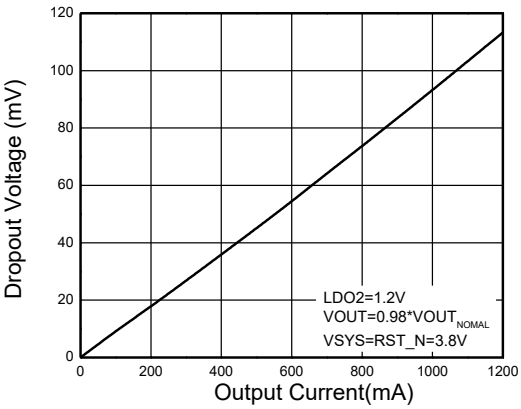
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Power Supply Rejection Ratio	LDO3,4,5,6 & 7(V_{IN_Target} to V_{OUT}) V_{IN_Target}=3.6V+0.2V_{PP}, V_{SYS}=3.8V,V_{OUT_Target}=2.8V, I_{OUT_Target}=100mA, C_{IN_Target}=1.0uF, C_{OUT_Target}=1.0uF	f=100 Hz		80		dB
		f=1kHz		90		dB
		f=10 kHz		80		dB
		f=100 kHz		61		dB
		f=1MHz		44		dB
Thermal Warning	T_{WRN}			115		°C
Thermal Shutdown	T_{SD}			155		°C
Thermal Hysteresis for T_SD and T_WRN	T_{HYS}			25		°C
Active Output Discharge Resistance	LDO1 & 2			120		Ω
	LDO3,4,5,6 & 7			150		Ω
Line Transient	LDO1 & 2	V_{IN} = ($V_{OUT(NOM)}$ + 2.2 V) to ($V_{OUT(NOM)}$ + 1 V) in 10 us, I_{OUT} = 1 mA	-1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 2 V) in 30 us, I_{OUT} = 1 mA			1	mV
	LDO3,4,5,6 & 7	V_{IN} = ($V_{OUT(NOM)}$ + 2.2 V) to ($V_{OUT(NOM)}$ + 1 V) in 10 us, I_{OUT} = 1 mA	-1			
		V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$) + 2 V) in 30 us, I_{OUT} = 1 mA			1	
Load Transient	LDO1 & 2	I_{OUT_Target}=1mA to 500mA in 1uS		-50		mV
		I_{OUT_Target}=500mA to 1mA in 1uS		30		mV
	LDO3,4,5,6 & 7	I_{OUT_Target}=1mA to 300mA in 1uS		-50		mV
		I_{OUT_Target}=300mA to 1mA in 1uS		10		mV
RST_N Logic Inputs						
Input Leakage	I_{LEAK}			0.5	1	μA
Input HIGH Voltage	V_{IH}		1.2			V
Input LOW Voltage	V_{IL}				0.4	V

Parameter	Symbol	Conditions	Min	Typ	Max	Units
IRQ Logic Output						
Input Leakage	I_{LEAK}			0.1	0.2	μA
Output High Voltage	V_{OH}	I_{OUT}=5 mA	1.7	1.8	1.9	V
Input LOW Voltage	V_{OL}	I_{OUT}=5 mA			0.4	V
I2C Logic Level						
Input Leakage	I_{LEAK}			0.1	0.2	μA
Input HIGH Voltage	V_{IH}		1.2			V
Input LOW Voltage	V_{IL}				0.4	V

Typical Characteristics (T_A=25°C, unless otherwise noted)



Dropout Voltage vs. Output Current



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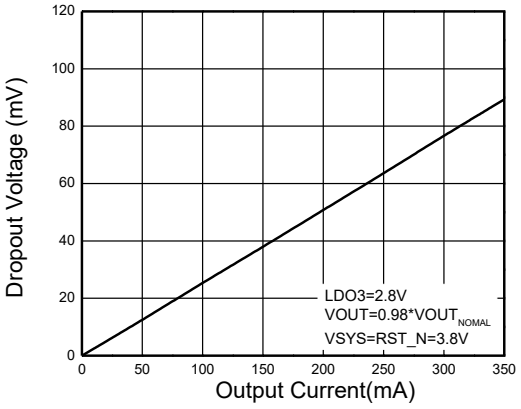

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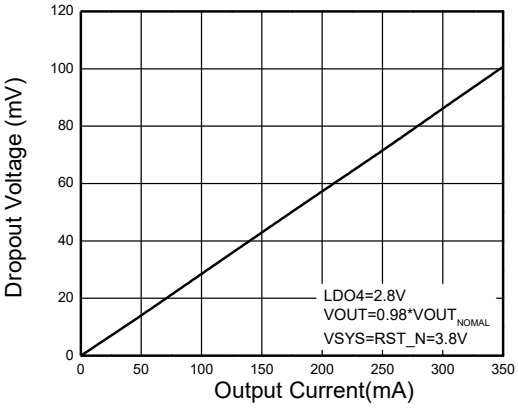

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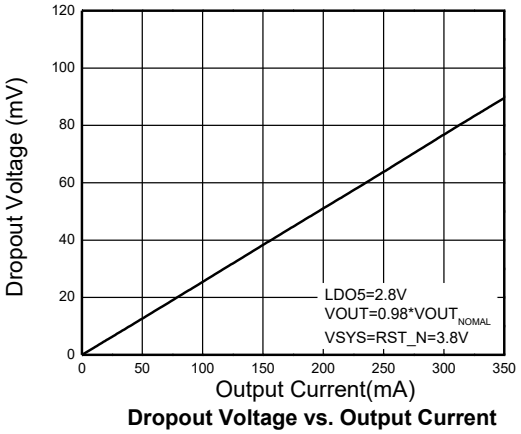

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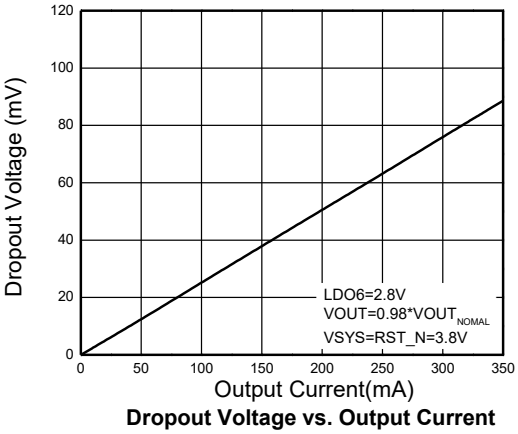

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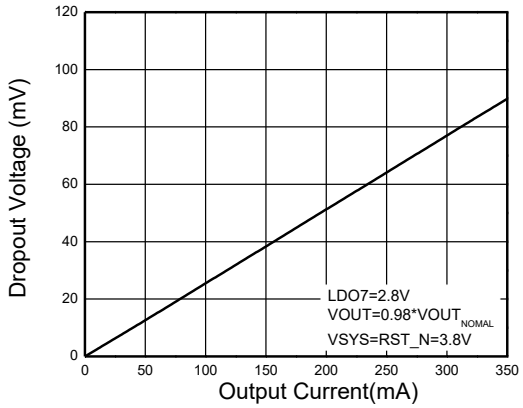

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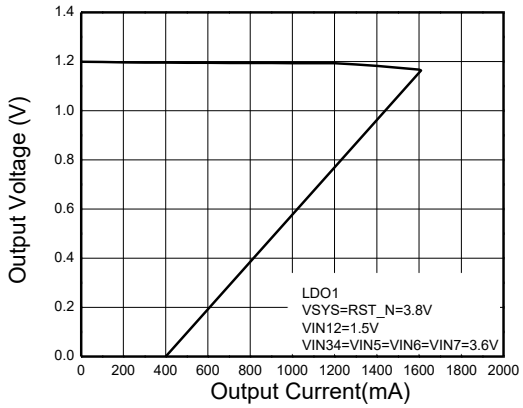
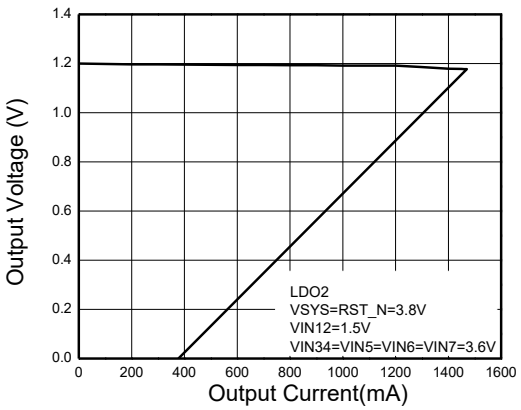


Output Voltage vs. Output Current



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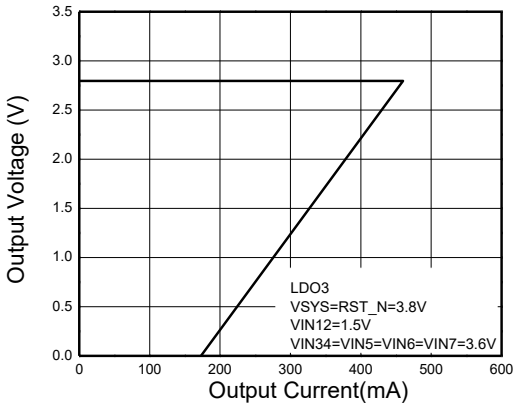

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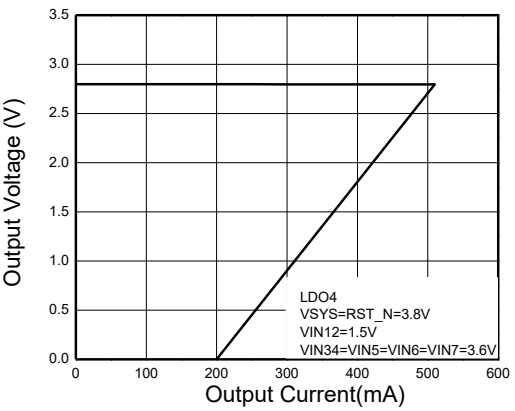

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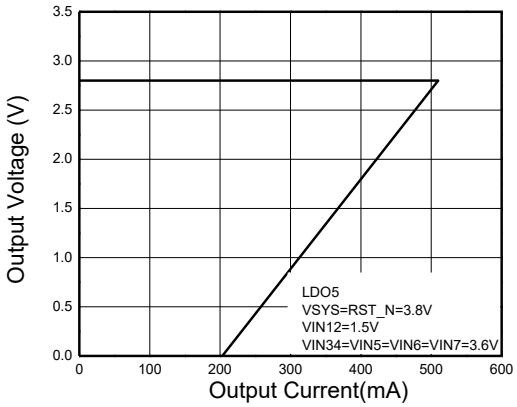
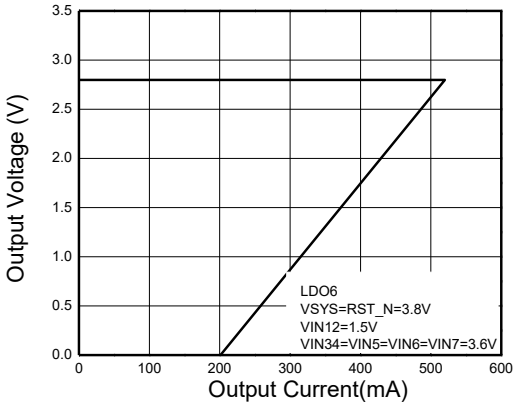


Output Voltage vs. Output Current



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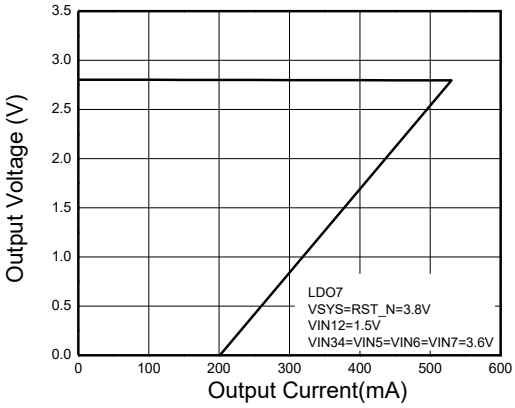
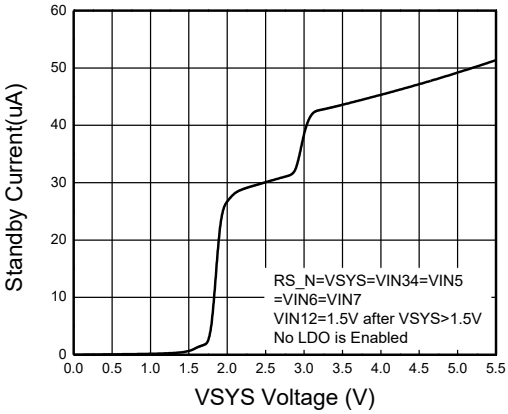
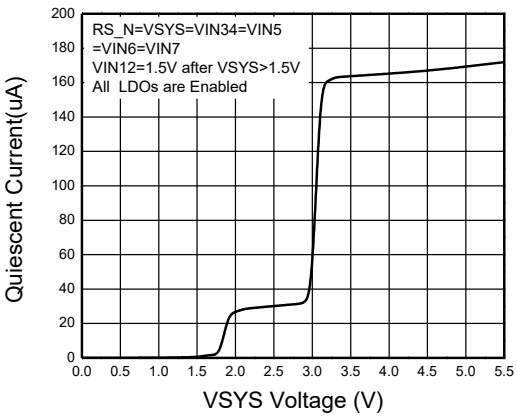


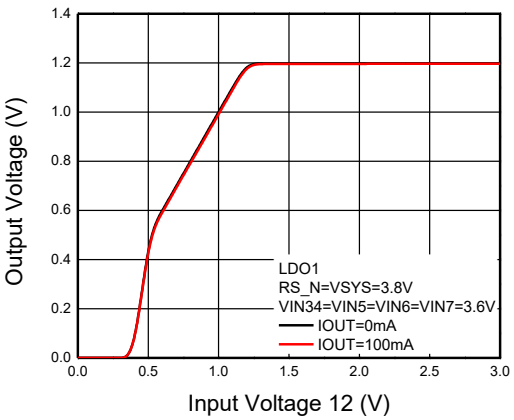
Output Voltage vs. Output Current



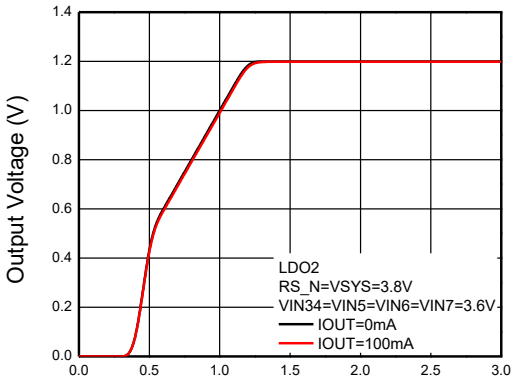
Standby Current vs. VSYS Voltage



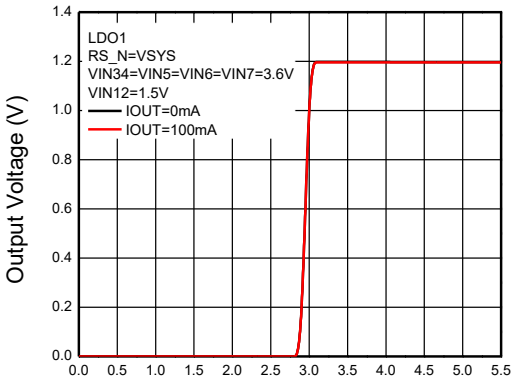
Quiescent Current vs. VSYS Voltage



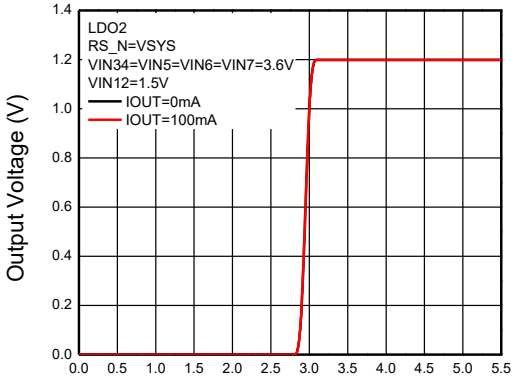
Output Voltage vs. Input Voltage 12



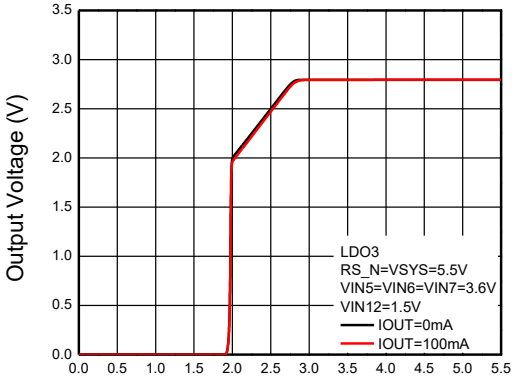
Output Voltage vs. Input Voltage 12



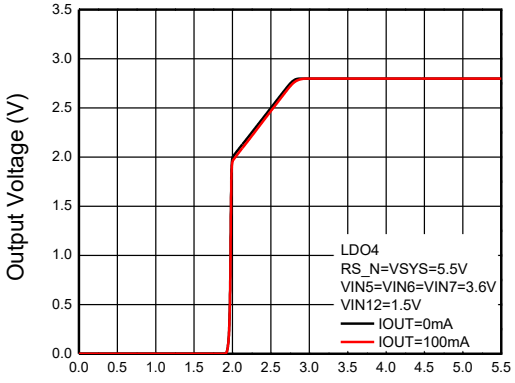
Output Voltage vs. VSYS Voltage



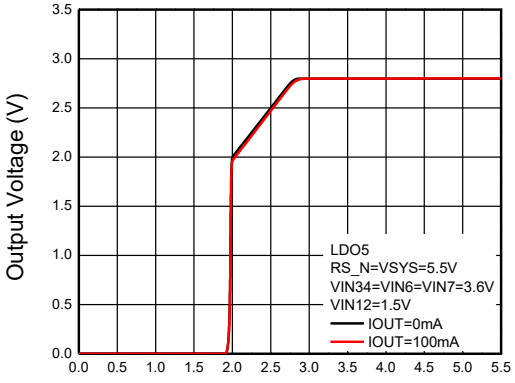
Output Voltage vs. VSYS Voltage



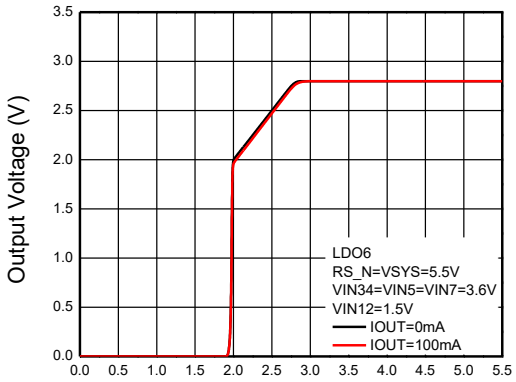
Output Voltage vs. Input Voltage 34



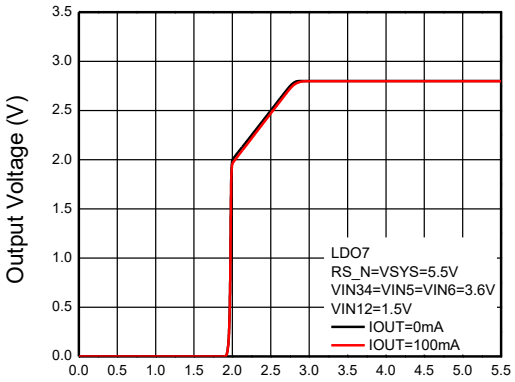
Output Voltage vs. Input Voltage 34



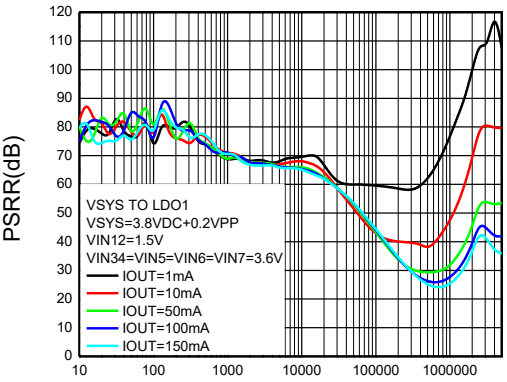
Output Voltage vs. Input Voltage 5



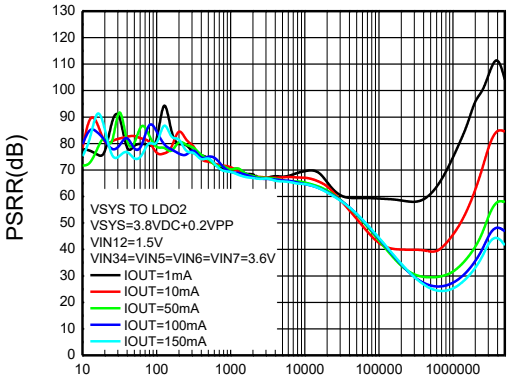
Output Voltage vs. Input Voltage 6



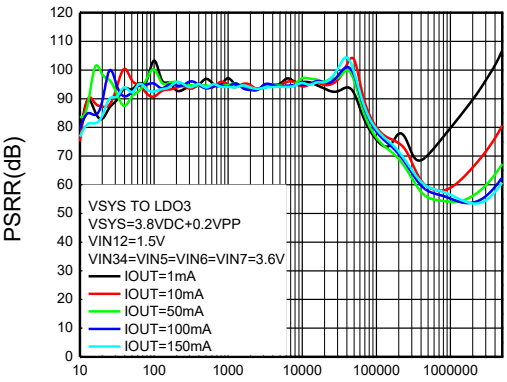
Output Voltage vs. Input Voltage 7



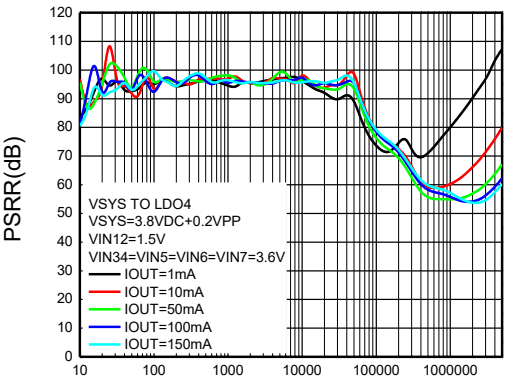
PSRR vs Frequency



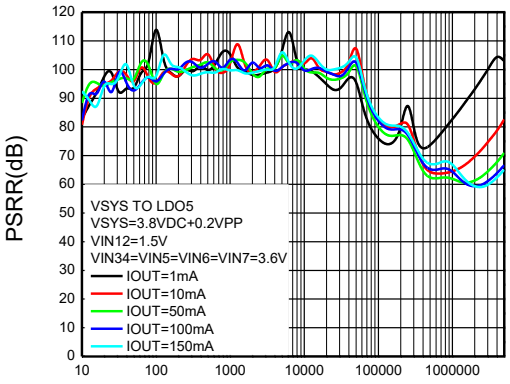
PSRR vs Frequency



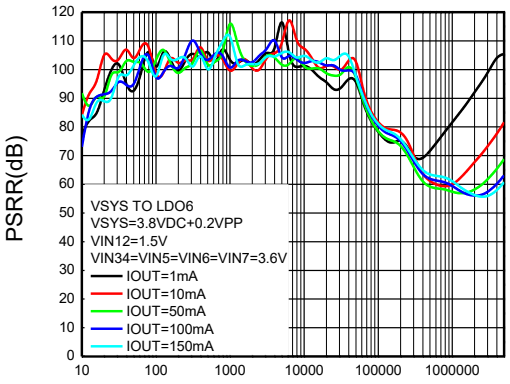
PSRR vs Frequency



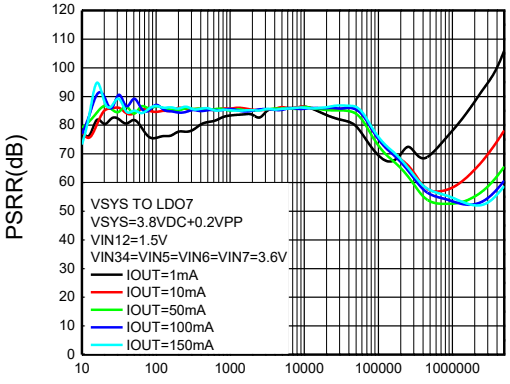
PSRR vs Frequency



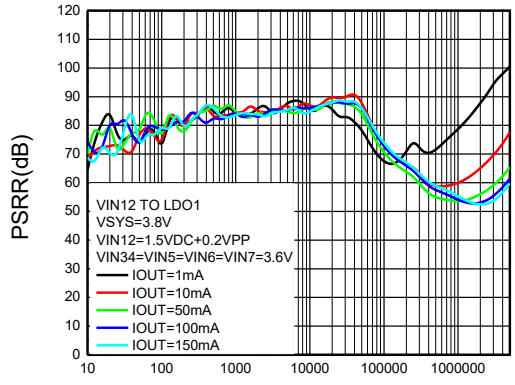
PSRR vs Frequency



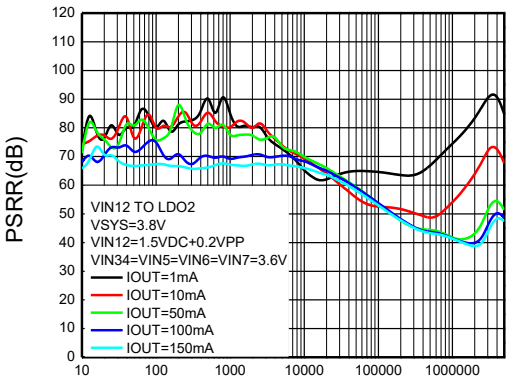
PSRR vs Frequency



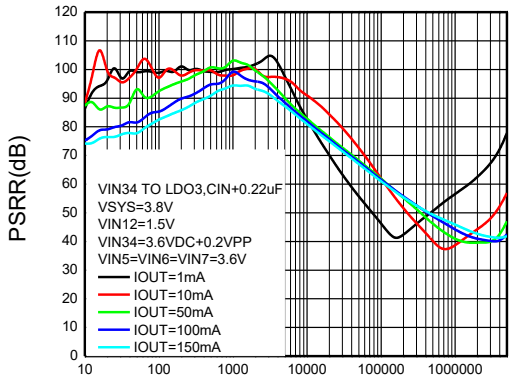
PSRR vs Frequency



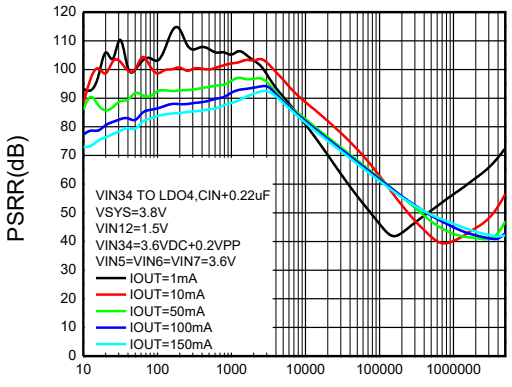
PSRR vs Frequency



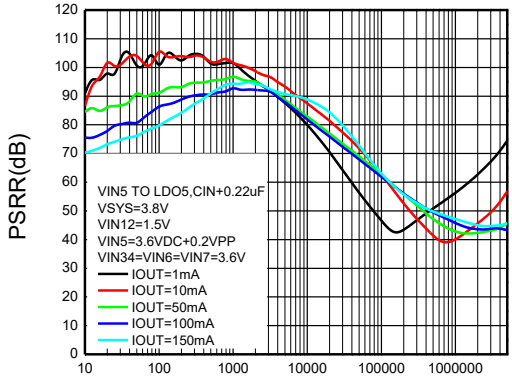
PSRR vs Frequency



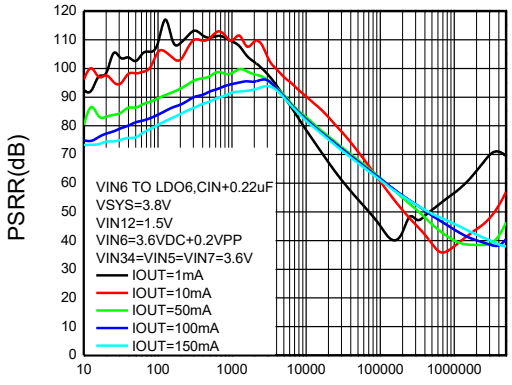
PSRR vs Frequency



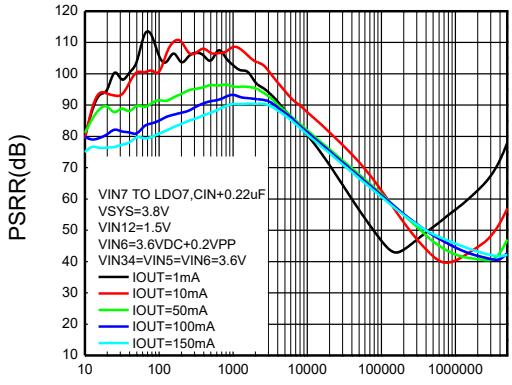
PSRR vs Frequency



PSRR vs Frequency



PSRR vs Frequency

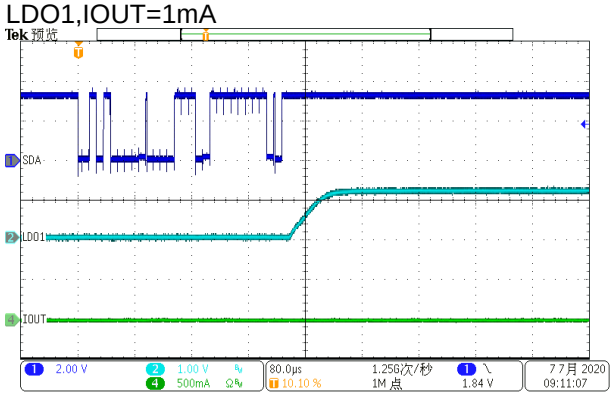


PSRR vs Frequency

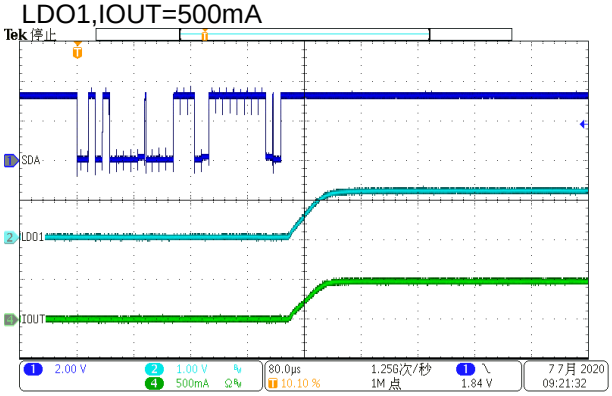
Eble LDOs Through I2C

RST_N=VSYS=3.8V, VIN12=1.5V, VIN34=VIN5=VIN6=VIN7=3.6V

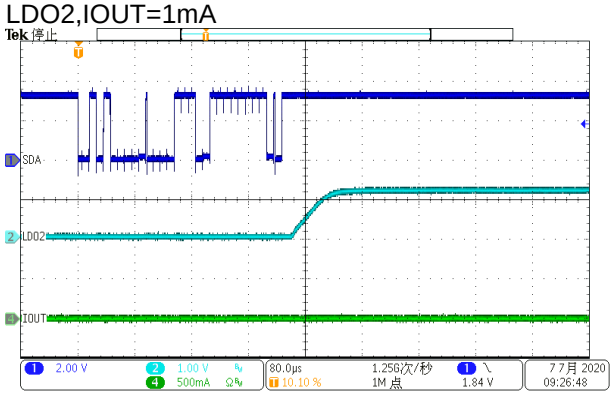
LDO1,IOUT=1mA



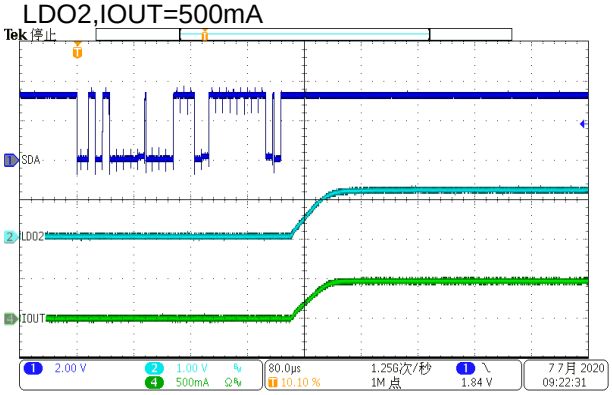
LDO1,IOUT=500mA



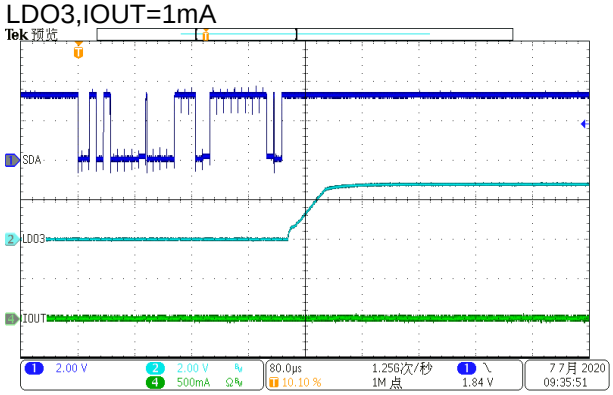
LDO2,IOUT=1mA



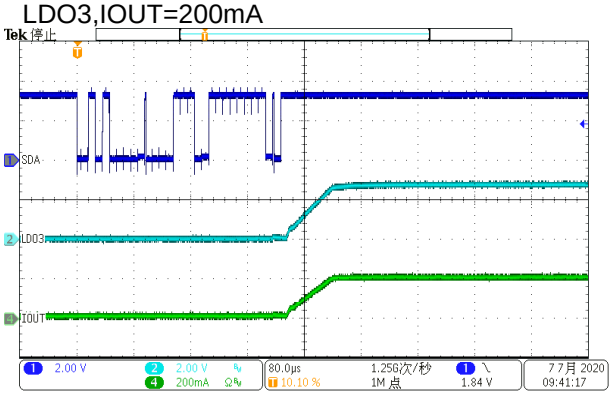
LDO2,IOUT=500mA



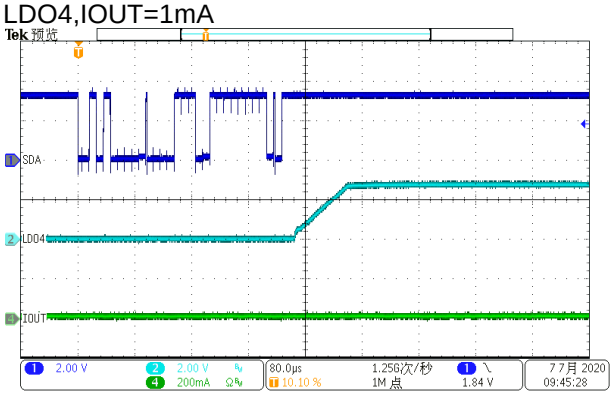
LDO3,IOUT=1mA



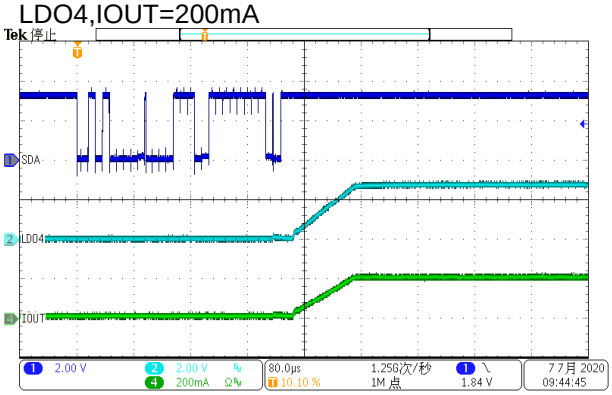
LDO3,IOUT=200mA



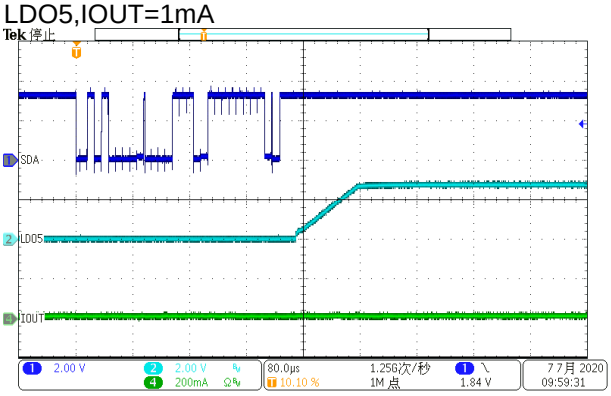
LDO4,IOUT=1mA



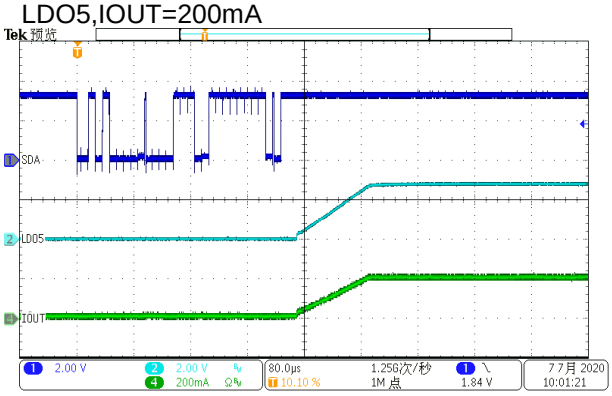
LDO4,IOUT=200mA



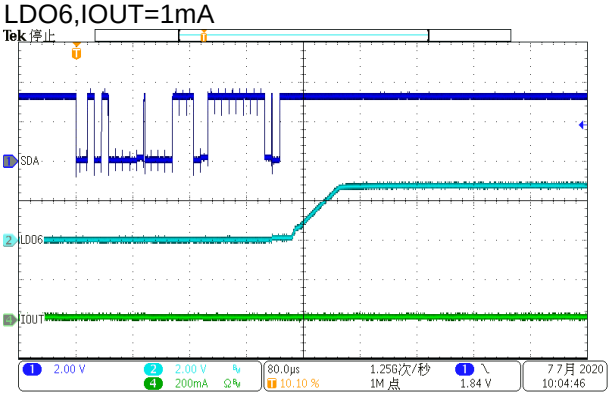
LDO5,IOUT=1mA



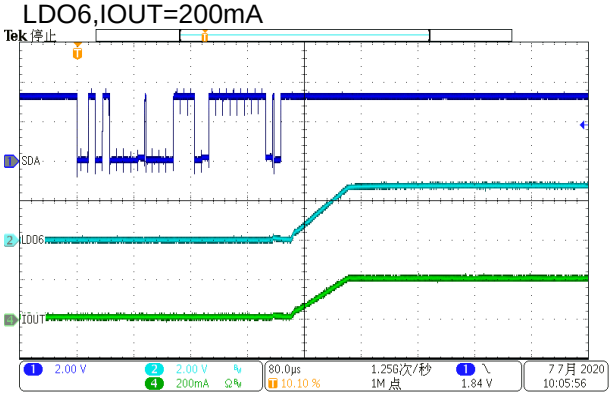
LDO5,IOUT=200mA



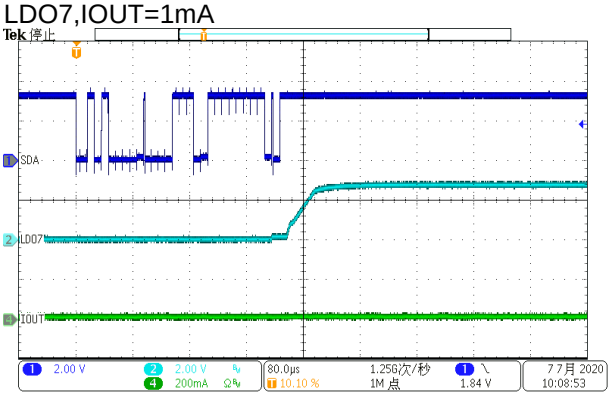
LDO6,IOUT=1mA



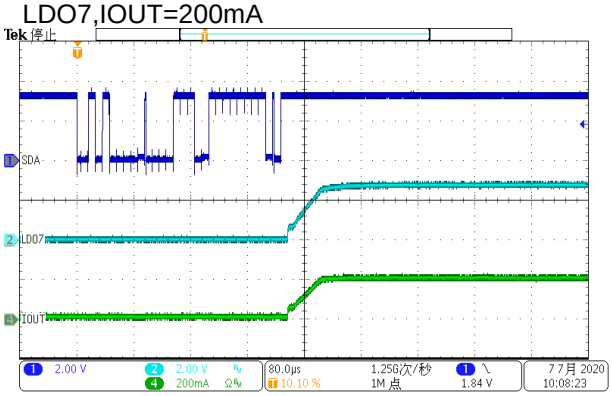
LDO6,IOUT=200mA



LDO7,IOUT=1mA



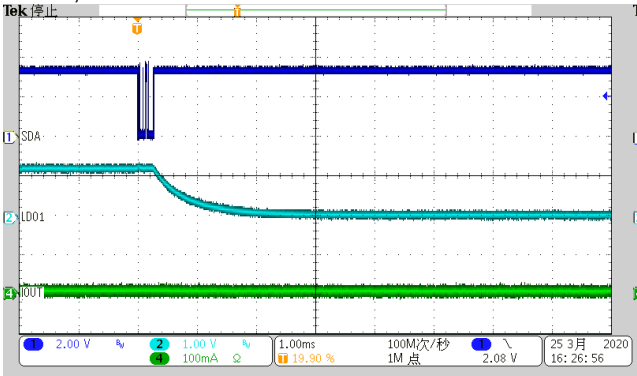
LDO7,IOUT=200mA



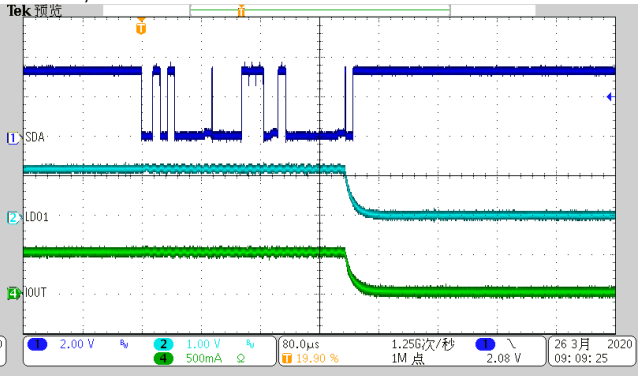
Shut Down LDOs through I2C

RST_N=VSYS=3.8V, VIN12=1.5V, VIN34=VIN5=VIN6=VIN7=3.6V

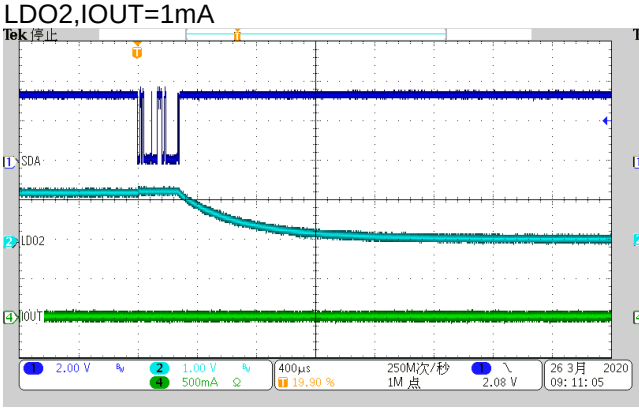
LDO1,IOUT=1mA



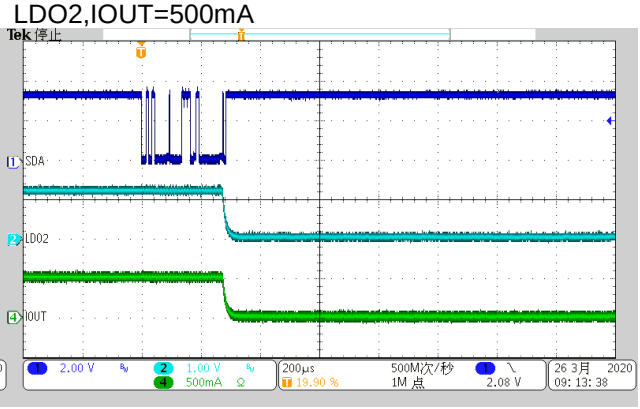
LDO1,IOUT=500mA



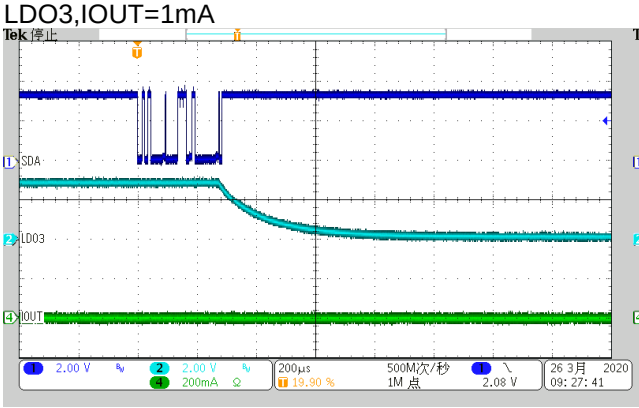
LDO2,IOUT=1mA



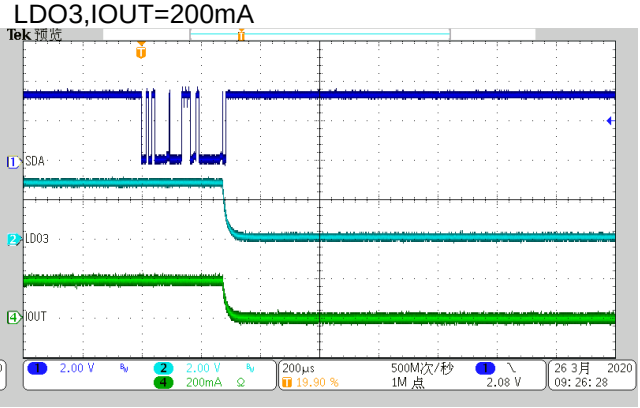
LDO2,IOUT=500mA



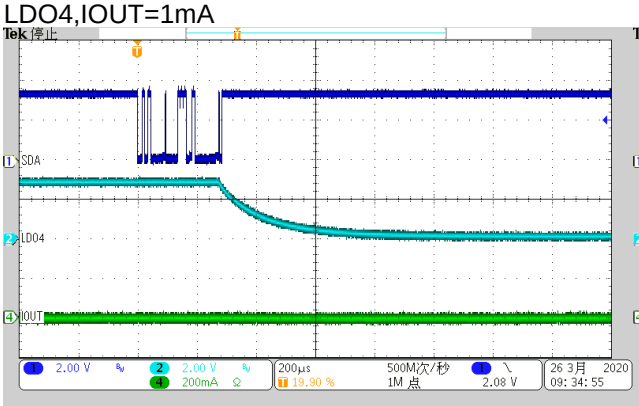
LDO3,IOUT=1mA



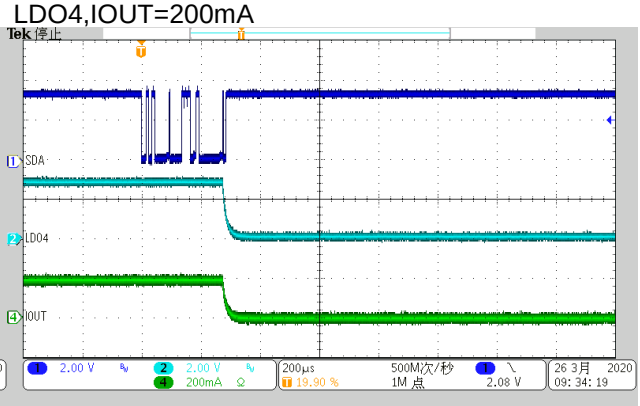
LDO3,IOUT=200mA



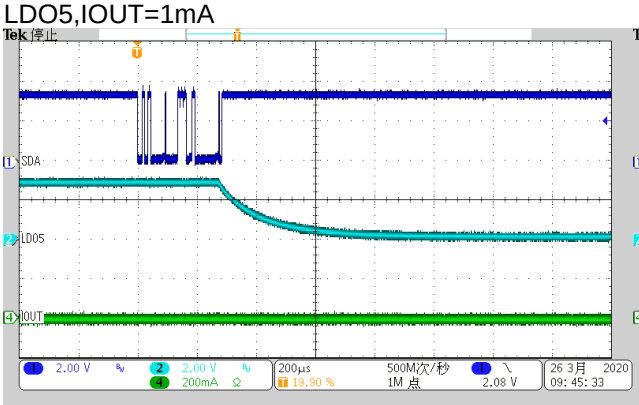
LDO4,IOUT=1mA



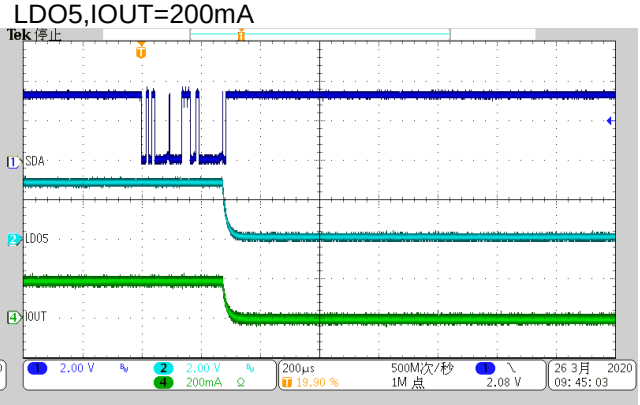
LDO4,IOUT=200mA



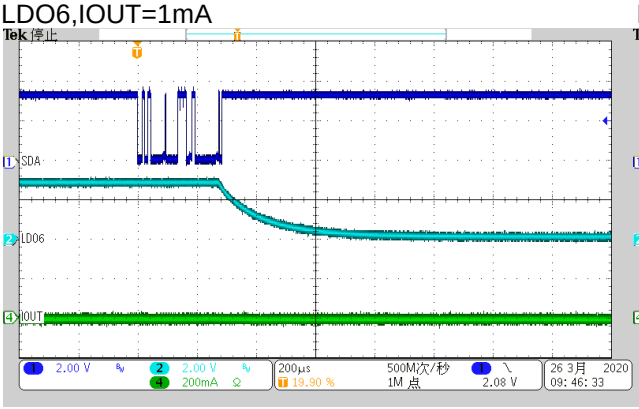
LDO5,IOUT=1mA



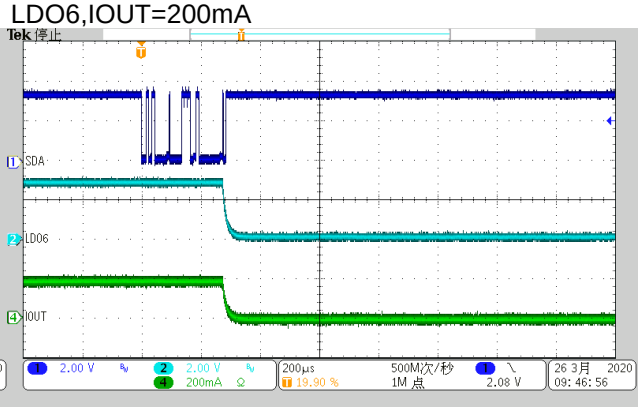
LDO5,IOUT=200mA



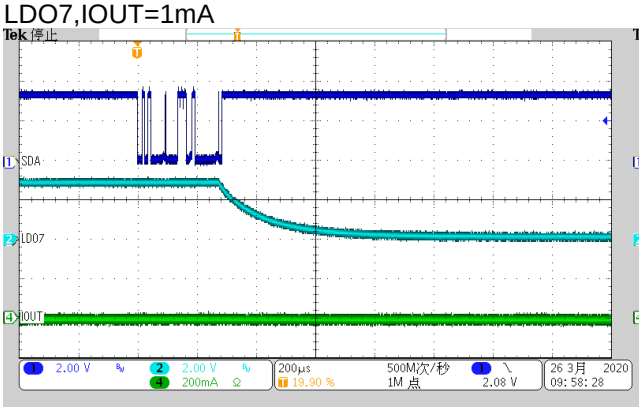
LDO6,IOUT=1mA



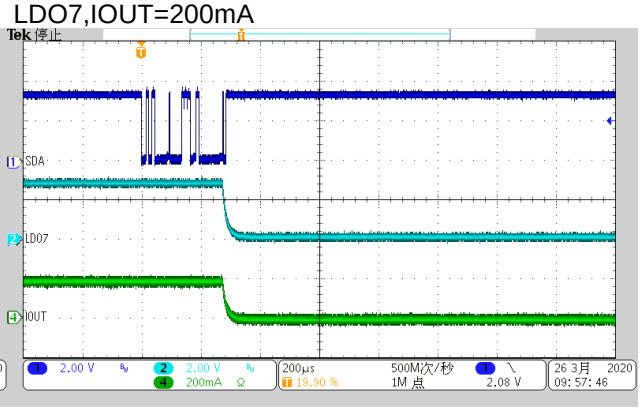
LDO6,IOUT=200mA



LDO7,IOUT=1mA



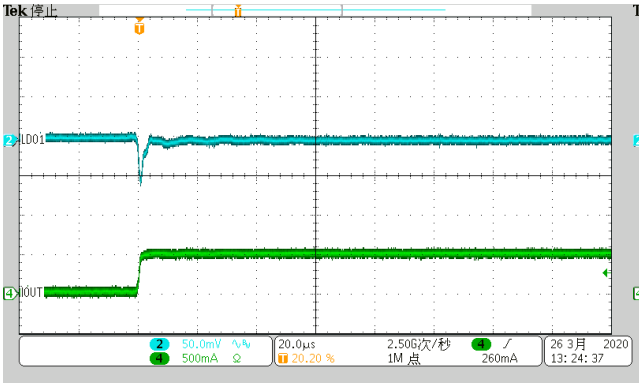
LDO7,IOUT=200mA

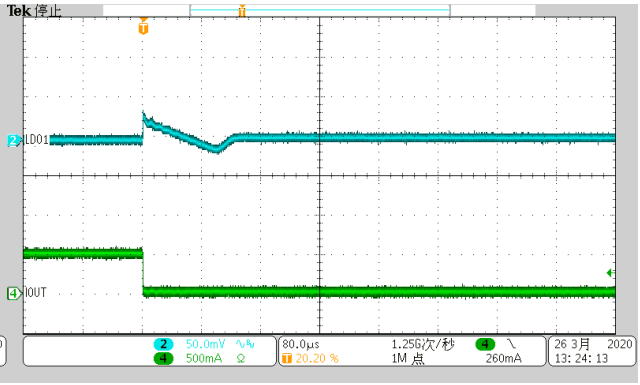


LDO1&2 Load Transient

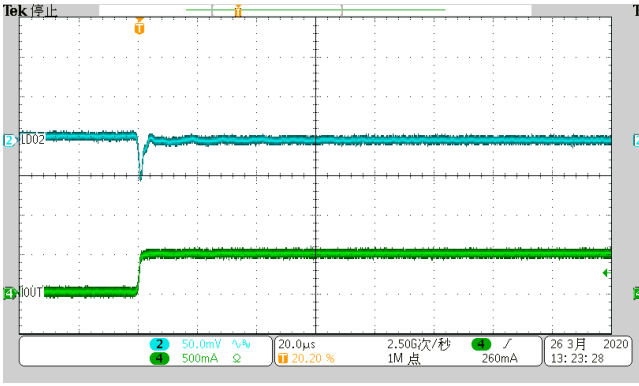
RST_N=VSYS=3.8V, VIN12=1.5V, VIN34=VIN5=VIN6=VIN7=3.6V, IOUT=1mA~500mA in 1us.

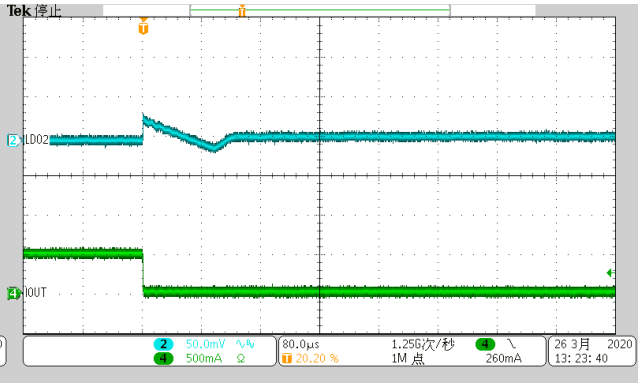
LDO1





LDO2

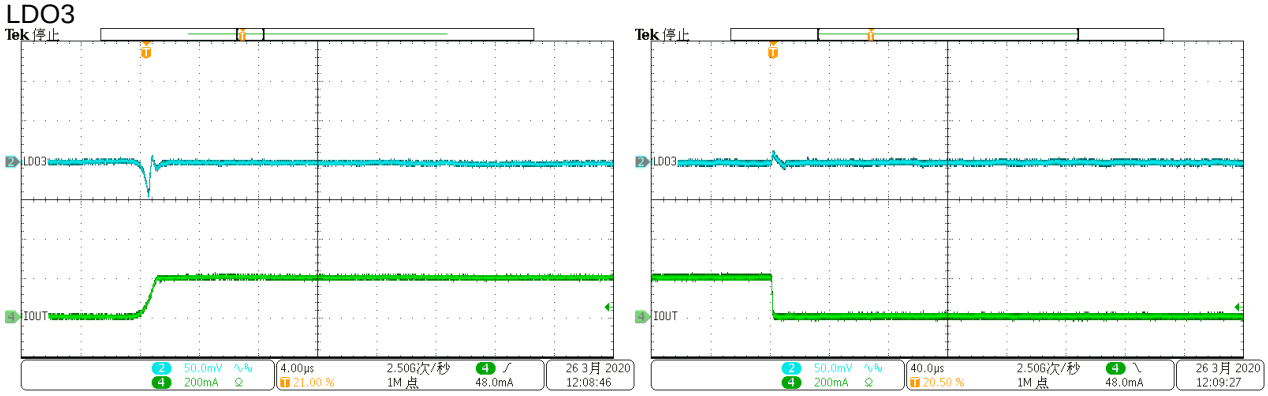




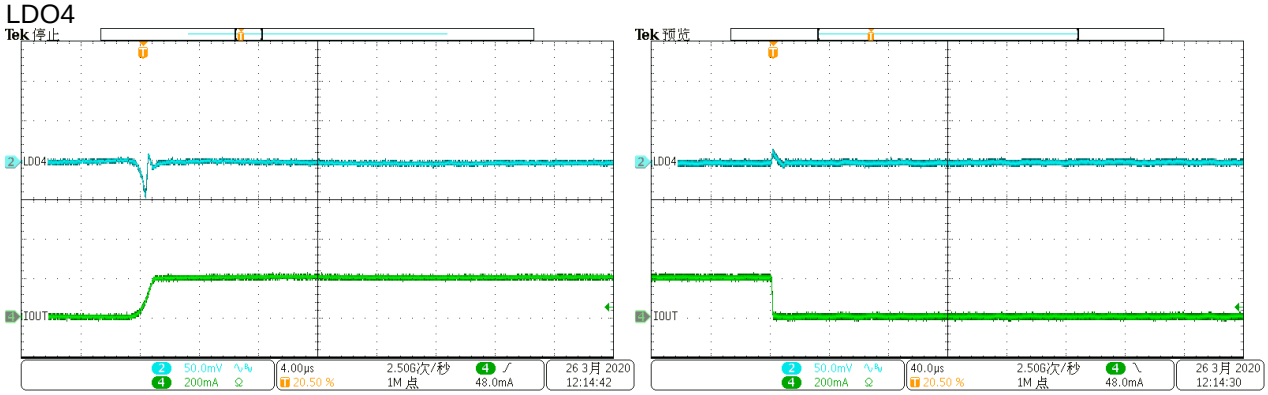
LDO3,4,5,6&7 Load Transient

RST_N=VSYS=3.8V, VIN12=1.5V, VIN34=VIN5=VIN6=VIN7=3.6V, IOUT=1mA~200mA in 1us.

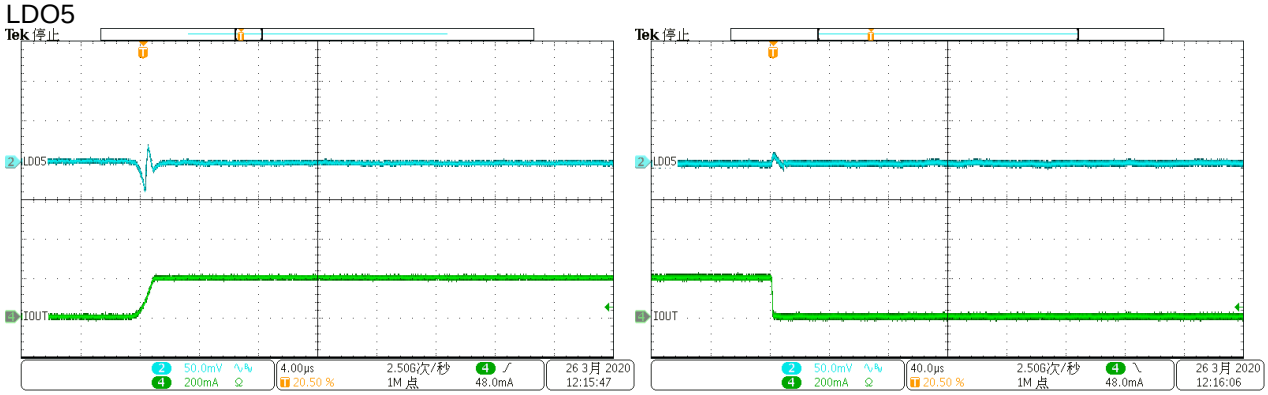
LDO3



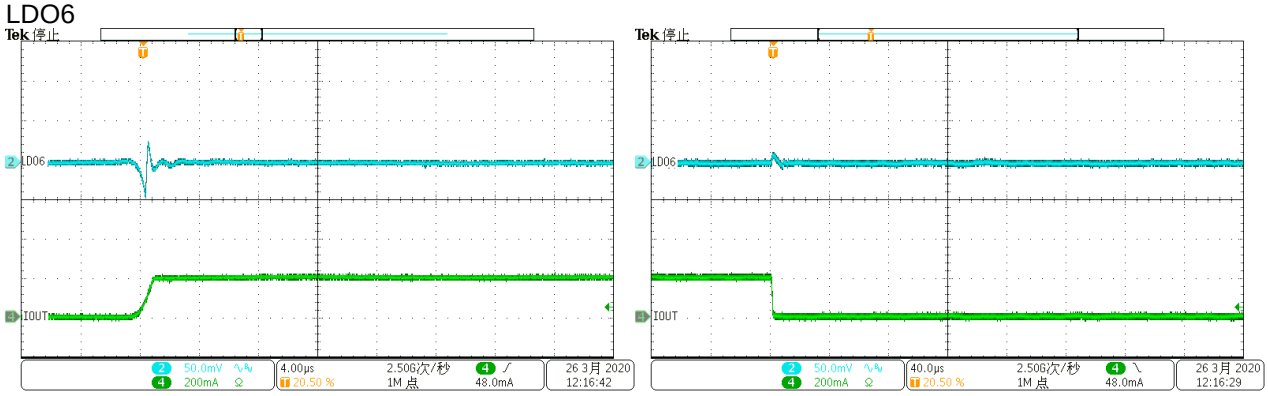
LDO4



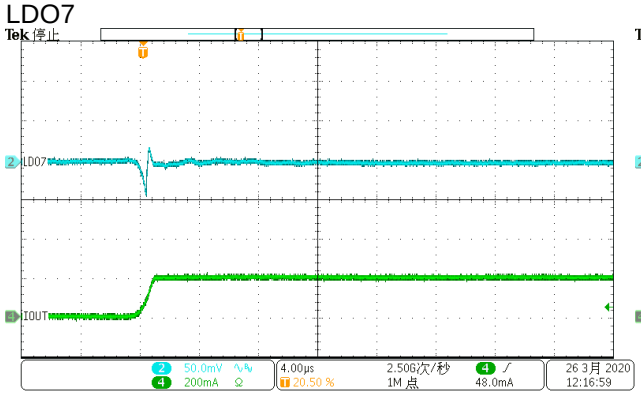
LDO5

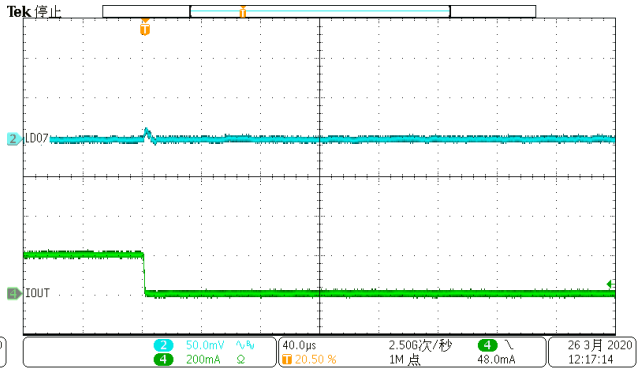


LDO6



LDO7

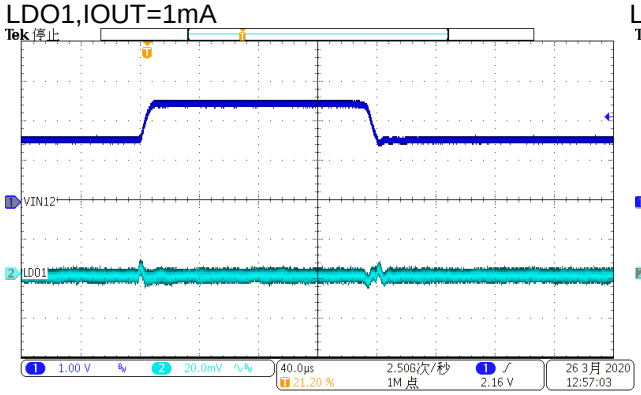




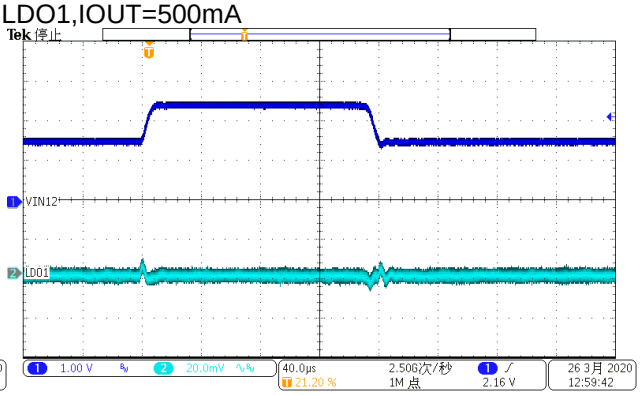
LDO1&2 Line Transient

RST_N=VSYS=3.8V, VIN12=1.5V~2.5V in 10us, VIN34=VIN5=VIN6=VIN7=3.6V

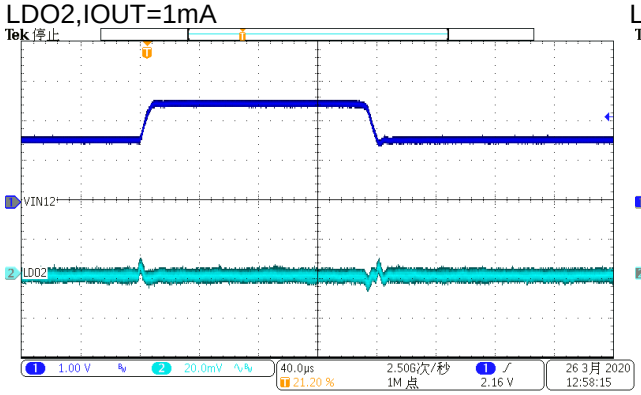
LDO1,IOUT=1mA



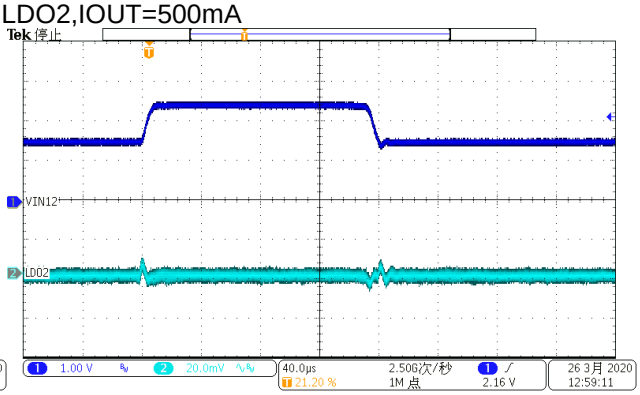
LDO1,IOUT=500mA



LDO2,IOUT=1mA



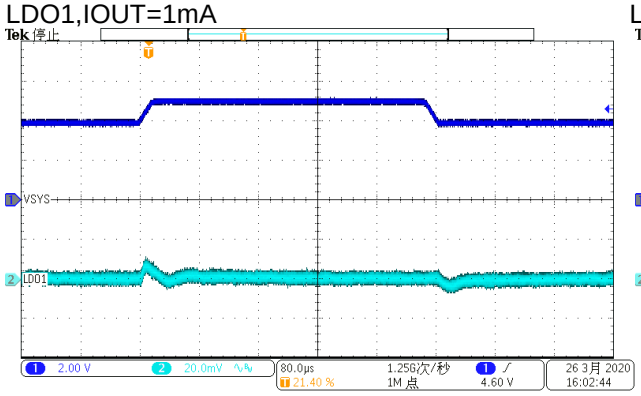
LDO2,IOUT=500mA



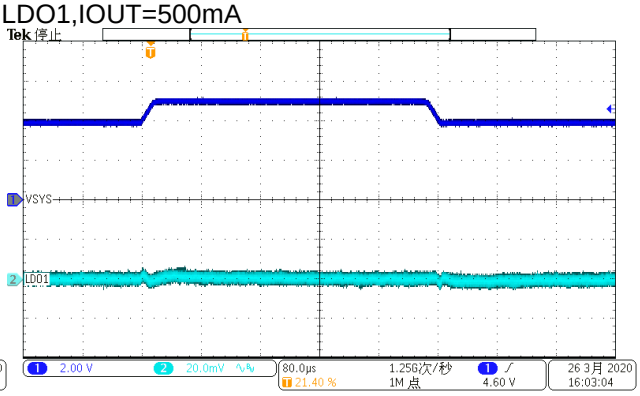
LDO1&2 Line Transient

RST_N=VSYS=3.8V~5V in 10us, VIN12=1.5V, VIN34=VIN5=VIN6=VIN7=3.6V

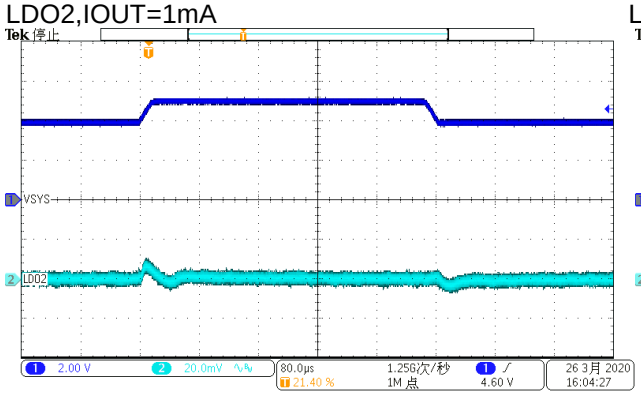
LDO1,IOUT=1mA



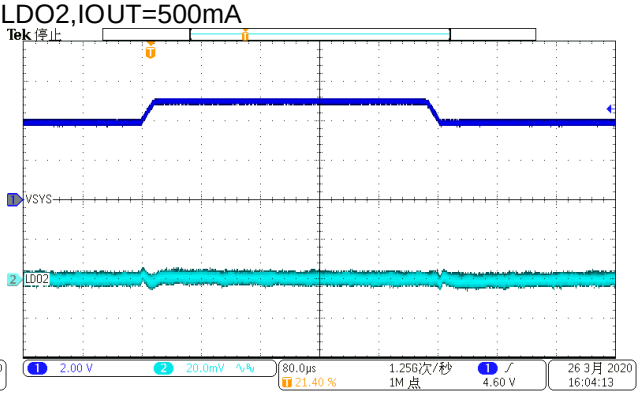
LDO1,IOUT=500mA



LDO2,IOUT=1mA



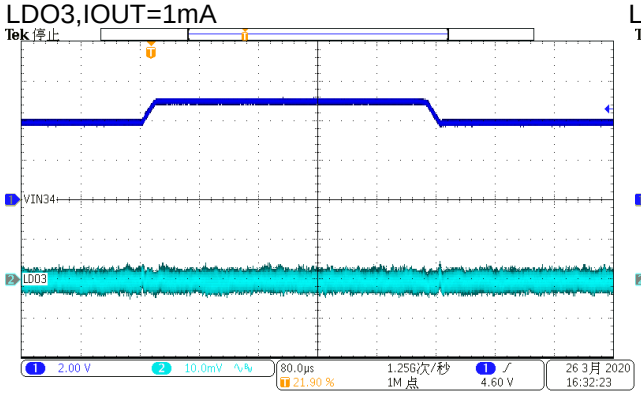
LDO2,IOUT=500mA



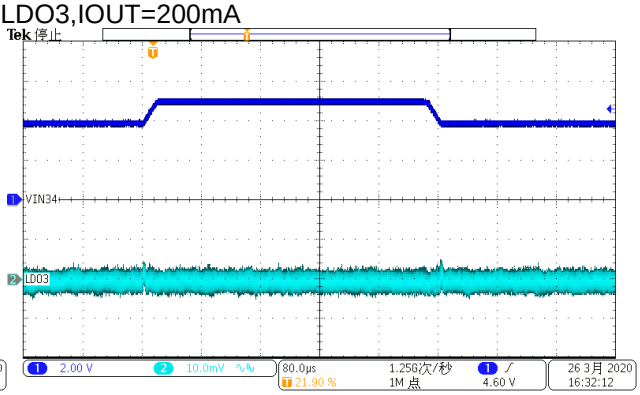
LDO3,4,5,6&7 Line Transient

RST_N=VSYS=VIN34=VIN5=VIN6=VIN7=3.8V~5V in 10us, VIN12=1.5V

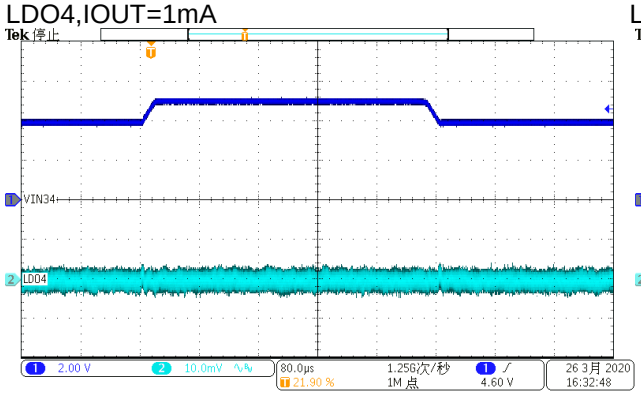
LDO3,IOUT=1mA



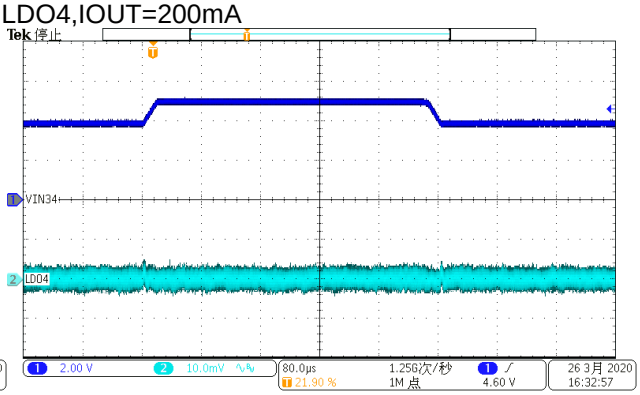
LDO3,IOUT=200mA



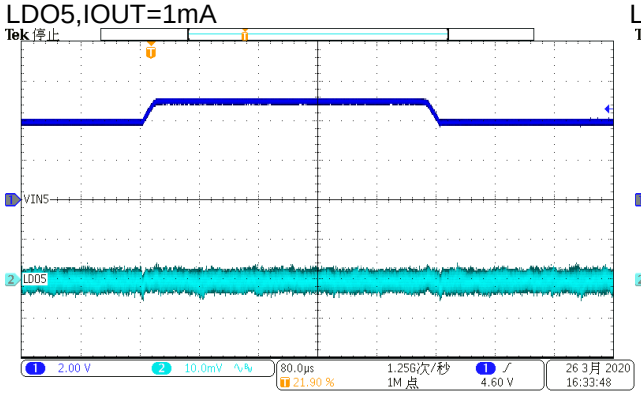
LDO4,IOUT=1mA



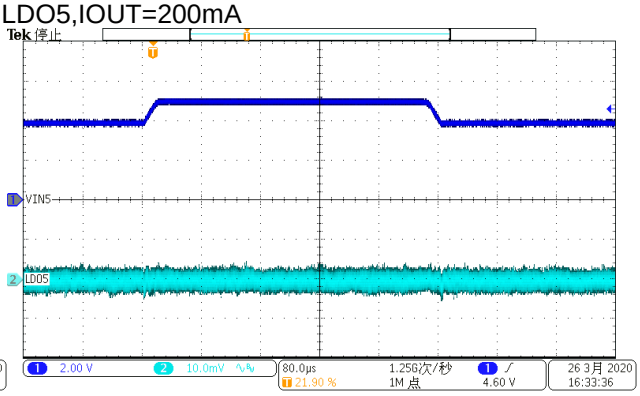
LDO4,IOUT=200mA



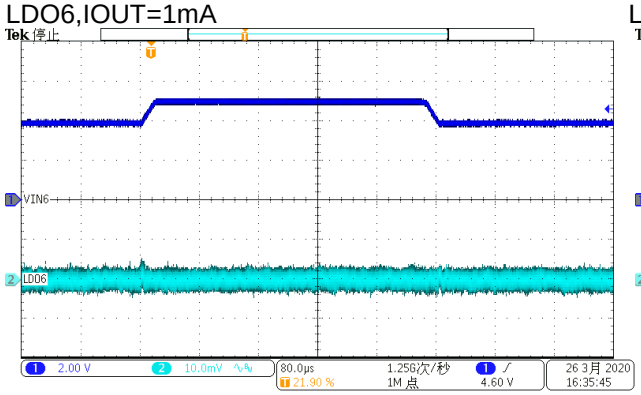
LDO5,IOUT=1mA



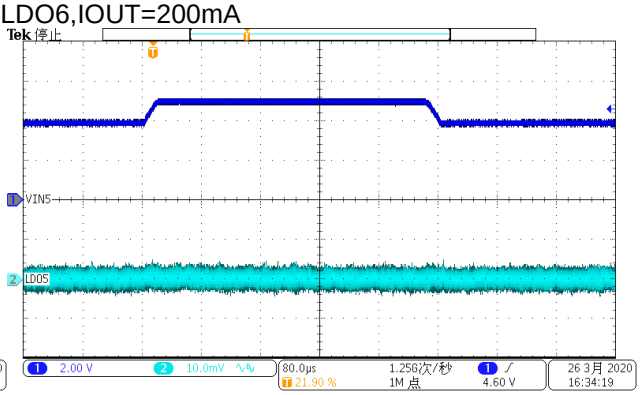
LDO5,IOUT=200mA



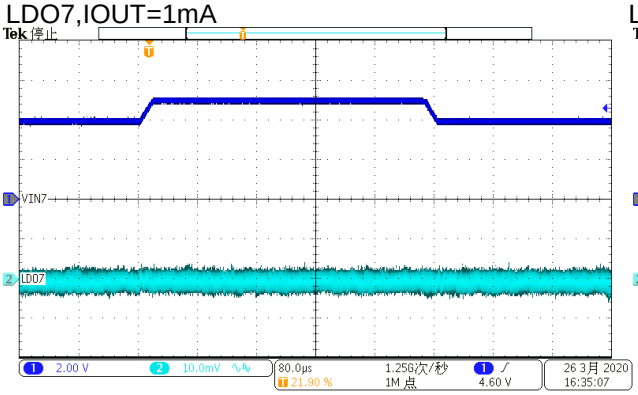
LDO6,IOUT=1mA



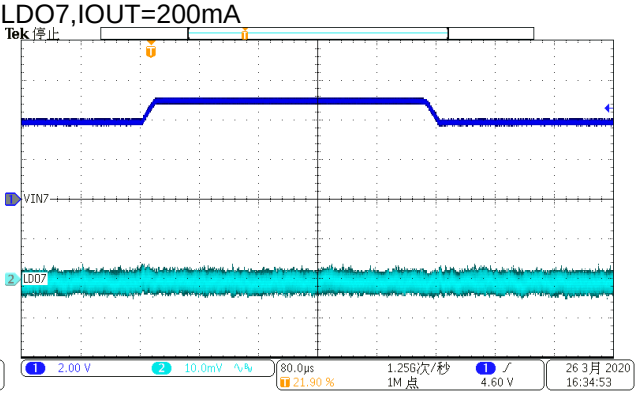
LDO6,IOUT=200mA



LDO7,IOUT=1mA



LDO7,IOUT=200mA



Function Description

WL2868C is a PMU with 7 LDO regulators, 2 of which are high current low dropout LDOs to power the digital circuits and 5 of which are high PSRR low noise LDOs to power the analog circuit. Each LDO output voltage and power up sequence can be programed though the I2C interface

VSYS UVLO and VIN7

The internal control logic and Bias are powered by VSYS or VIN7 whichever is higher, there is the VSYS UVLO circuit monitoring the VSYS voltage, when VSYS voltage is lower than the UVLO threshold. The LDOs will be shut down mode. UVLO hysteresis prevents minor glitches from being detected as UVLO events. The I2C communication will keep functional if either VIN7 or VSYS voltage is higher than the POR voltage which is 2V. The UVLO event can generate the interrupt if configured to do so when I2C is in active state. VSYS UVLO threshold default is 3V but can be changed by a dedicated register (0x24H) after the device is on (when I2C communication is active when POR is high).

Input UVLO

All the LDOs has the individual UVLO circuits, when the input voltage is lower than the UVLO threshold, the LDO will shut down.

Enable and Reset

WL2868C has two methods of enabling or resetting:

Hardware enable/reset:

RST_N is the dedicated enable/reset pin, the device is enabled by pulling RST_N HIGH, and the registers can be configured through the I2C interface, the device will be in standby mode comsuming about 40uA current. Pulling RST_N LOW disables WL2868C and all register configurations are lost. All modules of WL2868C are reset by RST_N and I2C communication will not work until RST_N is pulled HIGH, the device is in low current consumption sleep mode consuming only 2 uA current.

Software enable/reset:

Bit7 of register 0x0E is dedicated to enable/disable the PMU if RST_N is pulled high. Writing 1 to this register bit enables WL2868C, the Hardware default of this bit is 1 which enables WL2868C during first boot. Writing a 0 to bit7 of register 0x0E disables WL2868C,but will not reset the register configurations as long as RST_N remains high. In the software reset mode, I2C hardware is still enabled. When the device is in the software reset mode, the UVLO_LATCHED_STS bit will be set. The UVLO_LATCHED_CLR bit need to be reset before the PMU enabled again, otherwise the UVLO_LATCHED_STS will trigger the interrupt wrongly.

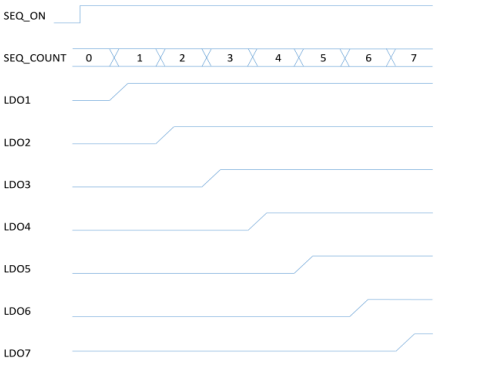
LDO On/off Control and sequencing

A. Individual LDO on/off control
Power-up and shut down of each regulator can be controlled by the register 0x0E. LDOx_EN is an internal signal to enable the individual LDOs. If LDOx_SEQ [3:0] set to '0000', the LDOx can be controlled directly by the bit LDOx_EN specified in register 0x0E.

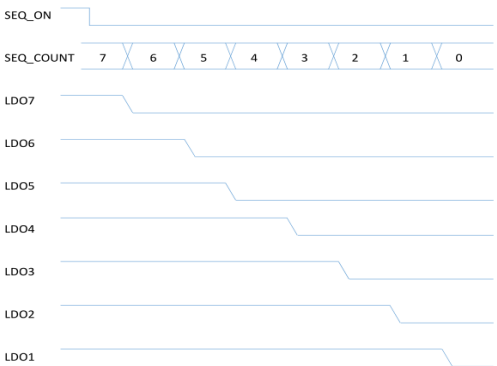
B. Automatic power up/down sequence control.
WL2868C has seven SLOTs to which each regulator can be assigned.

SLOT1	SLOT2	SLOT3	SLOT4	SLOT5	SLOT6	SLOT7

They are started by SEQ_ON signal. When SEQ_ON is high, internal counter SEQ_COUNT [2:0] starts increment from 0 ("000") to 7 ("111"). When SEQ_ON is low, SEQ_COUNT [2:0] decrements from 7 ("111") to 0 ("000"). Regulators assigned to one of the SLOTs starts power-up or power-down when SEQ_COUNT [2:0] matches the SLOT number. Internal logic signal SEQ_ON is asserted by I2C, write '00' to SEQ_CTRL [1:0] will set SEQ_ON to'0', while write '01' to SEQ_CTRL [1:0] will set SEQ_ON to '1'.



Example of Power-up in the case of LDO1 — LDO7



Example of Power-down in the case of LDO7 — LDO1

Output Speed Discharge

There are the pull down resistors at each LDO output which will discharge the output capacitors quickly during power off, the discharge is enabled by default and can be disabled by set the individual bits in register 0x02.

Fault Protection and Interrupt

The PMU has the VSYS UVLO, over current and over temperature protection, when the fault condition happens, the interrupt signal will be initiated by setting high or output a pulse on IRQ pin, and the interrupts can be masked individually or globally by writing the register 0x21, the interrupt status is latched in 0x22 and only one fault event is active if there are multiple fault conditions happen, to get the multiple fault condition, the interrupt latch register must be cleared so as other fault condition can be captured into the register 0x22.

I2C Interface

WL2868C utilizes I2C interface to write / read internal registers. It supports 100Kbps standard mode 400Kbps fast mode.

I2C Serial Data Bus

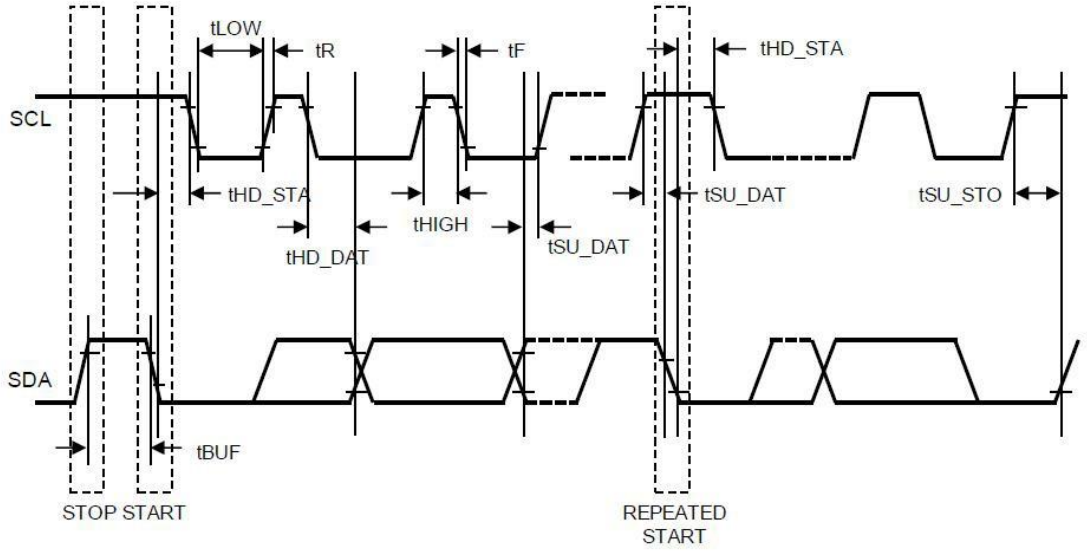


Figure 2. I²C Mode Timing Diagram

The WL2868C supports the I2C bus protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The device that controls the bus is called a master, whereas the devices controlled by the master are known as slaves. A master device must generate the serial clock (SCL), control bus access and generate START and STOP conditions to control the bus. The WL2868C operates as a slave on the I2C bus. Within the bus specifications a standard mode (100 kHz maximum clock rate) and a fast mode (400 kHz maximum clock rate) are defined. The WL2868C works in both modes. Connections to the bus are made through the open-drain I/O lines SDA and SCL. The following bus protocol has been defined (Figure2 and Figure 3). Data transfer may be initiated only when the bus is not busy. During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is high are interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy

Both data and clock lines remain HIGH.

Start Data Transfer

A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer

A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid

The state of the data line represents valid data when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. The data on the line must be changed during the LOW period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions are not limited, and are determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth bit.

Acknowledge

Each receiving device, when addressed, is obliged to generate Acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge-related clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

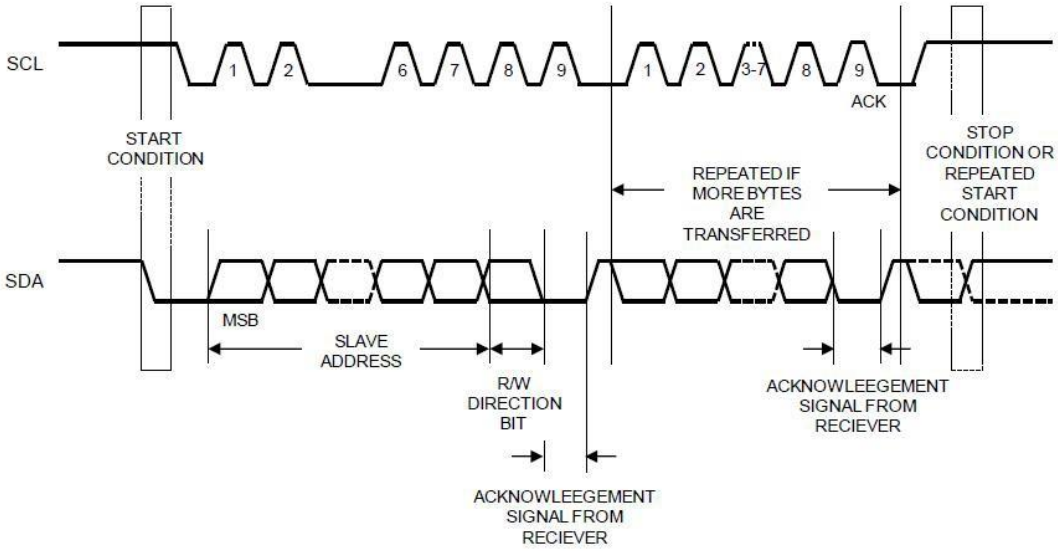


Figure 3. Data Transfer on I²C Serial Bus

Depending upon the state of the R/W bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after each received byte. Data is transferred with the most significant bit (MSB) first.

2. **Data transfer from a slave transmitter to a master receiver.** The master transmits the first byte (the slave address). The slave then returns an acknowledge bit, followed by the slave transmitting a number of data bytes. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a “not acknowledge” is returned. The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus is not released. Data is transferred with the most significant bit (MSB) first.

The WL2868C can operate in the following two modes:

1. **Slave Receiver Mode (Write Mode):** Serial data and clock are received through SDA and SCL. After each byte is received an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit (see Figure 4 for Interface). The slave address byte is the first byte received after the master generates the START condition. The slave address byte contains the 7-WL2868C address followed by the direction bit (R/W), which, for a write, is 0. After receiving and decoding the slave address byte the device outputs an Acknowledge on the SDA line. After the WL2868C acknowledges the slave address + write bit, the master transmits a register address to the WL2868C. This sets the register pointer on the WL2868C. The master may then transmit zero or more bytes of data, with the WL2868C acknowledging each byte received. The address pointer will increment after each data byte is transferred. The master generates a STOP condition to terminate the data write.

2. Slave Transmitter Mode (Read Mode): The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit indicates that the transfer direction is reversed. Serial data is transmitted on SDA by the WL2868C while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer. The slave address byte is the first byte received after the master generates a START condition. The slave address byte contains the 7-bit WL2868C address followed by the direction bit (R/W), which, for a read, is 1. After receiving and decoding the slave address byte the device outputs acknowledge on the SDA line. The WL2868C then begins to transmit data starting with the register address pointed to by the register pointer. If the register pointer is not written to before the initiation of a read mode the first address that is read is the last one stored in the register pointer. The WL2868C must receive a “not acknowledge” to end a read.

The 7-bit slave device address is 0101 111 binary

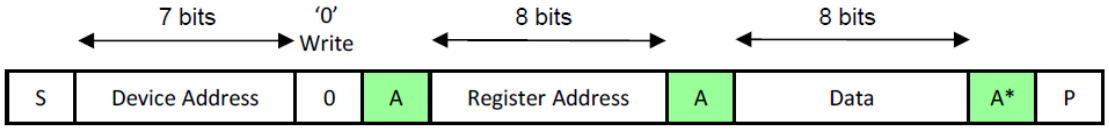


Figure 4. I²C Write – Slave Receiver Mode

device address is 0101 1110

From master to slave

From slave to master **(8 bit device write address)**

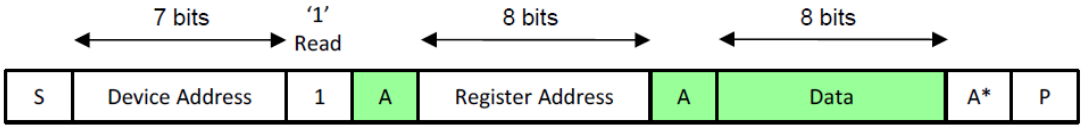


Figure 5. I²C Read – Slave Transmitter Mode

device address is 0101 1111

From master to slave

From slave to master **(8 bit device read address)**

Where

S = START condition

P = STOP condition

Device Address = 0101 111 (7 bits, MSB first)

Register Address = Reg0 – Reg15 address (8 bits)

Data = data to read or write (8 bits)

1 = Read command bit

0 = Write command bit

A = acknowledge (SDA low)

A* = not acknowledge (SDA high)

I2C and Interrupt Manager

The interrupt manager receives internal reports on numerous functions and generate interrupt signal through the IRQ pin. Each interrupt event has the following associated register bits:

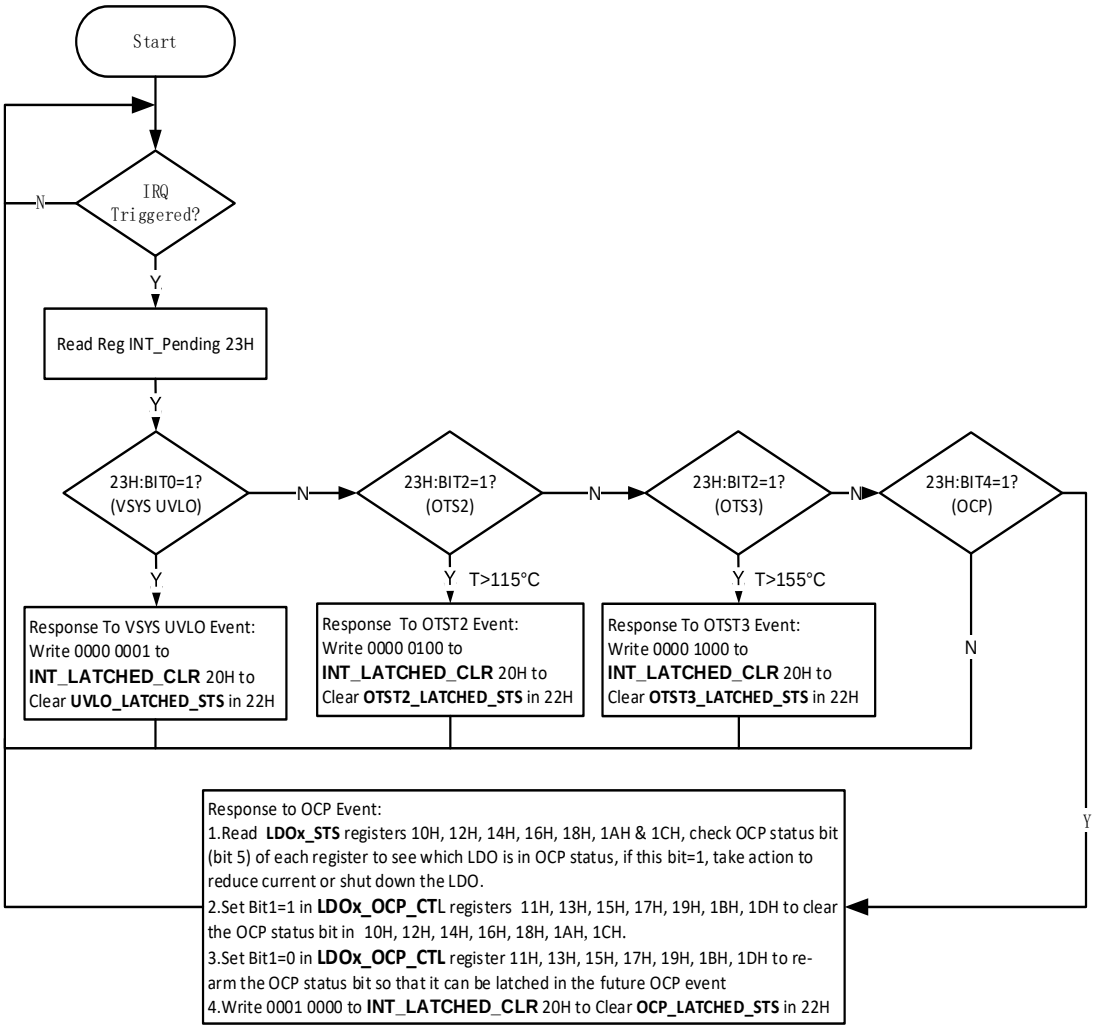
Interrupt mask (read/write): allows the application IC to ignore an event; latched status is hidden and interrupt is not asserted.

Interrupt real-time status (read-only): follows the real-time interrupt status (active or inactive) for standard configuration interrupts.

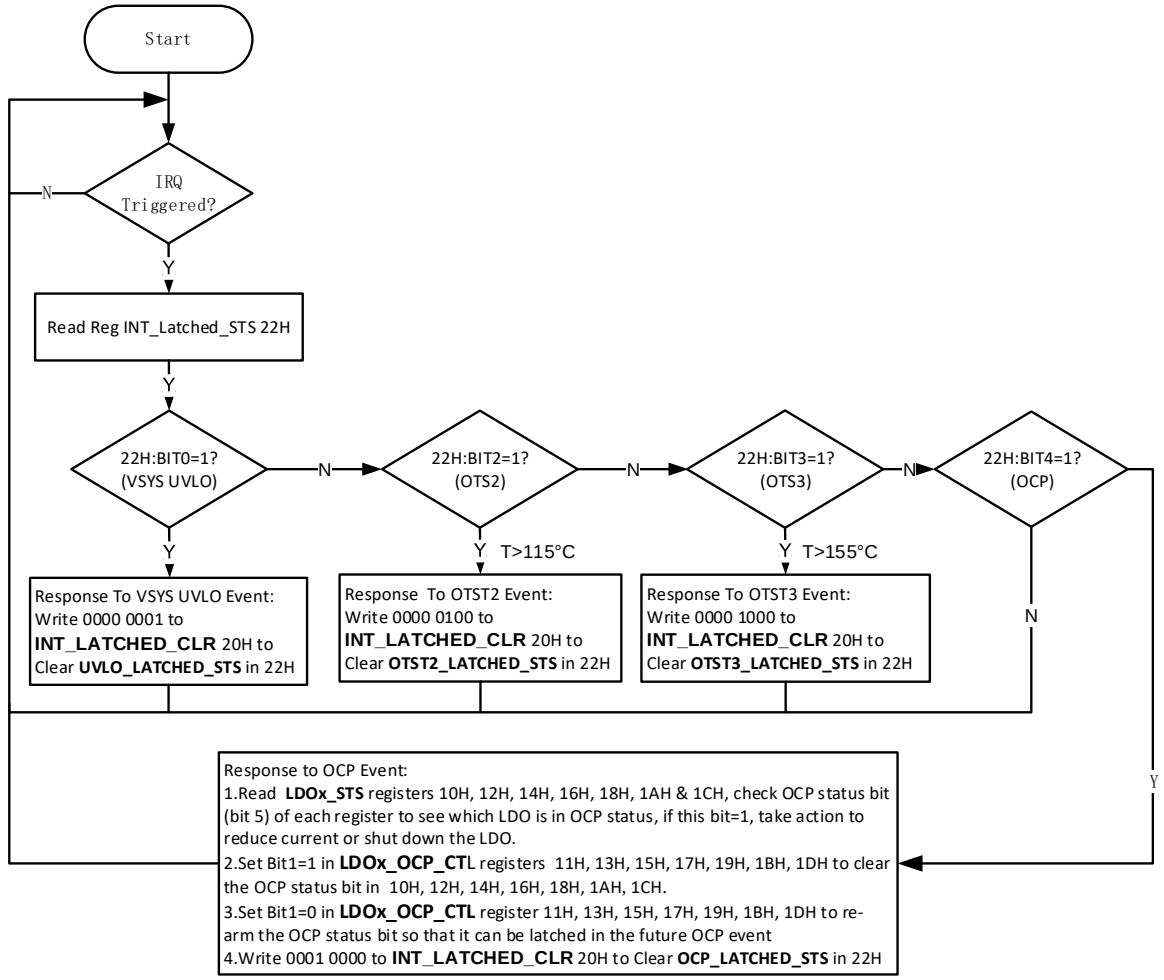
Interrupt latched status (read-only): set when an event is active and an interrupt mask bit is cleared; stays set until a clear bit is set.

Unmasked interrupts notify the application that at least one interrupt has occurred.

The interrupt response flow is showed in the following diagram。There are 2 ways to respond the interrupt，the difference is that with the flow 1 we can know exactly which fault event triggers the current interrupt if multiple fault happens and the fault interrupt can be captures one by one， with flow 2， we can only know what and how many fault event happens。



Interrupt Flow Chart 1



Interrupt Flow Chart 2

Register Table. Type Indicator R: Read Only W：Write Only R/W: Read & Write

Reg Add	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Type	Default(B)	Default(H)
0x00	DeviceID_1[7:0]								R	1000 0010	82
0x01	DeviceID_2[7:0]								R	0011 0011	33
0x02	Reserved	Output Discharge Resistor							R/W	0000 0000	00
0x03	LDO1_VOUT[7:0]								R/W	0101 1000	58
0x04	LDO2_VOUT[7:0]								R/W	0101 1000	58
0x05	LDO3_VOUT[7:0]								R/W	1010 0010	A2
0x06	LDO4_VOUT[7:0]								R/W	1010 0010	A2
0x07	LDO5_VOUT[7:0]								R/W	1010 0010	A2
0x08	LDO6_VOUT[7:0]								R/W	1010 0010	A2
0x09	LDO7_VOUT[7:0]								R/W	1010 0010	A2
0x0A	LDO2_SEQ [3:0]				LDO1_SEQ [3:0]				R/W	0000 0000	00
0x0B	LDO4_SEQ [3:0]				LDO3_SEQ [3:0]				R/W	0000 0000	00
0x0C	LDO6_SEQ [3:0]				LDO5_SEQ [3:0]				R/W	0000 0000	00
0x0D	Reserved				LDO7_SEQ [3:0]				R/W	0000 0000	00
0x0E	SYS_EN	LDOx_EN							R/W	1000 0000	80
0x0F	SEQ_SPEED[1:0]		SEQ_CTRL[1:0]		SEQ_ON	SEQ_COUNT[2:				0000 0000	00
	R/W		R/W		R	R					
0x10	LDO1_STATUS								R	0100 0000	40
0x11	Reserved	LDO1_OCP_CTL							R/W	1100 0000	C0
0x12	LDO2_STATUS								R	0100 0000	40
0x13	Reserved	LDO2_OCP_CTL							R/W	1100 0000	C0
0x14	LDO3_STATUS								R	0100 0000	40
0x015	Reserved	LDO3_OCP_CTL							R/W	1100 0000	C0
0x16	LDO4_STATUS								R	0100 0000	40
0x17	Reserved	LDO4_OCP_CTL							R/W	1100 0000	C0
0x18	LDO5_STATUS								R	0100 0000	40
0x19	Reserved	LDO5_OCP_CTL							R/W	1100 0000	C0
0x1A	LDO6_STATUS								R	0100 0000	40
0x1B	Reserved	LDO6_OCP_CTL							R/W	1100 0000	C0
0x1C	LDO7_STATUS								R	0100 0000	40
0x1D	Reserved	LDO7_OCP_CTL							R/W	1100 0000	C0
0x1E	Reprogrammable I2C Address								R/W	0000 0000	00
0x1F	Reserved								R/W	0000 0000	00
0x20	INT_LATCHED_CLR								W	0000 0000	00
0x21	INT_EN_SET								R/W	0000 0000	00
0x22	INT_LATCHED_STS								R	0000 0000	00
0x23	INT_PENDING_STS								R	0000 0000	00
0x24	UVLO_CTL								R/W	0001 1110	1E
0x25	Reserved								R/W	0000 0000	00

Registers Function Description

0x00: DeviceID_1

Mode: Read only

Reset: 1000 0010

This is the device ID with revision information

0x01: DeviceID_2

Mode: Read only. Reset: 0011 0011

This is the device ID with revision information

0x02: R_SD [6:0]

Mode: Read/Write Reset: 0000 0000

The 7LSB control bits used for setting output speed discharge resistor. Bit0 to Bit6 for LDO1 to LDO7 respectively.

"0": enable speed discharge.

"1": no speed discharge.

0x03: LDO1_VOUT [7:0]

Mode: Read/Write Reset: 0101 1000

7 LSB is used for LDO1 output voltage set. VOUT1=0.496V+LDO1_VOUT [6:0]*0.008. Program range: 0.496V~1.512V, default VOUT1=1.2V. It can be trimmed to 8-bit program range of 0.496V~2.536V.

0x04: LDO2_VOUT [7:0]

Mode: Read/Write Reset: 0101 1000

7 LSB used for 7-bit LDO2 output voltage set. VOUT2=0.496V+LDO2_VOUT [6:0]*0.008. Program range: 0.496V~1.512V, default VOUT2=1.2V. It can be trimmed to 8-bit program range of 0.496V~2.536V. Used for sensor DVDD.

Dec.	Binary	Hex.	Voltage (V)	Dec.	Binary	Hex.	Voltage (V)
0	0000 0000	00H	0.496	75	0100 1011	4BH	1.096
1	0000 0001	01H	0.504	76	0100 1100	4CH	1.104
2	0000 0010	02H	0.512	77~80	***** ****		
3	0000 0011	03H	0.520	81	0101 0001	51H	1.144
4~62	**** ****			82	0101 0010	52H	1.152
63	0011 1111	3FH	1.000	83	0101 0011	53H	1.16
64	0100 0000	40H	1.008	84	0101 0100	54H	1.168
65	0100 0001	41H	1.016	85	0101 0101	55H	1.176
66	0100 0010	42H	1.024	86	0101 0110	56H	1.184
67	0100 0011	43H	1.032	87	0101 0111	57H	1.192
68	0100 0100	44H	1.040	88	**0101 1000**	**58H**	**1.200**
69	0100 0101	45H	1.048	89	0101 1001	59H	1.208
70	0100 0110	46H	1.056	90~254	**** ****		
71~74	**** ****			255	1111 1111	FFH	2.536

0x05 to 0x09: LDOx_VOUT [7:0]

Mode: Read/Write Reset: 1010 0010

These are the 8-bit registers to set the LDO3 to LDO7 output voltage, the output Voltage VOUTx=1.504V+LDOx_VOUT [7:0]*0.008. Program range: 1.504V~3.544V, default VOUT3x=2.8V.

Dec.	Binary	Hex.	Voltage (V)	Dec.	Binary	Hex.	Voltage (V)
0	0000 0000	00H	1.504	**162**	**1010 0010**	**A2H**	**2.800**
1	0000 0001	01H	1.512	163	1010 0011	A3H	2.808
2	0000 0010	02H	1.520	164	1010 0100	A4H	2.816
3	0000 0011	03H	1.528	165	1010 0101	A5H	2.824
4~35	**** ****			166	1010 0110	A6H	2.832
36	0010 0100	24H	1.792	167	1010 0111	A7H	2.840
37	0010 0101	25H	1.800	168	1010 1000	A8H	2.848
38	0010 0110	26H	1.808	169	1010 1001	A9H	2.856
39	0010 0111	27H	1.816	170	1010 1010	AAH	2.864
40	0010 1000	28H	1.824	171	1010 1011	ABH	2.872
41	0010 1001	29H	1.832	172	1010 1100	ACH	2.880
42	0010 1010	2AH	1.840	173~254	**** ****		
43~161	**** ****			255	1111 1111	FFH	3.544

0x0A, 0x0B, 0x0C and 0x0D: LDOx_SEQ [3:0]

Mode: Read/Write Reset: 0000 0000

These are the registers to define the power up and shut down sequence slot of the LDOs. The sequence is defined by assigning the LDO into one of the 7 time slots. The Power Up sequence is start from slot1 to slot7 if SEQ_ON in 0x0F register changes from 0 to 1, and the Shut Down sequence starts from slot7 to slot1 if SEQ_ON changes from 1 to 0. Any LDO can be assigned to any time slot for very flexible Power Up/Down sequence. If the LDOx_SEQ[3:0] is set to 0000, the LDOx power up/down is controlled by the LDOx_EN bit in 0x0E instead of by the sequencer, the default setting is 0000 which means the LDOx power up/down is controlled by the individual LDOx_EN bit in 0x0E..

LDOx_SEQ[3:0]	Enable signal
0000	Controlled by register 0x0E
x001	slot1
x010	slot2
x011	slot3
x100	slot4
x101	slot5
x110	slot6
x111	slot7

0x0E: LDOx_EN

Mode: Read/Write Reset: 1000 0000

This register is for the System enable and individual LDO enable control. Bit7 is used for system enable. When bit7=0, the PMIC is shut down. When bit7=1 and RESET_N is pulled high, the system bias will be getting ready for enabling individual LDO. In the case that regulators are set to be controlled by register 0x0E (LDOx_SEQ[3:0]=0000), this register can be written to enable or disable the corresponding LDO.

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Enable signal	SYS_EN	LDO7_EN	LDO6_EN	LDO5_EN	LDO4_EN	LDO3_EN	LDO2_EN	LDO1_EN

0x0F: SEQ

Mode: Read/Write Reset: 0000 0000

This register set the sequencer for automatic power up/down sequence of the LDOs

SEQ_SPEED [1:0] (Bit [7:6])

These 2 bits define each slot period as following:

Register Value	Slot period (ms)
00	2
01	1
10	0.5
11	0.25

SEQ_CTRL [1:0] (Bit [5:4])

These 2 bit Enables power up or shut down sequence of the LDOs

Register Value	SEQ Status
x0	Shut down
x1	Power up

SEQ_ON (Bit [3])

The Indicator of the of sequencer status. Read only.

Register Value	SEQ Status
0	Shut down
1	Power up

SEQ_COUNT [2:0] (Bit [2:0])

The real time indicator the slot number of SEQ at the moment. Read only.

Register Value	SEQ Counter
000	No LDO starts.

001	The LDO assigned to slot1 starts.
010	The LDO assigned to slot2 starts.
011	The LDO assigned to slot3 starts.
100	The LDO assigned to slot4 starts.
101	The LDO assigned to slot5 starts.
110	The LDO assigned to slot6 starts.
111	The LDO assigned to slot7 starts and stop counting.

0x10: LDO1_STATUS

Mode: Read only Reset: 0000 0000

LDO1 Status

Bits	Name	Description
0	VIN12 OK	Indicate VIN12 status when LDO1 is enabled. 1=VIN12 OK 0=VIN12 is Locked Out
1	Not Used	
2	Stepper_Done	Indicate stepper is done when LDO is enabled or Vset is changed 1=Stepper done 0=Stepper is stepping
[4:3]	Not Used	
5	LDO1_OCP	The signal driving this bit is the OCP_LATCHED_STS signal that only resets with RESET_N pin or by writing to OCP_STATUS_CLR bit in register 0x11 1=Over Current has been detected/latched. 0=No fault detected.
6	LDO1_ERROR	1=Regulator is not stepping and fallen below VREG1_OK comparator threshold, or done stepping/softstart and not reached VREG1_OK comparator threshold. 0=Regulator is okay.
7	LDO1_READY	1=Regulator is settled and ready to use. 0=Regulator is not ready due to stepping or soft-start in progress or below the de-bounced VREG1_OK comparator threshold.

0x11: LDO1_OCP_CTL

Mode: Read/Write Reset: 1100 0000

Bits	Name	Description
0:0	Reserved	This bit should always be 0
1:1	OCP_STATUS_CLR	Writing a 1 to this bit clears the LDO1_OCP bit in LDO1_STATUS. This bit must then be toggled from 1 to 0 to re-arm the status bit so that it can be latched in the event of another OCP event.
2:2	OCP_GLOBAL _BROADCAST_EN	Determines if the LDO initiate the interrupt when OCP happens1=LDO initiates the interruption when OCP happens 0=LDO doesn't initiates the interruption when OCP happens (DEFAULT).
3:3	Not Used	

5:4	OCP_DEB	Debounce time for OCP detection 00: DEB_120us 01: DEB_240us 10: DEB_480us 11: DEB_960us
6:6	OCP_SELF_ SHUTDOWN_EN	Determines if the LDO1 performs self-shutdown upon OCP event. 1=LDO1 self-shutdowns upon OCP event (DEFAULT) 0=LDO1 does not self-shutdown upon OCP event.
7:7	OCP_EN	1=Enable OCP feature (DEFAULT) 0=Disable OCP feature

0x12: LDO2_STATUS

Mode: Read only Reset: 0000 0000

Bits	Name	Description
0:0	VIN12 OK	Indicate VIN12 is OK when LDO2 is enabled. 1=VIN12 OK 0=VIN12 is Locked Out
1:1	Not Used	
2:2	Stepper_Done	Indicate stepper is done when LDO is enabled or Vset is changed 1=Stepper done 0=Stepper is stepping
4:3	Not Used	
5:5	LDO2_OCP	The signal driving this bit is the OCP_LATCHED_STS signal that only resets with RESET_N pin or by writing to OCP_STATUS_CLR bit in register 0x13 1=Over Current has been detected/latched. 0=No fault detected.
6:6	LDO2_ERROR	1=Regulator is not stepping and fallen below VREG2_OK comparator threshold, or done stepping/softstart and not reached VREG2_OK comparator threshold. 0=Regulator is okay.
7:7	LDO2_READY	1=Regulator is settled and ready to use. 0=Regulator is not ready due to stepping or soft-start in progress or below the de-bounced VREG2_OK comparator threshold.

0x13: LDO2_OCP_CTL

Mode: Read/Write Reset: 1100 0000

Bits	Name	Description
0:0	Reserved	This bit should always be 0
1:1	OCP_STATUS_C LR	Writing a 1 to this bit clears the LDO2_OCP bit in LDO2_STATUS. This bit must then be toggled from 1 to 0 to re-arm the status bit so that it can be latched in the event of another OCP event.
2:2	OCP_GLOBAL _ BROADCAST_EN	Determines if the LDO initiate the interrupt when OCP happens1=LDO initiates the interruption when OCP happens 0=LDO doesn't initiates the interruption when OCP happens (DEFAULT).
3:3	Not Used	

5:4	OCP_DEB	Debounce time for OCP detection 00: DEB_120us 01: DEB_240us 10: DEB_480us 11: DEB_960us
6:6	OCP_SELF_ SHUTDOWN_EN	Determines if the LDO2 performs self-shutdown upon OCP event. 1=LDO2 self-shutdowns upon OCP event (DEFAULT) 0=LDO2 does not self-shutdown upon OCP event.
7:7	OCP_EN	1=Enable OCP feature (DEFAULT) 0=Disable OCP feature

0x14: LDO3_STATUS

Mode: Read only Reset: 0000 0000

Bits	Name	Description
0:0	VIN34 OK	Indicate VIN34 is OK when LDO3 is enabled. 1=VIN34 OK 0=VIN34 is Locked Out
1:1	Not Used	
2:2	Stepper_Done	Indicate stepper is done when LDO is enabled or Vset is changed 1=Stepper done 0=Stepper is stepping
4:3	Not Used	
5:5	LDO3_OCP	The signal driving this bit is the OCP_LATCHED_STS signal that only resets with RESET_N pin or by writing to OCP_STATUS_CLR bit in register 0x15 1=Over Current has been detected/latched. 0=No fault detected.
6:6	LDO3_ERROR	1=Regulator is not stepping and fallen below VREG3_OK comparator threshold, or done stepping/softstart and not reached VREG3_OK comparator threshold. 0=Regulator is okay.
7:7	LDO3_READY	1=Regulator is settled and ready to use. 0=Regulator is not ready due to stepping or soft-start in progress or below the de-bounced VREG3_OK comparator threshold.

0x15: LDO3_OCP_CTL

Mode: Read/Write Reset: 1100 0000

Bits	Name	Description
0:0	Reserved	This bit should be always 0
1:1	OCP_STATUS_CLR	Writing a 1 to this bit clears the LDO3_OCP bit in LDO3_STATUS. This bit must then be toggled from 1 to 0 to re-arm the status bit so that it can be latched in the event of another OCP event.
2:2	OCP_GLOBAL _ BROADCAST_EN	Determines if the LDO initiate the interrupt when OCP happens1=LDO initiates the interruption when OCP happens

		0=LDO doesn't initiates the interruption when OCP happens (DEFAULT).
3:3	Not Used	
5:4	OCP_DEB	Debounce time for OCP detection 00: DEB_120us 01: DEB_240us 10: DEB_480us 11: DEB_960us
6:6	OCP_SELF_ SHUTDOWN_EN	Determines if the LDO3 performs self-shutdown upon OCP event. 1=LDO1 self-shutdowns upon OCP event (DEFAULT) 0=LDO1 does not self-shutdown upon OCP event.
7:7	OCP_EN	1=Enable OCP feature (DEFAULT) 0=Disable OCP feature

0x16: LDO4_STATUS

Mode: Read only Reset: 0000 0000

Name	Description
VIN34 OK	Indicate VIN34 is OK when LDO4 is enabled. 1=VIN34 OK 0=VIN34 is Locked Out
Not Used	
Stepper_Done	Indicate stepper is done when LDO is enabled or Voltage setting is changed 1=Stepper done 0=Stepper is stepping
Not Used	
LDO4_OCP	The signal driving this bit is the OCP_LATCHED_STS signal that only resets with RESET_N pin or by writing to OCP_STATUS_CLR bit in register 0x17 1=Over Current has been detected/latched. 0=No fault detected.
LDO4_ERROR	1=Regulator is not stepping and fallen below VREG4_OK comparator threshold, or done stepping/softstart and not reached VREG4_OK comparator threshold. 0=Regulator is okay.
LDO4_READY	1=Regulator is settled and ready to use. 0=Regulator is not ready due to stepping or soft-start in progress or below the de-bounced VREG4_OK comparator threshold.

0x17: LDO4_OCP_CTL

Mode: Read/Write Reset: 1100 0000

Bits	Name	Description
0:0	Reserved	This bit be always 1
1:1	OCP_STATUS_C LR	Writing a 1 to this bit clears the LDO4_OCP bit in LDO4_STATUS. This bit must then be toggled from 1 to 0 to re-arm the status bit so that it can be latched in the event of another OCP event.
2:2	OCP_GLOBAL _ BROADCAST_EN	Determines if the LDO initiate the interrupt when OCP happens1=LDO initiates the interruption when OCP happens 0=LDO doesn't initiates the interruption when OCP happens (DEFAULT).

3:3	Not Used	
5:4	OCP_DEB	Debounce time for OCP detection 00: DEB_120us 01: DEB_240us 10: DEB_480us 11: DEB_960us
6:6	OCP_SELF_ SHUTDOWN_EN	Determines if the LDO4 performs self-shutdown upon OCP event. 1=LDO4 self-shutdowns upon OCP event (DEFAULT) 0=LDO4 does not self-shutdown upon OCP event.
7:7	OCP_EN	1=Enable OCP feature (DEFAULT) 0=Disable OCP feature

0x18: LDO5_STATUS

Mode: Read only Reset: 0000 0000

Bits	Name	Description
0:0	VIN5 OK	Indicate VIN5 is OK when LDO5 is enabled. 1=VIN5 OK 0=VIN5 is Locked Out
1:1	Not Used	
2:2	Stepper_Done	Indicate stepper is done when LDO is enabled or Vset is changed 1=Stepper done 0=Stepper is stepping
4:3	Not Used	
5:5	LDO5_OCP	The signal driving this is the OCP_LATCHED_STS signal that only resets with RESET_N pin or by writing to OCP_STATUS_CLR bit in register 0x19 1=Over Current has been detected/latched. 0=No fault detected.
6:6	LDO5_ERROR	1=Regulator is not stepping and fallen below VREG5_OK comparator threshold, or done stepping/softstart and not reached VREG5_OK comparator threshold. 0=Regulator is okay.
7:7	LDO5_READY	1=Regulator is settled and ready to use. 0=Regulator is not ready due to stepping or soft-start in progress or below the de-bounced VREG5_OK comparator threshold.

0x19: LDO5_OCP_CTL

Mode: Read/Write Reset: 1100 0000

Bits	Name	Description
0:0	Reserved	This bit should be always 0
1:1	OCP_STATUS_C LR	Writing a 1 to this bit clears the LDO5_OCP bit in LDO5_STATUS. This bit must then be toggled from 1 to 0 to re-arm the status bit so that it can be latched in the event of another OCP event.
2:2	OCP_GLOBAL _ BROADCAST_EN	Determines if the LDO initiate the interrupt when OCP happens1=LDO initiates the interruption when OCP happens 0=LDO doesn't initiates the interruption when OCP happens (DEFAULT).
3:3	Not Used	

5:4	OCP_DEB	Debounce time for OCP detection 00: DEB_120us 01: DEB_240us 10: DEB_480us 11: DEB_960us
6:6	OCP_SELF_ SHUTDOWN_EN	Determines if the LDO5 performs self-shutdown upon OCP event. 1=LDO5 self-shutdowns upon OCP event (DEFAULT) 0=LDO5 does not self-shutdown upon OCP event.
7:7	OCP_EN	1=Enable OCP feature (DEFAULT) 0=Disable OCP feature

0x1A: LDO6_STATUS

Mode: Read only Reset: 0000 0000

Bits	Name	Description
0:0	VIN6 OK	Indicate VIN6 is OK when LDO6 is enabled. 1=VIN6 OK 0=VIN6 is Locked Out
1:1	Not Used	
2:2	Stepper_Done	Indicate stepper is done when LDO is enabled or Vset is changed 1=Stepper done 0=Stepper is stepping
4:3	Not Used	
5:5	LDO6_OCP	The signal driving this bit is the OCP_LATCHED_STS signal that only resets with RESET_N pin or by writing to OCP_STATUS_CLR bit in the register 0x1B 1=Over Current has been detected/latched. 0=No fault detected.
6:6	LDO6_ERROR	1=Regulator is not stepping and fallen below VREG6_OK comparator threshold, or done stepping/softstart and not reached VREG6_OK comparator threshold. 0=Regulator is okay.
7:7	LDO6_READY	1=Regulator is settled and ready to use. 0=Regulator is not ready due to stepping or soft-start in progress or below the de-bounced VREG6_OK comparator threshold.

0x1B: LDO6_OCP_CTL

Mode: Read/Write Reset: 1100 0000

Bits	Name	Description
0:0	Reserved	This bit should be always 0
1:1	OCP_STATUS _CLR	Writing a 1 to this bit clears the LDO6_OCP bit in LDO6_STATUS. This bit must then be toggled from 1 to 0 to re-arm the status bit so that it can be latched in the event of another OCP event.
2:2	OCP_GLOBAL _BROADCAST _EN	Determines if the LDO initiate the interrupt when OCP happens1=LDO initiates the interruption when OCP happens 0=LDO doesn't initiates the interruption when OCP happens (DEFAULT).
3:3	Not Used	

5:4	OCP_DEB	Debounce time for OCP detection 00: DEB_120us 01: DEB_240us 10: DEB_480us 11: DEB_960us
6:6	OCP_SELF_SHUTDOWN_EN	Determines if the LDO6 performs self-shutdown upon OCP event. 1=LDO6 self-shutdowns upon OCP event (DEFAULT) 0=LDO6 does not self-shutdown upon OCP event.
7:7	OCP_EN	1=Enable OCP feature (DEFAULT) 0=Disable OCP feature

0x1C: LDO7_STATUS

Mode: Read only Reset: 0000 0000

Bits	Name	Description
0:0	VIN7 OK	Indicate VIN7 is OK when LDO7 is enabled. 1=VIN7 OK 0=VIN7 is Locked Out
1:1	Not Used	
2:2	Stepper_Done	Indicate stepper is done when LDO is enabled or Vset is changed 1=Stepper done 0=Stepper is stepping
4:3	Not Used	
5:5	LDO7_OCP	The signal driving this bit is the OCP_LATCHED_STS signal that only resets with RESET_N pin or by writing to OCP_STATUS_CLR bit in register 0x1D 1=Over Current has been detected/latched. 0=No fault detected.
6:6	LDO7_ERROR	1=Regulator is not stepping and fallen below VREG7_OK comparator threshold, or done stepping/softstart and not reached VREG7_OK comparator threshold. 0=Regulator is okay.
7:7	LDO7_READY	1=Regulator is settled and ready to use. 0=Regulator is not ready due to stepping or soft-start in progress or below the de-bounced VREG7_OK comparator threshold.

0x1D: LDO7_OCP_CTL

Mode: Read/Write Reset: 1100 0000

Bits	Name	Description
0:0	Reserved	This bit should be always 0
1:1	OCP_STATUS_CLR	Writing a 1 to this bit clears the LDO7_OCP bit in LDO7_STATUS. This bit must then be toggled from 1 to 0 to re-arm the status bit so that it can be latched in the event of another OCP event.
2:2	OCP_GLOBAL _BROADCAST_EN	Determines if the LDO initiate the interrupt when OCP happens1=LDO initiates the interruption when OCP happens 0=LDO doesn't initiates the interruption when OCP happens (DEFAULT).
3:3	Not Used	
5:4	OCP_DEB	Debounce time for OCP detection 00: DEB_120us 01: DEB_240us 10: DEB_480us 11: DEB_960us
6:6	OCP_SELF_SHUTDOWN_EN	Determines if the LDO7 performs self-shutdown upon OCP event. 1=LDO7 self-shutdowns upon OCP event (DEFAULT) 0=LDO7 does not self-shutdown upon OCP event.
7:7	OCP_EN	1=Enable OCP feature (DEFAULT) 0=Disable OCP feature

0x1E: Dynamic I2C address change.

Mode: Read/Write Reset: 0000 0000

The default I2C address is 0101 111. Writing any data except 0x00H to this register will change the I2C address. The 7 LSB data is the new address. Writing 0x00H or after reset, the I2C address returns to 0101 111.

0x20: INT_LATCHED_CLR

Mode: Write Reset: 0000 0000

Writing a "1" to this register clears the corresponding latched register bits in 0x22 so as other fault condition can generate the interrupt.

Bits	Name	Description
0:0	UVLO_LATCHED_CLR	No description provided for this bit field.
1:1	Not used	
2:2	OTST2_LATCHED_CLR	No description provided for this bit field.
3:3	OTST3_LATCHED_CLR	No description provided for this bit field.
4:4	OCP_LATCHED_CLR	No description provided for this bit field.

0x21: INT_EN_SET

Mode: Read/Write Reset: 0000 0000

Writing 0/1 to this register bits will disable/enable the corresponding interrupt.

Bits	Name	Description
0:0	UVLO_EN_CLR	Enable/disable UVLO interrupt.
1:1	Not used	
2:2	OTST2_EN_CLR	Enable/disable OTST2 interrupt.
3:3	OTST3_EN_CLR	Enable/disable OTST3 interrupt.
4:4	OCP_EN_CLR	Enable/disable OCP interrupt.
6:5	IRQ Selection	Set the interrupt pulse width 00: Always high 01: 8ms Pulse 10: 16ms Pulse 11: 32ms Pulse
7:7	INTERRUPT_MASK	Set 1 to mask all interrupt.

0x22: INT_LATCHED_STS

Mode: Read Reset: 0000 0000

Latched (Sticky) Interrupt. '1' indicates that the interrupt has triggered. Once the latched bit is set it can only be cleared by writing the clear bit in register INT_LATCHED_CLR 0x20. The OCP_Latched_STS is the global OCP event indication, to know the exact LDO channel triggering the interrupt latch, the user need to read the LDOx_Status registers to get the information

Note: Register 0x0EH is used to enable/disable LDOs. Its default value is 1000 0000. When RESET_N="1", the WL2868C will be at standby mode with I_q = 40uA. Any operation changing 0x0EH value from 1xxx xxxx to 0000 0000 to put WL2868C in sleep mode with Iq=2uA would latch the UVLO_LATCHED_STS bit of 0x22H register, so 0x22H register should be cleared by writing the 0x20 register UVLO_LATCHED_CLR bit to avoid the mistake interrupt before getting back to normal operation.

Bits	Name	Description
0:0	UVLO_LATCHED_STS	No description provided for this bit field.
1:1	Not used	
2:2	OTST2_LATCHED_STS	No description provided for this bit field.
3:3	OTST3_LATCHED_STS	No description provided for this bit field.
4:4	OCP_LATCHED_STS	No description provided for this bit field.

0x23: INT_PENDING_STS

Mode: Read Reset: 0000 0000

The interrupt source is stored in this register. Pending is set if there is the interrupt has been sent but not cleared. The bit in set state is the source which initiate the interrupt, only one bit is set at one time even if there are multiple fault condition happened in the INT_Latched_STS register. INT_Latched_Clear register bit need to be cleared so as other fault event can generate the interrupt signal. For OCP interrupt, Both the OCP_LATCHED_CLR bit in 0x20 and the individual OCP_STATUS_CLR bits need to be set so as other fault event can initiate the interrupt

Bits	Name	Description
0:0	UVLO_PENDING_STS	Indication of the VSYS UVLO fault event
1:1	Not used	
2:2	OTST2_ PENDING _STS	Indication of the OTST2 fault event.
3:3	OTST3_ PENDING _STS	Indication of the OTST3 fault event.
4:4	OCP_ PENDING _STS	Indication of the OCP fault event.

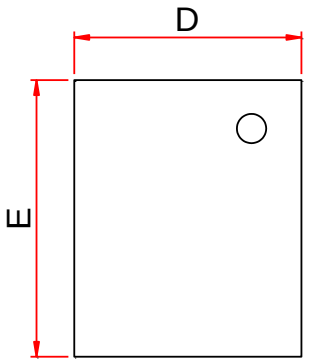
0x24: UVLO_CTL

Mode: Read/Write Reset: 0001 1110

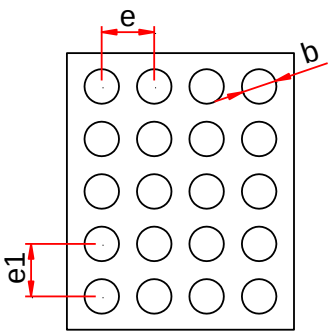
Bits	Name	Description
4:0	UVLO_THRESHOLD	UVLO Rising Threshold = 1.5V+0.05*X; default/reset value is 3.00V. 0:V_1p85 1: V_1p85 2: V_1p85 3: V_1p85 4: V_1p85 5: V_1p85 6:V_1p85 7: V_1p85 8: V_1p90 9: V_1p95 10: V_2p00 11: V_2p05 12:V_2p10 13:V_2p15 14:V_2p20 15:V_2p25 16: V_2p30 17:V_2p35 18:V_2p40 19:V_2p45 20:V_2p50 21:V_2p55 22:V_2p60 23:V_2p65 24:V_2p70 25:V_2p75 26:V_2p80 27:V_2p85 28:V_2p90 29:V_2p95 30:V_3p00 31:V_3p05
6:5	UVLO_HYST	Falling threshold = Rising threshold - Hysteresis. UVLO Hysteresis setting: 00=150mV (default/reset value), 01=300mV, 10=450mV, 11=600mV
7:7	Not used	

PACKAGE OUTLINE DIMENSIONS

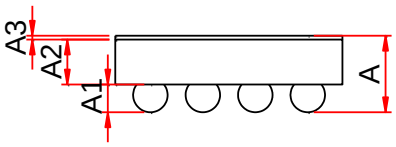
CSP-20L



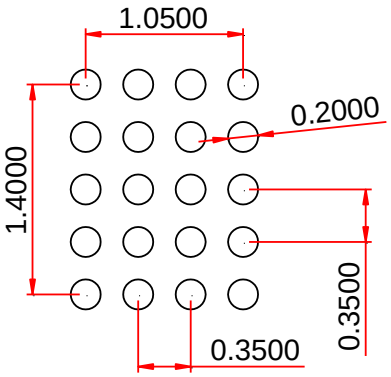
TOP VIEW



BOTTOM VIEW



SIDE VIEW

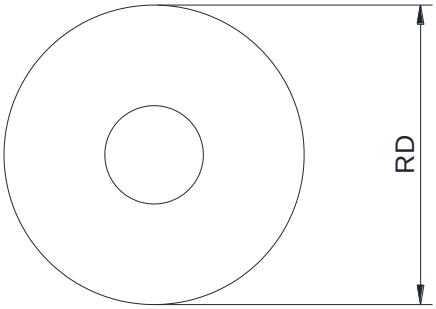


RECOMMENDED LAND PATTERN(Unit:mm)

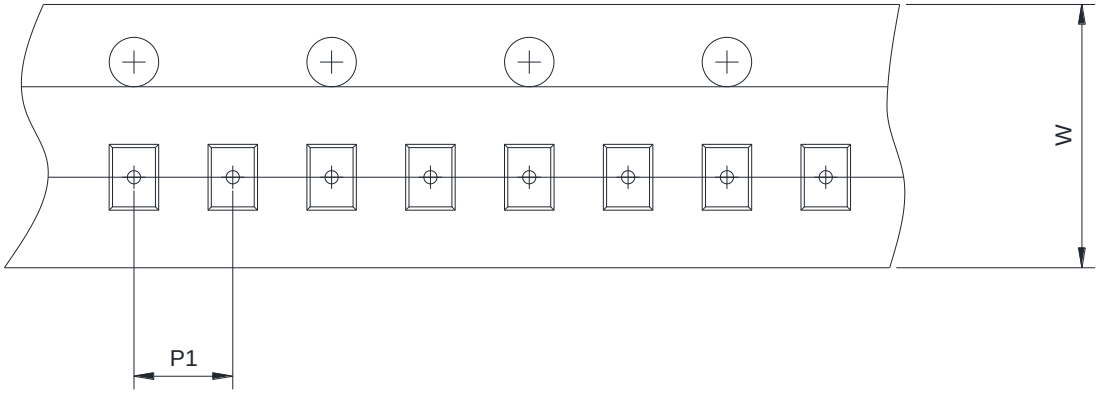
Symbol	Dimensions in Millimeters		
	Min.	Nom	Max.
A	0.47	0.51	0.55
A1	0.16	0.19	0.21
A2	0.31	0.32	0.34
A3	0.025 Ref.		
b	0.21	0.23	0.25
D	1.49	1.52	1.54
E	1.82	1.85	1.87
e/e1	0.35BSC		

TAPE AND REEL INFORMATION

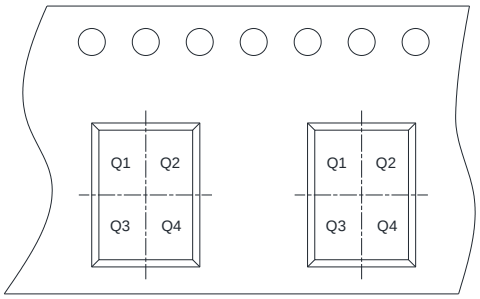
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



User Direction of Feed

RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☑ Q2	☐ Q3	☐ Q4

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