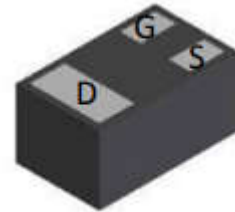
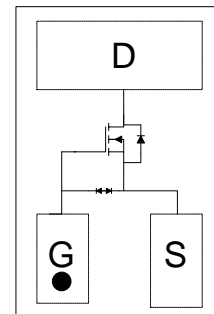


WNM2046E
Single N-Channel, 20V, 0.8A, Power MOSFET
[Http://www.sh-willsemi.com](http://www.sh-willsemi.com)

V_{DS} (V)	Max. $R_{DS(on)}$ (m Ω)
20	500 @ $V_{GS}=4.5V$
	570 @ $V_{GS}=3.1V$
	700 @ $V_{GS}=2.5V$
	1500 @ $V_{GS}=1.8V$
ESD Rating: 2000V HBM	


DFN1006-3L
Description

The WNM2046E is N-Channel enhancement MOS Field Effect Transistor. Uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in DC-DC conversion, power switch and charging circuit. Standard Product WNM2046E is Pb-free.


Pin configuration (Top view)
Features

- Trench Technology
- Supper high density cell design
- Excellent ON resistance
- Extremely Low Threshold Voltage
- Small package DFN1006-3L



6 = Device Code
* = Month (A~Z)

Marking
Applications

- DC/DC converters
- Power supply converters circuit
- Load/Power Switching for portable device

Order information

Device	Package	Shipping
WNM2046E-3/TR	DFN1006-3L	10K/Tape&Reel

Absolute Maximum ratings

Parameter	Symbol	Maximum	Unit	
Drain-Source Voltage	V_{DS}	20	V	
Gate-Source Voltage	V_{GS}	± 10		
Continuous Drain Current ^d	I_D	$T_A=25^\circ\text{C}$	800	mA
		$T_A=70^\circ\text{C}$	640	
Pulsed Drain Current ^c	I_{DM}	3000	mA	
Power Dissipation ^a	P_D	$T_A=25^\circ\text{C}$	480	mW
		$T_A=70^\circ\text{C}$	305	
Operating Junction Temperature	T_J	-55 to 150	$^\circ\text{C}$	
Storage Temperature Range	T_{STG}	-55 to 150	$^\circ\text{C}$	

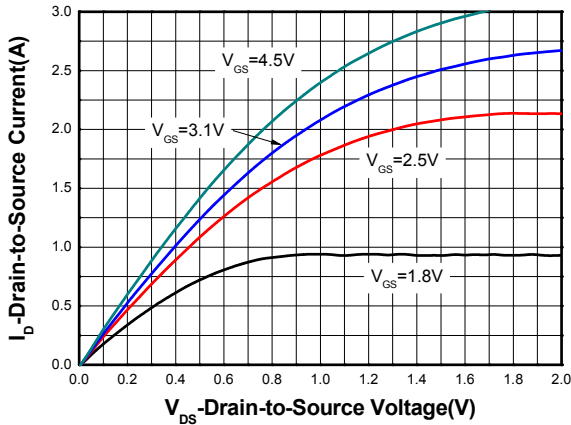
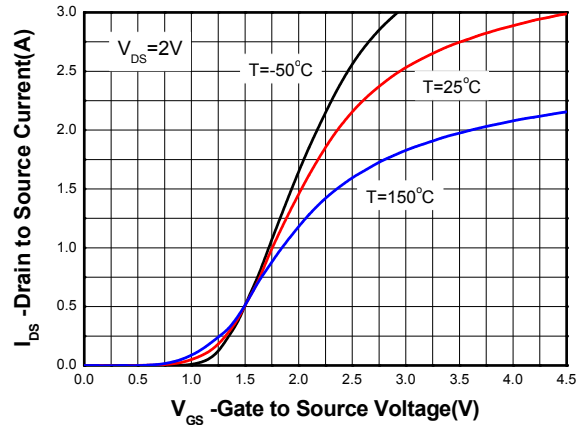
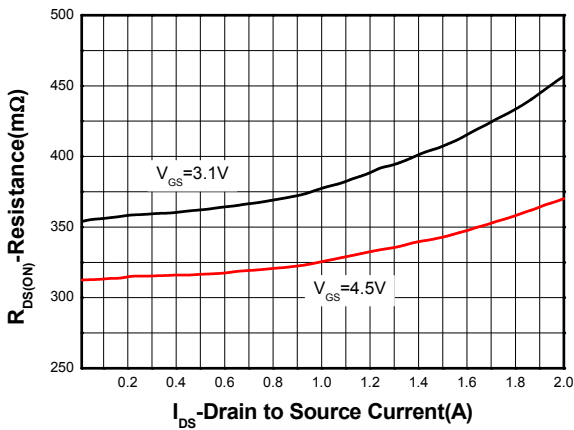
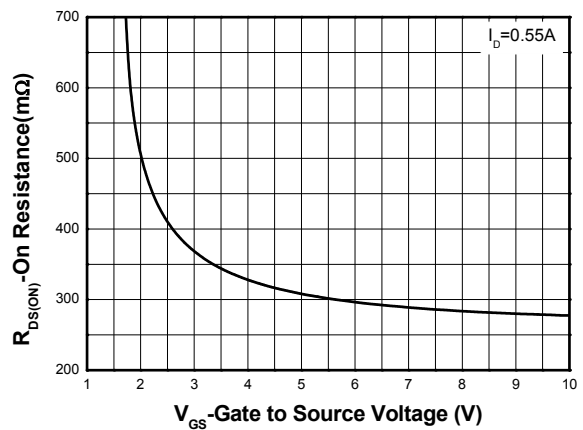
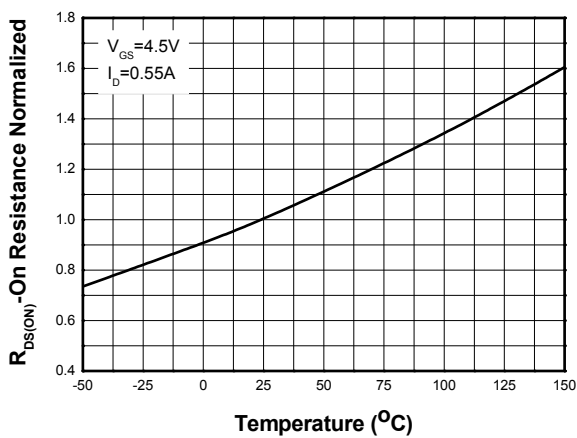
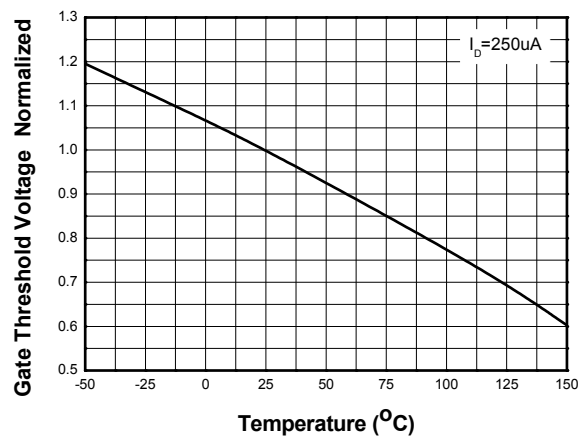
Thermal resistance ratings

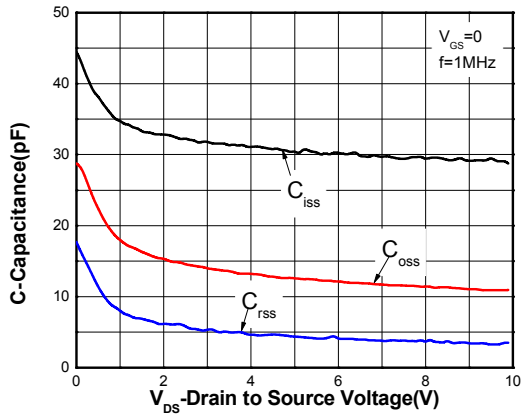
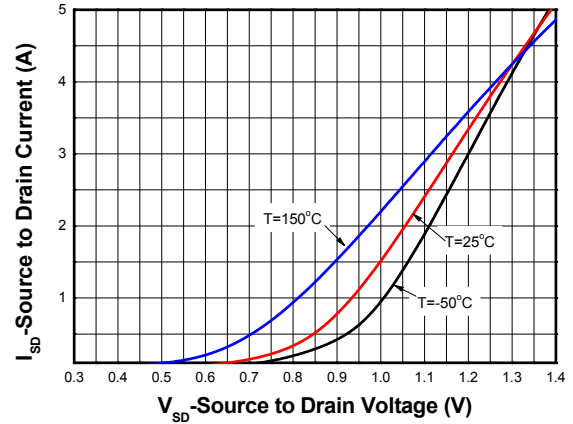
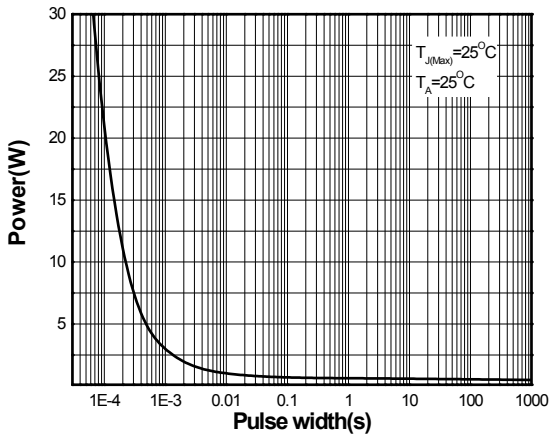
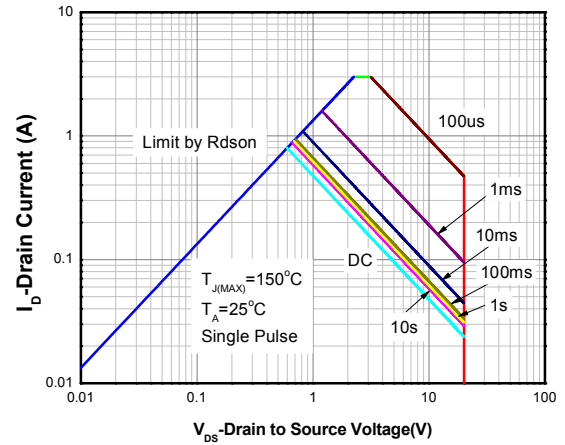
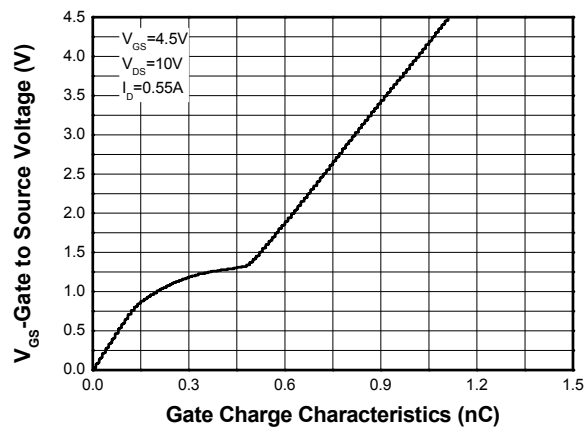
Single Operation				
Parameter		Symbol	Maximum	Unit
Junction-to-Ambient Thermal Resistance ^a	$t \leq 10 \text{ s}$	$R_{\theta JA}$	216	$^\circ\text{C/W}$
	Steady State		262	
Junction-to-Ambient Thermal Resistance ^b	$t \leq 10 \text{ s}$	$R_{\theta JA}$	464	
	Steady State		580	

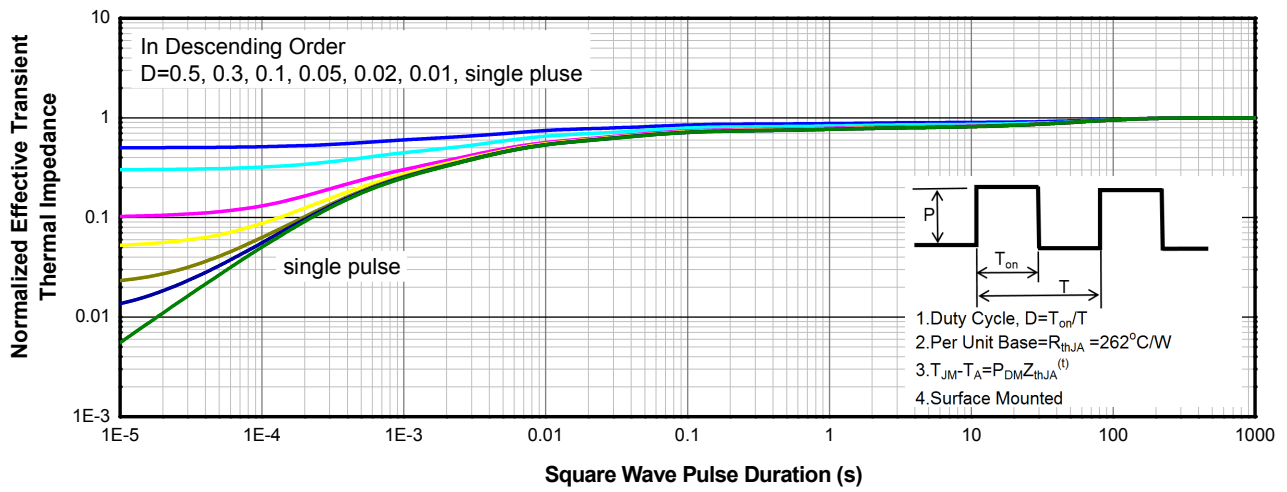
- a The value of $R_{\theta JA}$ is measured with the device mounted on 1-inch² (6.45cm²) with 2oz.(0.071mm thick) Copper pad on a 1.5*1.5 inch², 0.06-inch thick FR4 PCB, in a still air environment with $T_A = 25^\circ\text{C}$. The power dissipation P_D is based on $R_{\theta JA}$ value and the $T_{J(MAX)}=150^\circ\text{C}$. The value in any given application is determined by the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it to.
- b The value of $R_{\theta JA}$ is measured with the device mounted on FR-4 minimum pad board, in a still air environment with $T_A = 25^\circ\text{C}$. The power dissipation P_D is based on $R_{\theta JA}$ value and the $T_{J(MAX)}=150^\circ\text{C}$. The value in any given application is determined by the user's specific board design, and the maximum temperature of 150°C may be used if the PCB allows it to.
- c Repetitive rating, ~10us pulse width, duty cycle ~1%, keep initial $T_J = 25^\circ\text{C}$, the maximum allowed junction temperature of 150°C .
- d The maximum current rating by source bonding technology.
- e The static characteristics are obtained using ~380us pulses, duty cycle ~1%.

Electronics Characteristics (Ta=25°C, unless otherwise noted)

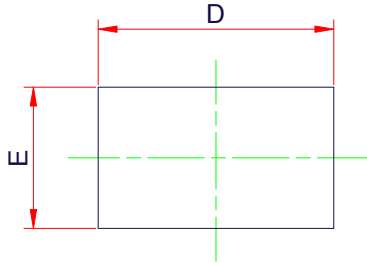
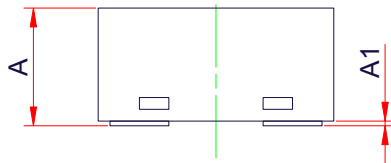
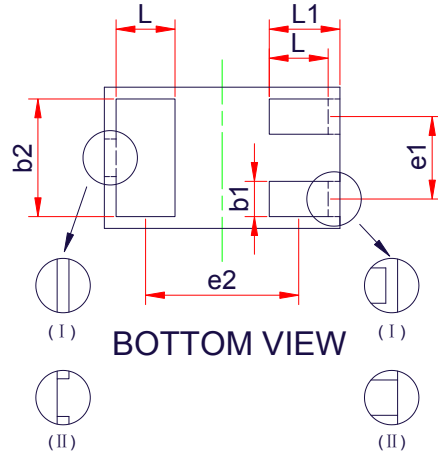
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 16\text{V}, V_{GS} = 0\text{V}$			1	μA
Gate-to-source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{V}$			± 10	μA
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	0.4	0.7	1.0	V
Drain-to-source On-resistance	$R_{DS(on)}$	$V_{GS} = 4.5\text{V}, I_D = 0.55\text{A}$		340	500	m Ω
		$V_{GS} = 3.1\text{V}, I_D = 0.35\text{A}$		380	570	
		$V_{GS} = 2.5\text{V}, I_D = 0.25\text{A}$		425	700	
		$V_{GS} = 1.8\text{V}, I_D = 0.15\text{A}$		560	1500	
CHARGES, CAPACITANCES AND GATE RESISTANCE						
Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{MHz}, V_{DS} = 10\text{ V}$		29		pF
Output Capacitance	C_{OSS}			11		
Reverse Transfer Capacitance	C_{RSS}			4		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{V}, I_D = 0.55\text{ A}$		1.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			0.11		
Gate-to-Source Charge	Q_{GS}			0.15		
Gate-to-Drain Charge	Q_{GD}			0.32		
SWITCHING CHARACTERISTICS						
Turn-On Delay Time	$t_d(ON)$	$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}, I_D = 0.55\text{A}, R_G = 6\Omega$		5		ns
Rise Time	t_r			5.8		
Turn-Off Delay Time	$t_d(OFF)$			15.4		
Fall Time	t_f			3.6		
BODY DIODE CHARACTERISTICS						
Forward Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 0.8\text{A}$		0.9	1.5	V

Typical Characteristics (Ta=25°C, unless otherwise noted)

Output Characteristics ^e

Transfer Characteristics ^e

On-Resistance vs. Drain Current ^e

On-Resistance vs. Gate-to-Source Voltage ^e

On-Resistance vs. Junction Temperature ^e

Threshold Voltage vs. Temperature

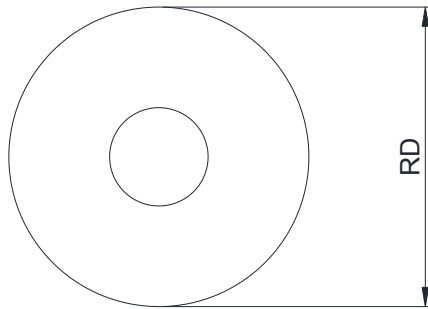
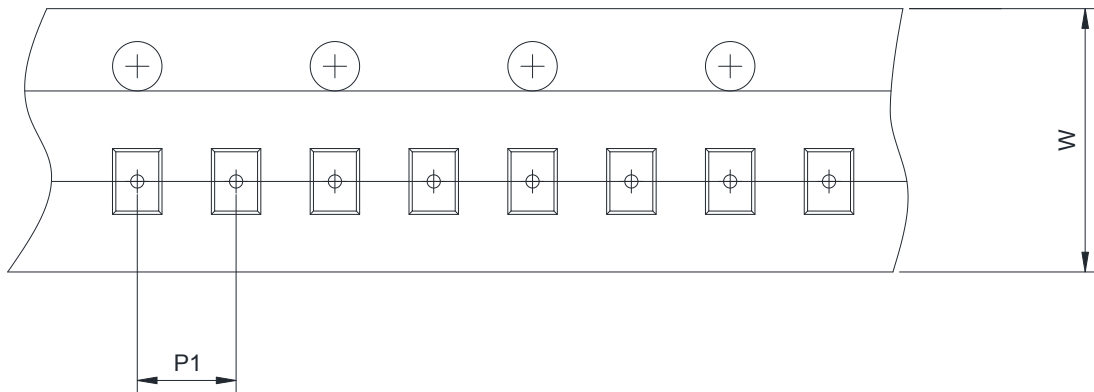
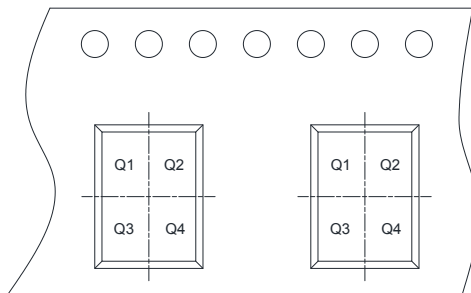

Capacitance

Body Diode Forward Voltage^e

Single Pulse power

Safe Operating Power

Gate Charge Characteristics



Transient Thermal Response (Junction-to-Ambient)

PACKAGE OUTLINE DIMENSIONS
DFN1006-3L

TOP VIEW

SIDE VIEW

BOTTOM VIEW

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.36	-	0.50
A1	0.00	-	0.05
D	0.95	1.00	1.05
E	0.55	0.60	0.65
b1	0.10	0.15	0.20
b2	0.40	0.50	0.60
L	0.20	0.25	0.30
L1	0.20	0.30	0.40
e1	0.35Ref		
e2	0.65Ref		

TAPE AND REEL INFORMATION
Reel Dimensions

Tape Dimensions

Quadrant Assignments For PIN1 Orientation In Tape



 User Direction of Feed

RD	Reel Dimension	<input checked="" type="checkbox"/> 7inch	<input type="checkbox"/> 13inch
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm	<input type="checkbox"/> 12mm <input type="checkbox"/> 16mm
P1	Pitch between successive cavity centers	<input checked="" type="checkbox"/> 2mm	<input type="checkbox"/> 4mm <input type="checkbox"/> 8mm
Pin1	Pin1 Quadrant	<input type="checkbox"/> Q1	<input type="checkbox"/> Q2 <input checked="" type="checkbox"/> Q3 <input type="checkbox"/> Q4

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