

# WS4639

## Configurable Reset Timer with Integrated Load Switch

[Http://www.sh-willsemi.com](http://www.sh-willsemi.com)

### Descriptions

The WS4639 is both a timer for resetting a mobile device and an advanced load management switches for applications requiring a highly integrated solution. Output auto-discharge while the device shutdown made output voltage off quickly. Thermal shutdown function can protect the device and load.

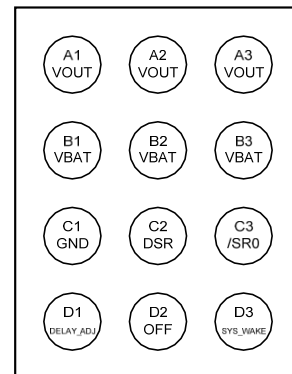
The WS4639 is available in CSP-12L package. Standard product is Pb-free and Halogen-free.

### Features

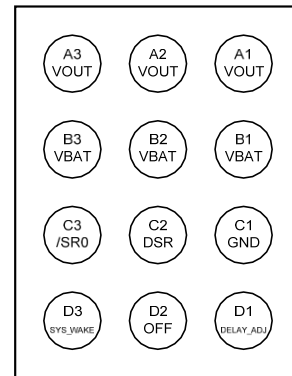
- Input voltage range : 1.8~5.5V
- Main switch  $R_{ON}$  : 23m $\Omega$  @  $V_{BAT}=3.8V$ , Typ.
- Continue output current :
  - 3.8A (JEDEC 2S2P, No VIA)
  - 4.5A (JEDEC 2S2P, Thermal VIA)
- Slew Rate / Inrush Control with  $t_R$ : 2.7ms (Typ.)
- Factory Programmed Reset Delay: 7.5s
- Factory Programmed Reset Pulse: 400ms
- Factory Customized Turn-on Time: 2.3s
- Factory Customized Turn-off Delay: 7.3s
- Adjustable Reset Delay Option with External Resistor
- Zero-Second Test-Mode Enable
- Over-Voltage Protection: Allow Input Pins >  $V_{BAT}$

### Applications

- Smart Phones
- Tablet PCs

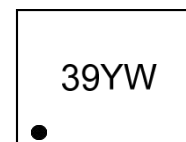


(Top View)



(Bottom View)

### Pin configuration



**39** = Device code

**Y** = Year code

**W** = Week code

### Marking

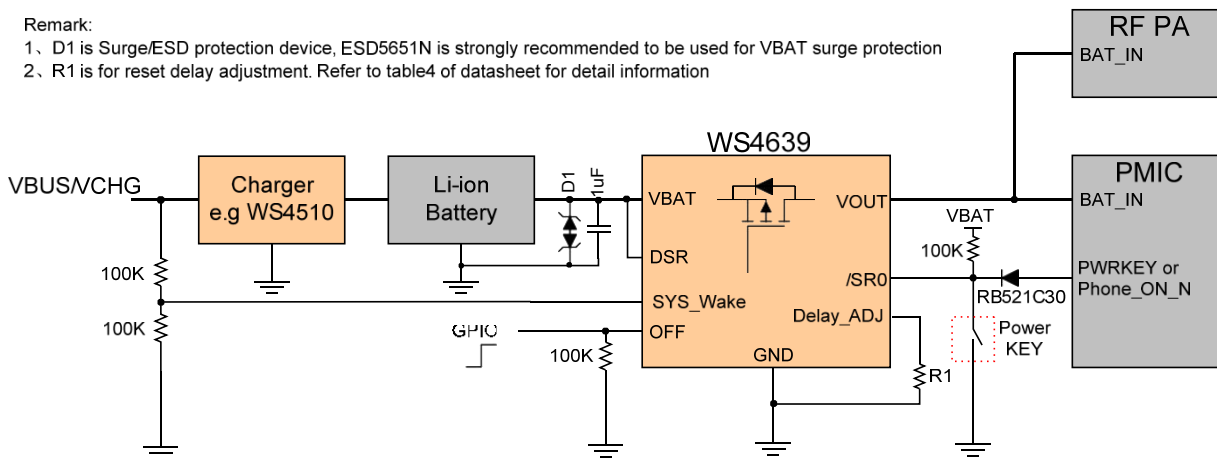
### Order information

Device	Package	Shipping
WS4639FC-12/TR	CSP-12L (1.16*1.56)	3000/Reel&Tape

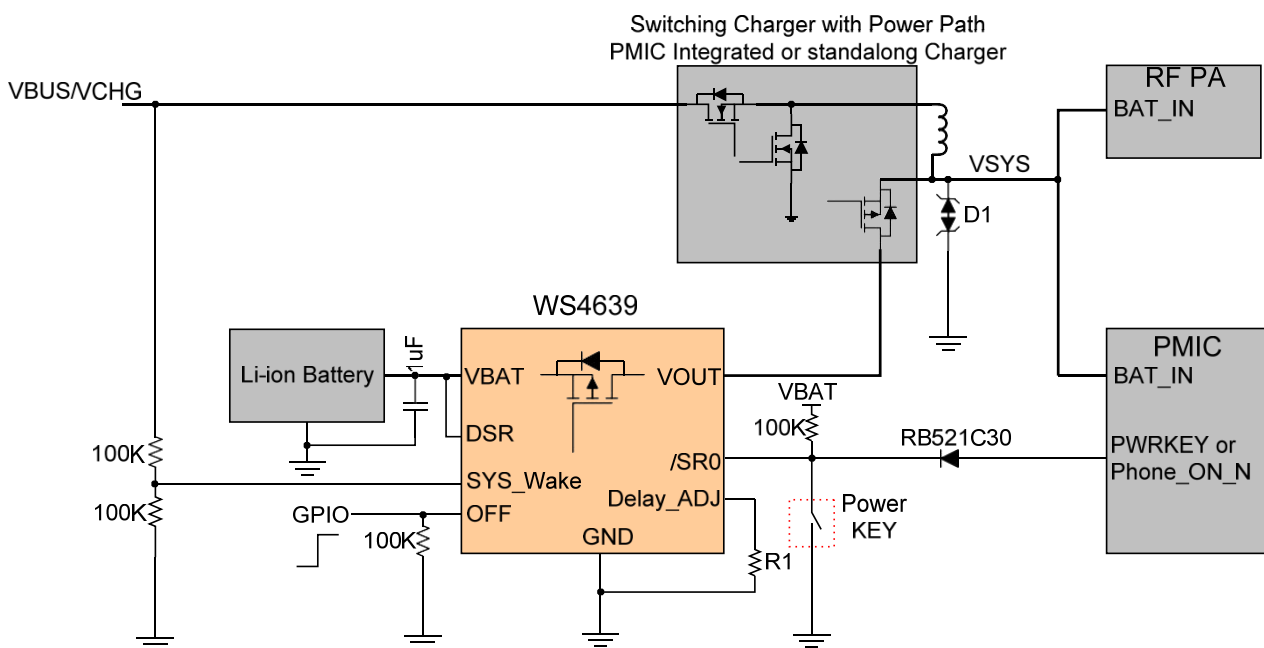
## Typical Applications

Remark:

- 1、 D1 is Surge/ESD protection device, ESD5651N is strongly recommended to be used for VBAT surge protection
- 2、 R1 is for reset delay adjustment. Refer to table4 of datasheet for detail information



**Figure 1. Typical Application without power path system**



Remark:

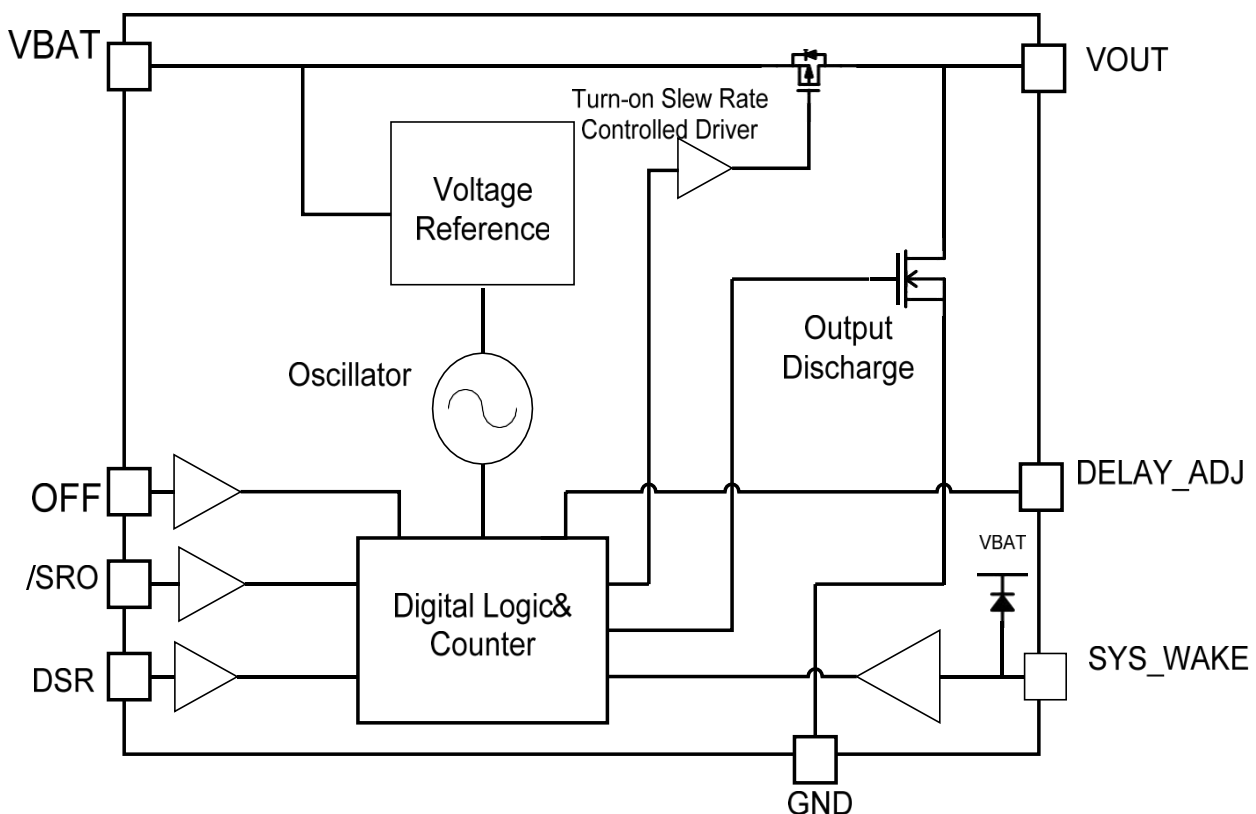
- 1、 D1 is Surge/ESD protection device, ESD5651N is strongly recommended to be used for VBAT surge protection
- 2、 R1 is for reset delay adjustment. Refer to table4 of datasheet for detail information

**Figure 2. Typical Application with power path system**

**Pin Descriptions**

Pin Number	Symbol	Descriptions	Zero-Second Factory Test-Mode <sup>(1)</sup>
A1, A2, A3	VOUT	Switch Output	Switch Output
B1, B2, B3	VBAT	Supply Input	Supply Input
C1	GND	Ground	Ground
C2	DSR	Delay selection input, connected to GPIO with 100KΩ pull-up or to VBAT directly without pull-up resistor	Logic Low Level
C3	/SR0	Power-on or reset input, active LOW	Logic Low Level
D1	DELAY_ADJ	Reset delay adjustment, Must tie to VBAT directly if not used. To adjust the reset delay, a resistor (R <sub>ADJ</sub> ) is connected between this pin and ground	Connect to VBAT or GND
D2	OFF	Load switch disable, Rising Edge Triggered, changes load switch from ON state to OFF state	NA
D3	SYS_WAKE	System wake-up input, changes load switch from OFF state to ON state	NA

**Note:** (1) Zero-Second Factory Test-Mode applies only to  $t_{VON}$  and  $t_{PHL1}$ .

**Block Diagram**


**Figure 3. Block Diagram**

### Absolute maximum ratings

Parameter	Symbol	Value	Unit
VBAT VOUT pin voltage range	$V_{BAT}, V_{OUT}$	-0.3~6.5	V
Other pin voltage range	V	-0.3~5.5	V
Power Dissipation @25 °C, ( $I_{OUT} = 4.5A$ )	$P_D$	0.34	W
Junction-to-Ambient Thermal Resistance	$\theta_{JA}$	85	°C/W
Junction-to-Case Thermal Resistance	$\theta_{JC}$	48	°C/W
Junction temperature	$T_J$	150	°C
Lead temperature(Soldering, 10s)	$T_L$	260	°C
Storage temperature	Tstg	-65 ~ 150	°C
VBAT VOUT Pin ESD Ratings	HBM	10000	V
	CDM	2000	V
All other Pins ESD Ratings	HBM	8000	V
	CDM	2000	V

These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

### Recommend Operating Conditions

Parameter	Symbol	Value	Unit
VBAT pin voltage range <sup>(1)</sup>	$V_{BAT}$	1.8 ~ 5.5	V
/SR0, DSR, OFF, VOUT pin voltage range	V	0 ~ 5.5	V
SYS_WAKE pin voltage range		0 ~ VBAT	V
Operating ambient temperature	$T_A$	-40 ~ 85	°C

**Note:** (1) When input pin have a voltage, ban VBAT float

**DC Electronics Characteristics (Ta=25°C, V<sub>BAT</sub>=4.5V, unless otherwise noted)**

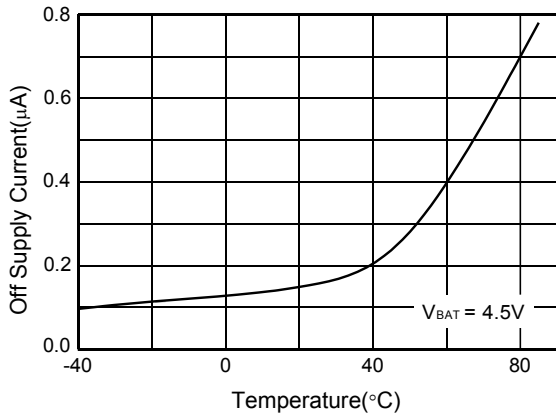
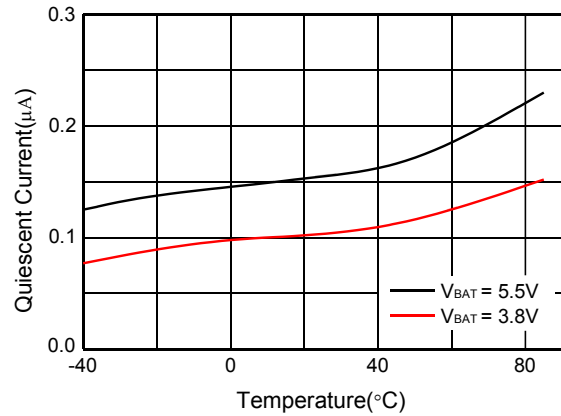
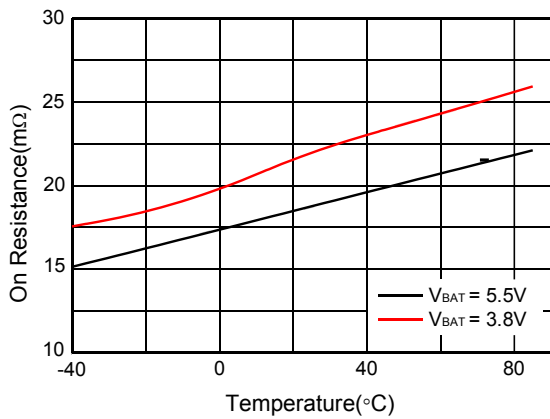
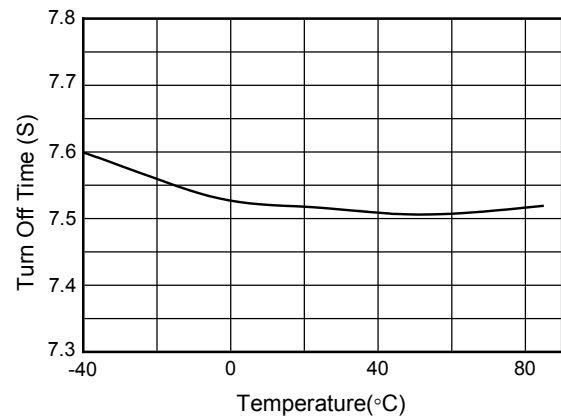
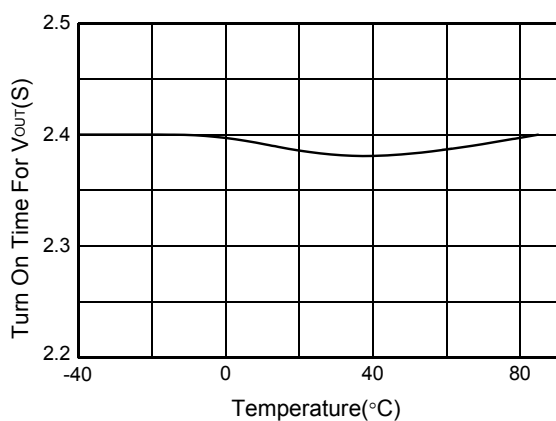
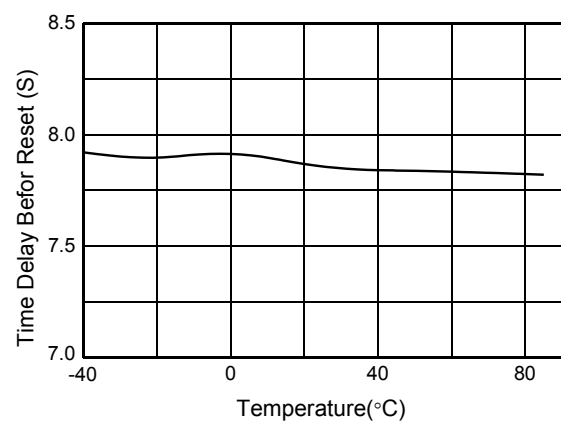
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
<b>Basic Operation</b>							
Off Supply Current	I <sub>OFF</sub>	V <sub>BAT</sub> =4.5V, V <sub>OUT</sub> =Open, Load Switch = OFF	Ta=25 °C		0.2	1	uA
			Ta=-40~85 °C			3	uA
		V <sub>BAT</sub> =4.5V, V <sub>OUT</sub> =GND, Load Switch = OFF	Ta=25 °C		0.2	1	uA
			Ta=-40~85 °C			3	uA
		V <sub>BAT</sub> =3.8V, V <sub>OUT</sub> =GND, Load Switch = OFF	Ta=25 °C		0.1	1	uA
			Ta=-40~85 °C			3	uA
On Resistance	R <sub>ON</sub>	V <sub>BAT</sub> =5.5V, I <sub>OUT</sub> =1A <sup>(1)</sup>			20	24	mΩ
		V <sub>BAT</sub> =4.5V, I <sub>OUT</sub> =1A <sup>(1)</sup>			21	25	
		V <sub>BAT</sub> =3.8V, I <sub>OUT</sub> =500mA <sup>(1)</sup>			23	28	
		V <sub>BAT</sub> =3.3V, I <sub>OUT</sub> =500mA <sup>(1)</sup>			24	29	
		V <sub>BAT</sub> =2.5V, I <sub>OUT</sub> =500mA <sup>(1)</sup>			28	35	
		V <sub>BAT</sub> =1.8V, I <sub>OUT</sub> =250mA <sup>(1)</sup>			37	45	
Output Discharge R <sub>PULL DOWN</sub>	R <sub>PD</sub>	V <sub>BAT</sub> =4.5V, V <sub>OUT</sub> = OFF, I <sub>FORCE</sub> =20mA			65	85	Ω
Input High Voltage <sup>(2)</sup>	V <sub>IH</sub>	1.8V≤V <sub>BAT</sub> ≤5.5V		1.2			V
Input Low Voltage <sup>(2)</sup>	V <sub>IL</sub>					0.4	V
Input Leakage Current <sup>(2)</sup>	I <sub>IN</sub>	0V≤V <sub>BAT</sub> ≤5.5V				±1	uA
Quiescent Current	I <sub>CCQ</sub>	/SR0=5.5V, DSR=5.5V, SYS_WAKE=5.5V, OFF =GND, I <sub>OUT</sub> =0mA, V <sub>BAT</sub> =5.5V, Load Switch=ON			0.3	3	μA
		/SR0=3.8V, DSR=3.8V, SYS_WAKE=3.8V, OFF=GND, I <sub>OUT</sub> =0mA, V <sub>BAT</sub> =3.8V, Load Switch=ON			0.1	3	μA
	I <sub>CCT</sub>	DSR=OFF=GND, /SR0 = SYS_WAKE=1.2V, V <sub>BAT</sub> =5.5V, Load Switch=ON			2	6	μA
Dynamic Current	Supply I <sub>CC</sub>	/SR0=GND, DSR=5.5V, V <sub>BAT</sub> =5.5V, Load Switch =ON			20	40	μA

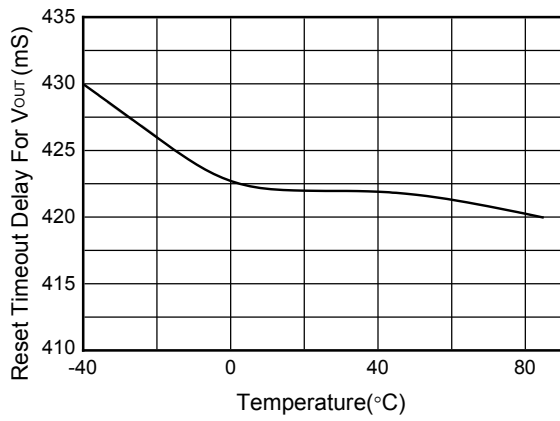
**AC Electronics Characteristics (Ta=25°C, V<sub>BAT</sub>=4.5V, unless otherwise noted)**

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
<b>Power-On and Reset Timing</b>						
Turn-On Time for V <sub>OUT</sub>	t <sub>VON</sub>	C <sub>L</sub> =5pF, R <sub>L</sub> =5kΩ, DSR= HIGH, Figure 19	1.8	2.3	2.8	s
Timer Delay before Reset	t <sub>PHL1</sub>	C <sub>L</sub> =5pF, R <sub>L</sub> =5kΩ, DSR= HIGH, Figure 20	6.0	7.5	9.0	s
Reset Timeout Delay of V <sub>OUT</sub>	t <sub>REC1</sub>	C <sub>L</sub> =5pF, R <sub>L</sub> =5kΩ, Figure 20	320	400	480	ms
<b>Load Switch Turn-On Timing</b>						
Turn-On Delay <sup>(3)</sup>	t <sub>DON</sub>	V <sub>BAT</sub> =4.5V, R <sub>L</sub> =5Ω, C <sub>L</sub> =100μF, T <sub>A</sub> =25°C, Figure 18		1.7		ms
V <sub>OUT</sub> Rise Time <sup>(3)</sup>	t <sub>R</sub>			2.7		ms
Turn-On Time, SYS_WAKE to V <sub>OUT</sub>	t <sub>ON</sub>			4.4		ms
<b>Load Switch Turn-Off with Delay</b>						
Delay to Turn Off Load Switch	t <sub>SD</sub>	V <sub>BAT</sub> =4.5V, R <sub>L</sub> =150Ω, C <sub>L</sub> =100μF, T <sub>A</sub> =25°C, DSR= HIGH, Figure 17	5.8	7.3	8.8	s
V <sub>OUT</sub> Fall Time <sup>(3)</sup>	t <sub>F</sub>				10	ms
Turn-Off <sup>(4) (5)</sup>	t <sub>OFF</sub>				7.3	s
<b>Load Switch Zero-Second Turn-Off</b>						
Delay to Turn Off Load Switch	t <sub>SD</sub>	V <sub>BAT</sub> =4.5V, R <sub>L</sub> =150Ω, C <sub>L</sub> =100μF, T <sub>A</sub> =25°C, DSR= LOW, Figure 17		0.6		ms
V <sub>OUT</sub> Fall Time <sup>(3)</sup>	t <sub>F</sub>				10	ms
Turn-Off <sup>(4) (5)</sup>	t <sub>OFF</sub>				10.6	ms
<b>Zero-Second Factory Test Mode</b>						
Turn-On Time for V <sub>OUT</sub>	t <sub>VON</sub>	C <sub>L</sub> =5pF, R <sub>L</sub> =5kΩ, V <sub>OUT</sub> =OFF, DSR=LOW, Figure 19		2		ms
Timer Delay before Reset	t <sub>PHL1</sub>	C <sub>L</sub> =5pF, R <sub>L</sub> =5kΩ, V <sub>OUT</sub> =ON, DSR=LOW, Figure 20		1		ms

**Note:**

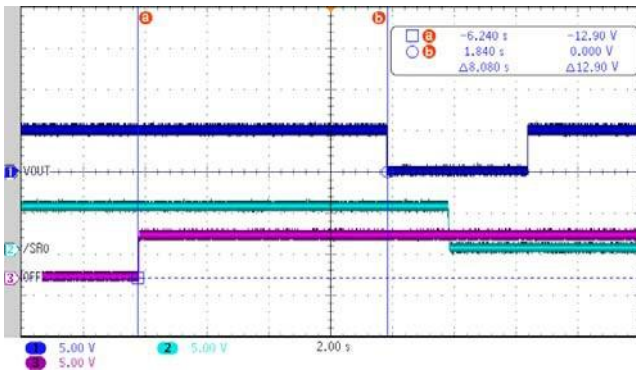
- (1) This parameter is guaranteed by design and characterization, RON is tested with different voltage and current conditions in production.
- (2) Input pins are /SR0, OFF, DSR, and SYS\_WAKE. Input pins should not be floated when VBAT is connected to the power supply.
- (3) t<sub>ON</sub>=t<sub>R</sub> + t<sub>DON</sub>.
- (4) t<sub>OFF</sub>=t<sub>F</sub> + t<sub>SD</sub>.
- (5) Output discharge enabled during off-state.

**Typical Characteristics (Ta=25°C, unless otherwise noted)**

**Figure 4. Off Supply Current vs. Temperature**

**Figure 5. Quiescent Current vs. Temperature**

**Figure 6. R<sub>ON</sub> vs. Temperature**

**Figure 7. t<sub>OFF</sub> vs. Temperature**

**Figure 8. t<sub>VON</sub> vs. Temperature**

**Figure 9. t<sub>PHL1</sub> vs. Temperature**

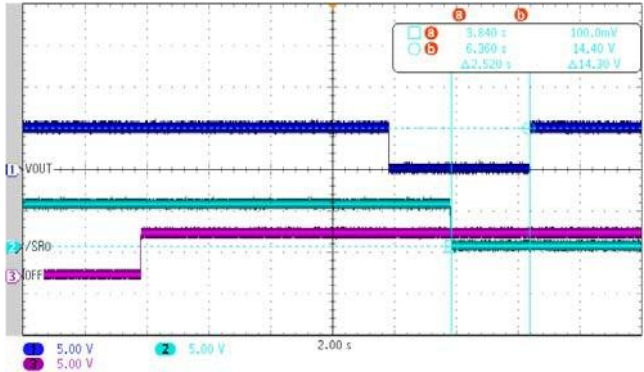


**Figure 10.  $t_{REC1}$  vs. Temperature**

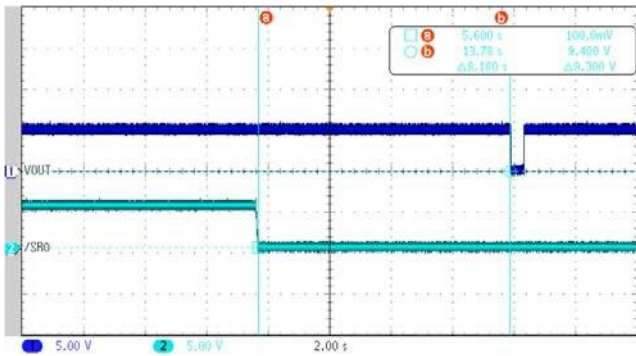



**Figure 11.  $t_{OFF}$** 

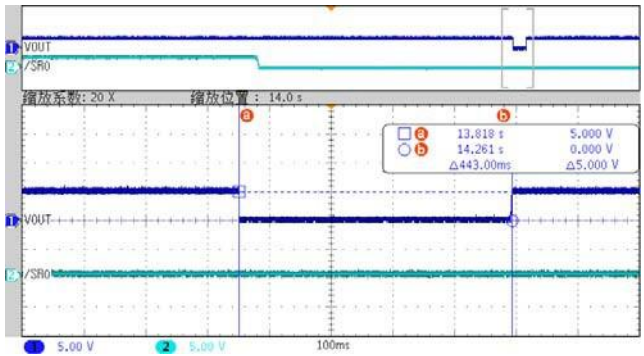
(/SR0=5V,Vbat=DSR=5V,OFF=SYS\_WAKE=GND)


**Figure 12.  $t_{VON}$** 

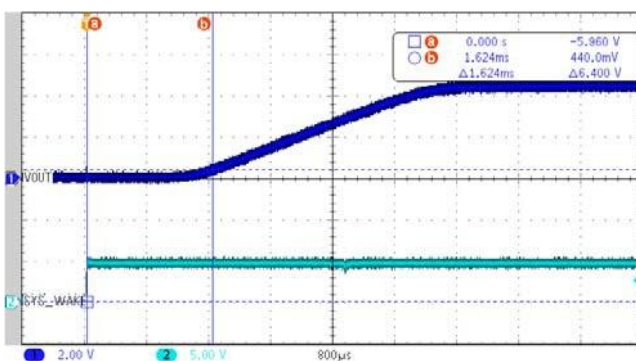
(/SR0=5V,Vbat=DSR=5V,OFF=SYS\_WAKE=GND)


**Figure 13.  $t_{PHL1}$** 

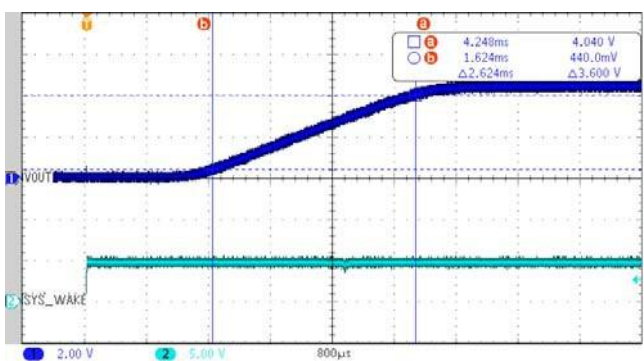
(/SR0=5V,Vbat=DSR=5V,OFF=SYS\_WAKE=GND)


**Figure 14.  $t_{REC1}$** 

(/SR0=5V,Vbat=DSR=5V,OFF=SYS\_WAKE=GND)


**Figure 15.  $t_{DON}$** 

(CI=100uF,RI=5ohm,Vbat=/SR0=DSR=4.5V,OFF=SYS\_WAKE=0V)


**Figure 16.  $t_R$** 

(CI=100uF,RI=5ohm,Vbat=/SR0=DSR=4.5V,OFF=SYS\_WAKE=0V)

## Application Information

### Reset Timer and Advanced Load Management

The WS4639 is both a reset IC and an advanced load management device. A typical application is shown in Figure 1.

#### Disconnect PMIC from Battery (Turn Off)

After holding the DSR pin HIGH, changing the OFF pin from LOW to HIGH (rising edge triggered) and holding it HIGH for at least 1ms, the WS4639 triggers an internal counter to allow a factory-customized 7.3s delay before turning off internal load switch. The delay is intended to allow the PMIC to complete a power-down sequence before safely disconnecting from the power supply. However, the turn-off sequence is terminated if a higher priority input is detected in  $t_{SD}$  period (see Resolving Input Conflicts).

Alternatively, after holding the DSR pin LOW, changing the OFF pin from LOW to HIGH (rising edge triggered) and holding it HIGH for at least 1ms, the WS4639 triggers the zero-second turn-off. Delay  $t_{SD}$  is significantly reduced to 0.6ms to avoid the default delay to turn-off load switch ( $t_{SD}$ ).

With its stringent shutdown current flow, the WS4639 significantly reduces the current drain on a battery when the PMIC is turned off. This preserves the battery power for a longer period when a mobile device is in Shutdown Mode.

#### Power On

There are two methods to turn on the load switch to wake up the PMIC. When a HIGH is inserted to the SYS\_WAKE pin or when /SR0 is held LOW for > 2.3s (see Figure 19), the WS4639 turns on its load switch to allow PMIC to connect to the battery. The reset feature is disabled when VOUT is toggled from OFF to ON. Continuously holding /SR0 LOW do not trigger a reset event. To enable

the reset feature, /SR0 must return to HIGH such that WS4639 resets its internal counter.

#### Reset Timer

During normal operation of a mobile device, if a reset operation is needed for mobile equipment holding the power switch, to which /SR0 is connected and is forced LOW, for at least 7.5s, causes the WS4639 to cut off the supply power to PMIC for 400ms by turning off the load switch. The WS4639 then automatically turns on the load switch to reconnect the PMIC to battery. This forces PMIC to enter a power-on sequence. If the power switch is released and /SR0 is returned to HIGH within 7.5s, the WS4639 resets its counter and VOUT remains in ON state, there is no change on VOUT and a reset does not occur.

#### Power-On Reset

When WS4639 is connected to a battery ( $V_{BAT} \geq 1.8V$ ), the part enters Power-On Reset (POR) Mode. All internal registers are reset and VOUT is ON at the end of POR sequence (see Table 2).

#### Zero-Second Factory Test Mode

WS4639 includes a Zero-Second Factory Test Mode to shorten the turn-on time for VOUT ( $t_{VON}$ ) and timer delay before reset ( $t_{PHL1}$ ) for factory testing. When VOUT is OFF, the default turn-on time ( $t_{VON}$ ) is 2.3s. If the DSR pin is LOW prior to /SR0 going LOW, the WS4639 bypasses the 2.3s delay and VOUT changes from OFF to ON immediately. Similarly, default reset delay ( $t_{PHL1}$ ) is 7.5s. If VOUT is ON and the DSR pin is LOW prior to /SR0 going LOW, the IC enters Zero-Second Factory Test Mode and bypasses the default reset delay of 7.5s, VOUT is pulled from ON to OFF immediately. The reset pulse ( $t_{REC1}$ ) remains at 400ms in Zero-Second Factory Test Mode. DSR should never be left floating during normal operation.

**Table 1. V<sub>OUT</sub> and Input Conditions**

Function	Initial Conditions (t=0 Second)				Associated Delay	V <sub>OUT</sub>	
	/SR0	SYS_WAKE	OFF	DSR		Before	After
Power-On	LOW	X	X	LOW	t <sub>VON</sub> <4ms	OFF	ON
	LOW	X	X	HIGH	t <sub>VON</sub> =2.3s	OFF	ON
	HIGH	HIGH	X	X	t <sub>ON</sub> =4.4ms	OFF	ON
Reset Function	LOW	X	X	LOW	t <sub>PHL1</sub> <1ms t <sub>REC1</sub> =400ms	ON	
	LOW	X	X	HIGH	t <sub>PHL1</sub> =7.5s <sup>(2)</sup> t <sub>REC1</sub> =400ms	ON	
Turn Off	HIGH	LOW	┐ <sup>(1)</sup>	LOW	t <sub>SD</sub> <1ms	ON	OFF
	HIGH	LOW		HIGH	t <sub>SD</sub> =7.3s	ON	OFF

**Note:**

(1) X=Don't Care, ┐ = Rising Edge, ┐┐ =HIGH to LOW to HIGH.

(2) Reset delay (t<sub>PHL1</sub>) is adjustable (see Table 4).

**Table 2. Pin Condition after POR**

Pin Name	/SR0	DSR	SYS_WAKE	OFF	V <sub>OUT</sub>
Default State (after POR)	1	1	0	0	ON

**Note:**

(1) 1=Input Logic HIGH, 0=Input Logic LOW, ON=load switch is ON state.

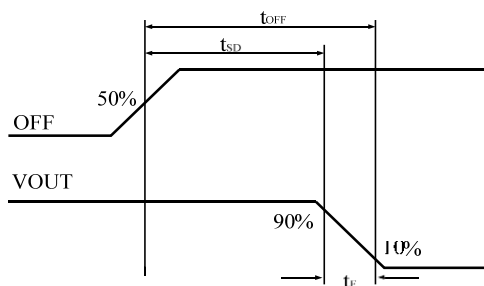
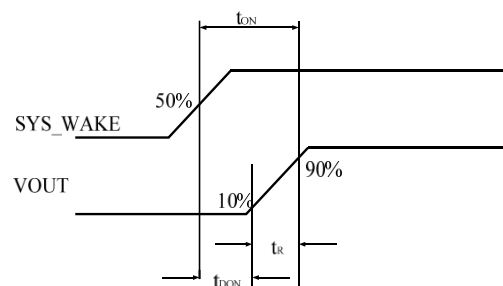
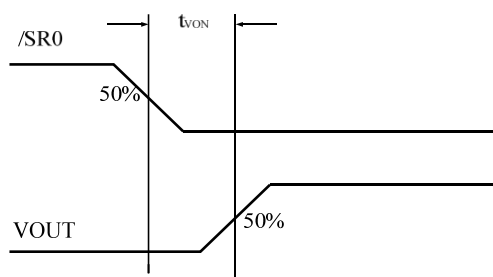
**Timing Diagrams**

 Figure 17. OFF vs. V<sub>OUT</sub>

 Figure 18. SYS\_WAKE vs. V<sub>OUT</sub>


Figure 19. /SR0 Power On

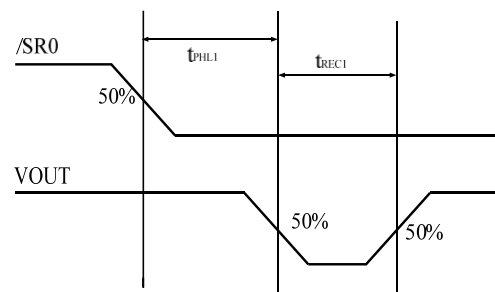


Figure 20. Reset Timing

## Resolving Input Conflicts

The WS4639 allows multiple simultaneous inputs and can resolve conflicts based on priority level (see Table 3). When two input pins are triggered at the same time, only the higher priority input is served and the lower priority input is ignored. The lower-priority signal must be repeated to be serviced.

**Table 3. Input Priority**

Input	Priority (1=Highest)
/SR0	1
SYS_WAKE	2
OFF	3

### Special Note on OFF Pin

In the  $t_{SD}$  period (DSR=HIGH only, see Figure 17), if /SR0 or SYS\_WAKE is triggered when  $0 < t < t_{SD}$ , the WS4639 exits the turn-off sequence and  $V_{OUT}$  remains in ON state. The higher priority input is served regardless of the condition of OFF pin.

To re-initiate the turn-off sequence, the OFF pins must return to LOW, and then toggle from LOW to HIGH again. The same input priority applies (Table 3) if DSR = HIGH.

### Special Note on SYS\_WAKE Pin

The SYS\_WAKE pin is designed and characterized to handle high voltage input at least 20V. Therefore, in application, a current-limiting resistor (i.e 100k $\Omega$ ) is required between SYS\_WAKE and the input signal regardless of input voltage.

### Adjustable Reset Delay with an External Resistor and DSR

The reset delay is adjustable by connecting a commonly available, low-power,  $\pm 5\%$ , RoHS-compliant resistor between the DELAY\_ADJ pin

and the GND pin (see Table 4). To disable the adjustable delay feature, DELAY\_ADJ should be tied to VBAT directly. The reset delay is factory programmed at 7.5s. The additional power consumption caused by using an external resistor is negligible. The external resistor is normally disconnected and is enabled for milliseconds when /SR0 is pulled LOW.

This external adjustment feature provides a simple alternate method for controlling delay time for engineering and production at customer's location. WILL can also factory program a wide range of turn-on times for  $V_{OUT}$  ( $t_{VON}$ ), timer delay before reset ( $t_{PHL1}$ ), reset timeout delay for  $V_{OUT}$  ( $t_{REC1}$ ), and load switch turn-off time ( $t_{OFF}$ ) to match customer applications. In this case, the external resistor ( $R_{ADJ}$ ) can be eliminated.

**Table 4. Delay Adjustment vs. External Resistor**

External Resistor $R_{ADJ}$ (k $\Omega$ )	Delay Multiplier	Adjusted Reset Delay $t_{PHL1\_ADJ}$ , (Seconds) $\pm 20\%$
Tie to GND (No Resistor)	$0.50 \times t_{PHL1}$	3.8
3.9	$0.75 \times t_{PHL1}$	5.6
10	$1.25 \times t_{PHL1}$	9.4
22	$1.50 \times t_{PHL1}$	11.3
47	$1.75 \times t_{PHL1}$	13.1
120	$2.00 \times t_{PHL1}$	15
Tie to VBAT (No Resistor)	$1.00 \times t_{PHL1}$	7.5

## Inside Load Switch Instruction

### Input Capacitor

The chip inside the reset timer doesn't require an input capacitor. To reduce device inrush current, a 0.1μF ceramic capacitor,  $C_{IN}$ , is recommended close to the  $V_{BAT}$  pin. A higher value of  $C_{IN}$  can be used to reduce the voltage drop experienced as the switch is turned on into a large capacitive load.

### Output Capacitor

While the load switch works without an output capacitor, if parasitic board inductance forces  $V_{OUT}$  below GND when switching off, a 0.1μF capacitor,  $C_{OUT}$ , should be placed between  $V_{OUT}$  and GND.

### Fall Time

Device output fall time can be calculated based on the RC constant of the external components, as:

$$T_F = R_L \times C_L \times 2.2 \quad (1)$$

Where  $t_F$  is 90% to 10% fall time,  $R_L$  is output load, and  $C_L$  is output capacitor.

The same equation works for a device with a pull-down output resistor.  $R_L$  is replaced by a parallel connected pull-down and an external output resistor combination, calculated as:

$$t_F = \frac{R_L \times R_{PD}}{R_L + R_{PD}} \times C_L \times 2.2 \quad (2)$$

Where  $t_F$  is 90% to 10% fall time,  $R_L$  is output load,  $R_{PD}=65\Omega$  is output pull-down resistor, and  $C_L$  is the output capacitor.

### Resistive Output Load

If resistive output load is missing, the chip without a pull-down output resistor does not discharge the output voltage. Output voltage drop depends, in that case, mainly on external device leaks.

## Application Specifics

At maximum operational voltage ( $V_{BAT}=5.5V$ ), device inrush current might be higher than expected. Spike current should be taken into account if  $V_{BAT}>5V$  and the output capacitor is much larger than the input capacitor. Input current  $I_{BAT}$  can be calculated as:

$$I_{BAT}(t) \approx \frac{V_{OUT}(t)}{R_{LOAD}} + (C_{LOAD} - C_{IN}) \frac{dV_{OUT}(t)}{dt} \quad (3)$$

Where switch and wire resistances are neglected and capacitors are assumed ideal.

Estimating  $V_{OUT}(t)=V_{BAT}/10$  and using experimental formula for slew rate ( $dV_{OUT}(t)/dt$ ), spike current can be written as:

$$\max(I_{BAT}) = \frac{V_{BAT}}{10R_{LOAD}} + (C_{LOAD} - C_{IN})(0.05V_{BAT} - 0.255) \quad (4)$$

Where supply voltage  $V_{BAT}$  is in volts, capacitances are in micro farads, and resistance is in ohms.

Example: If  $V_{BAT}=5.5V$ ,  $C_{LOAD}=100\mu F$ ,  $C_{IN}=10\mu F$ , and  $R_{LOAD}=50\Omega$ , calculate the spike current by:

$$\max(I_{BAT}) = \frac{5.5}{10 \times 50} + (100 - 10)(0.05 \times 5.5 - 0.2555) A = 1.8A$$

Maximum spike current is 1.8A, while average ramp-up current is:

$$I_{BAT}(t) \approx \frac{V_{OUT}(t)}{R_{LOAD}} + (C_{LOAD} - C_{IN}) \frac{dV_{BAT}(t)}{dt} \\ \approx 2.75 / 50 + 100 \times 0.0022 = 0.275A$$

### Output Discharge

The device contains a  $R_{PD}=65\Omega$  on-chip pull-down resistor for quick output discharge. The resistor is activated when the switch is turned off.



## Recommended Layout

For best thermal performance and minimal inductance and parasitic effects, keeping the input and output traces short and capacitors as close to the device as possible is recommended. Additional recommended layout considerations include:

- A1, A2, and A3 are interconnected at PCB, as close to the landing pad as possible.
- B1, B2, and B3 are interconnected at PCB, as close to the landing pad as possible.
- C1 (GND) is connected to GND plane of PCB.
- Reserve a pad for capacitor connection (C1) between  $V_{BAT}$  and GND, if no input capacitor is planned.
- Reserve a pad for capacitor connection (C2) between  $V_{OUT}$  and GND, if no output capacitor is planned.
- Use a dedicated  $V_{OUT}$  or  $V_{BAT}$  plane to improve thermal dissipation.

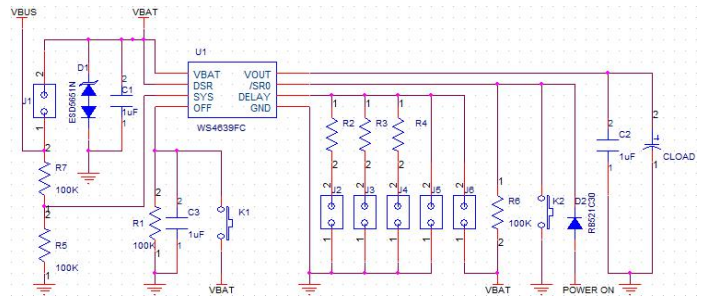


Figure 21. Demo Schematic

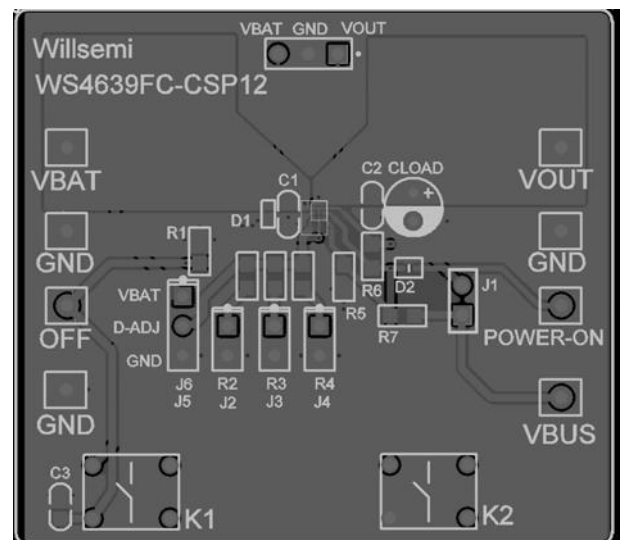


Figure 22. Demo Board Layout (TOP View)

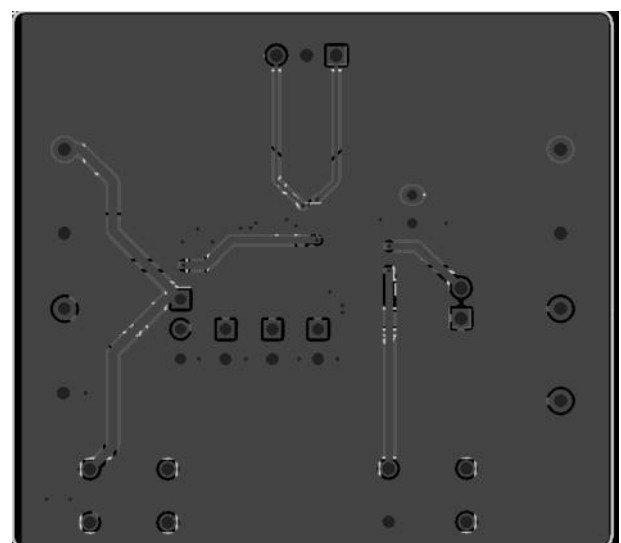
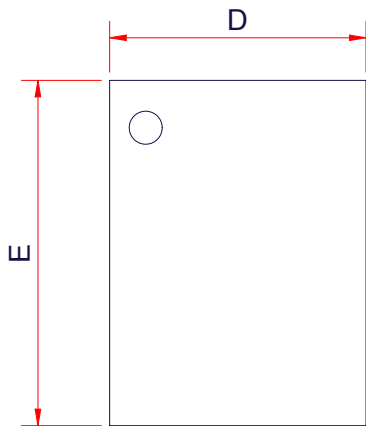
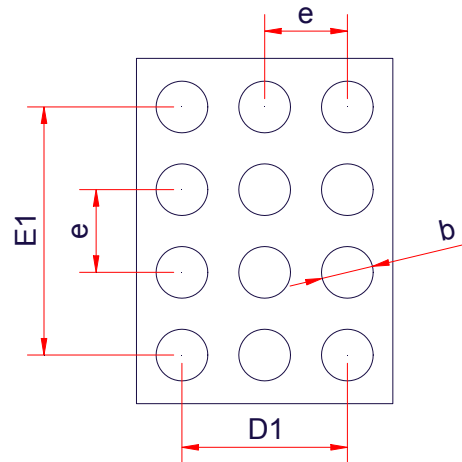
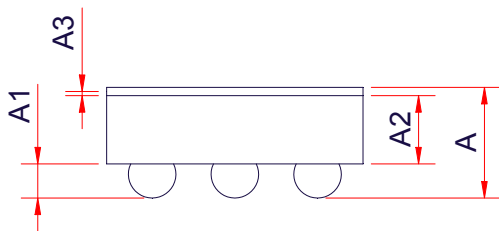
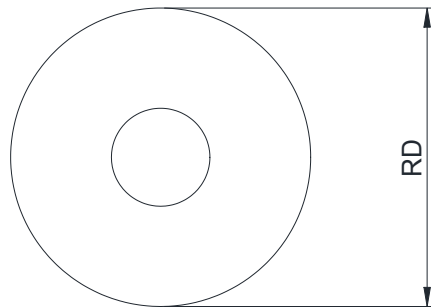
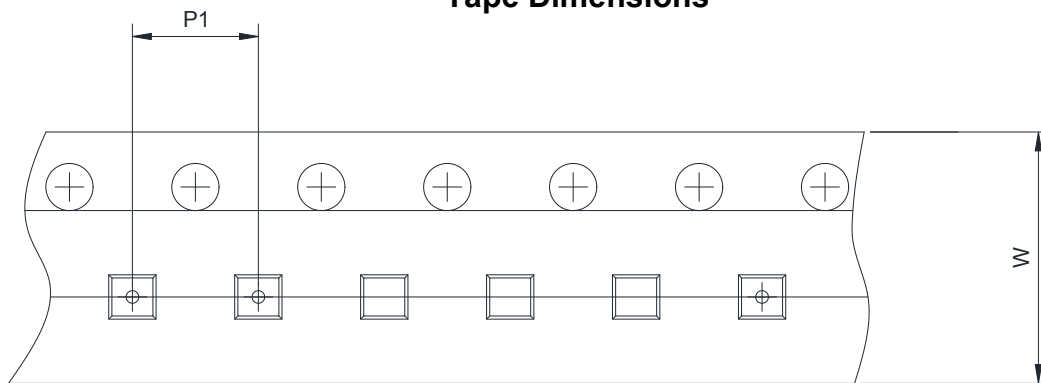
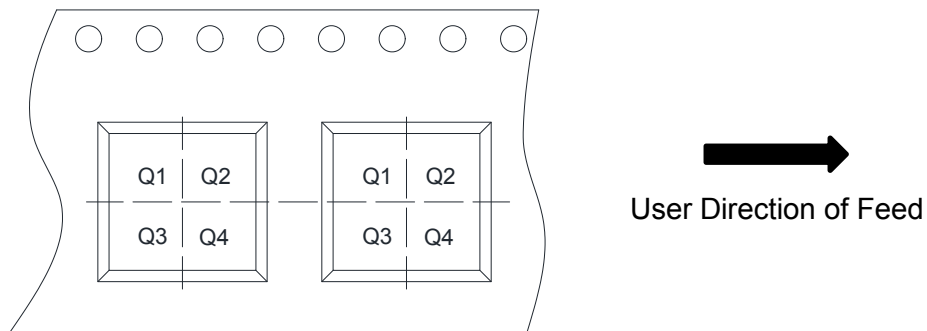


Figure 23. Demo Board Layout (Bottom View)

**PACKAGE OUTLINE DIMENSIONS**
**CSP-12L**

**TOP VIEW**

**BOTTOM VIEW**

**SIDE VIEW**

Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	0.54	0.60	0.65
A1	0.13	0.16	0.19
A2	0.38	0.41	0.44
A3	0.01	0.02	0.04
D	1.13	1.17	1.19
E	1.53	1.57	1.59
D1	0.75	0.80	0.85
E1	1.15	1.20	1.25
b	0.21	0.24	0.27
e	0.40 BSC		

**TAPE AND REEL INFORMATION**
**Reel Dimensions**

**Tape Dimensions**

**Quadrant Assignments For PIN1 Orientation In Tape**


RD	Reel Dimension	<input checked="" type="checkbox"/> 7inch	<input type="checkbox"/> 13inch		
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm	<input type="checkbox"/> 12mm		
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input checked="" type="checkbox"/> 4mm	<input type="checkbox"/> 8mm	
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2	<input type="checkbox"/> Q3	<input type="checkbox"/> Q4



## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for* [Power Switch ICs - Power Distribution](#) *category:*

*Click to view products by* [Will Semiconductor](#) *manufacturer:*

Other Similar products are found below :

[TLE6232GP](#) [NCP45520IMNTWG-L](#) [FPF1018](#) [DS1222](#) [BSP762TXT](#) [NCV380HMUAJAATBG](#) [TCK2065G,LF](#) [SZNCP3712ASNT3G](#)  
[NCP45520IMNTWG-H](#) [VND5004ATR-E](#) [ITS5215LXT](#) [AP22811BW5-7](#) [SLG5NT1437VTR](#) [SZNCP3712ASNT1G](#) [DML1008LDS-7](#)  
[KTS1640QGDV-TR](#) [KTS1641QGDV-TR](#) [NCV459MNWTBG](#) [NCP4545IMNTWG-L](#) [FPF2260ATMX](#) [SLG5NT1765V](#) [SLG5NT1757V](#)  
[NCP45780IMN24RTWG](#) [AP2151AMP-13](#) [NCP45540IMNTWG-L](#) [TPS2022P](#) [FPF2495BUCX](#) [NCP45650IMNTWG](#) [NCV8412ADDR2G](#)  
[DK5V100R20S](#) [JW7111SSOTB#TRPBF](#) [RY2121](#) [TPNTGD1100LT1G](#) [TPS27081ADDCR-TP](#) [FDC6331L-TP](#) [FDC6329L-TP](#) [FDC6323L-](#)  
[TP](#) [SI3865DDV](#) [TPS2116DRLR](#) [U3213](#) [BTS7020-2EPA](#) [BTT6100-2ERA](#) [BTS71220-4ESA](#) [RS2588CYF5](#) [RS2580XTDE8](#) [LP5308B6F](#)  
[ME1502AM5G](#) [SGM2576YN5G/TR](#) [DK5V100R15M](#) [SY6287CDEC](#)