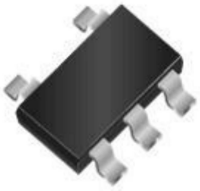
WS72631

9MHz Rail-to-Rail Input Output CMOS Operational Amplifiers

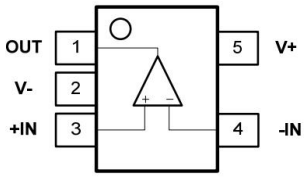
Http://www.omnivision-group.com

Descriptions

The WS72631 is a low power rail-to-rail input output operational amplifier featuring low current noise, high slew rate and wide signal bandwidth. The combination of low noise, low input bias currents, high speed and inside EMI filter make this amplifier useful in a wide variety of applications. Filters, integrators, photo-diode amplifiers, and high impedance sensors all benefit from this combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion of this device. Applications for this amplifier include power amplifier (PA) controls, laser diode control loops, portable and loop-powered instrumentation, audio amplification for portable devices, and ASIC input and output amplifiers. The WS72631 is dual channel version available in SOT23-5L package.



SOT23-5L



SOT23-5L
Pin configuration (Top view)

SOT23-5L

Marking

2631 = Device code
GE = Special code
Y = Year code
W = Week code

Applications

- Sensor Signal Conditioning
- Consumer Audio
- Multi-Pole Active Filters
- Communications
- Security
- Scanners

Features

- Gain-bandwidth Product : 9 MHz
- Low Noise : 12.5 nV/ √ Hz(f= 1kHz)
- Slew Rate : 5 V/μs
- Offset Voltage : 2.5 mV (max)
- Supply Range : 2.2 V to 5.5 V
- Supply Current : 720 uA/ch
- High Output Current : 130 mA
- Low THD+N : -100dB
- Rail-to-Rail Input/Output Swing
- －40˚C to 125˚C Operation Range
- Robust 8kV HBM and 400V MM and 2kV CDM

Order Information

Device	Package	Shipping
WS72631E-5/TR	SOT23-5L	3000/Reel &Tape

Pin Descriptions

Pin Number	Symbol	Descriptions
1	Out	Output
2	-Vs	Negative supply
3	+In	Non-inverting input
4	-In	Inverting input
5	+Vs	Positive supply

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage, ([V+] – [V-])	V_S(2)	6	V
Input Differential Voltage	V_{IDR}(3)	±6	V
Input Common Mode Voltage Range	V_{ICR}	(V-)-0.2 to (V+)+0.2	V
Output Short-Circuit Duration	t_{SO}	Unlimited	/
Operating Fee-Air Temperature Range	T_A	-40 to 125	˚C
Storage Temperature Range	T_{STG}	-65 to 150	˚C
Junction Temperature Range	T_J	150	˚C
Lead Temperature Range	T_L	260	˚C

Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values, except differential voltage are with respect to network terminal.
3. Differential voltages are at +IN with respect to -IN.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8 JEDEC-EIA/JESD22-A114A	±8000	V
MM	Machine Model ESD	JEDEC-EIA/JESD22-A115	±400	V
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	±2000	V

Electronics Characteristics

The *denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_S = 5V, V_{CM} = V_{OUT} = V_S/2, R_{load} = 100kΩ, C_{load} =100pF.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{OS}	Input Offset Voltage	V_{CM}= V_S/2	-2.5	±0.1	+2.5	mV
α_{VOS}	Input Offset Voltage Drift	-40°C to 125°C		2		μV/°C
I_{IB}	Input Bias Current			10		pA
I_{OS}	Input Offset Current			10		pA
V_n	Input Voltage Noise	f=0.1Hz to10Hz		0.9		μV_{P-P}
e_n	Input Voltage Noise Density	f=1kHz		12.5		nV/√Hz
CMRR	Common Mode Rejection Ratio	V_{CM}=1V to 3V	65	80		dB
V_{CM}	Common Mode Input Voltage Range		(V-)-0.1		(V+)+0.1	V
PSRR	Power Supply Rejection Ratio	V_S = 2.2V to 5.5V, V_{CM} = 0V	70	96		dB
A_{VOL}	Open Loop Large Signal Gain	V_{OUT} = -2V to 2V, R_{load} = 2kΩ	90	100		dB
V_{OH}	High Level Output Voltage	R_{load}=2kΩ		13		mV
		R_{load}=10kΩ		2		mV
V_{OL}	Low Level Output Voltage	R_{load}=2kΩ		8		mV
		R_{load}=10kΩ		2		mV
R_{OUT}	Closed-Loop Output Impedance	G = 1, f =1MHz, I_{OUT} = 0		0.5		Ω
I_{SC}	Output Short-Circuit Current	Source Current		130		mA
		Sink Current		130		mA
V_S	Supply Voltage		2.2		5.5	V
I_Q	Quiescent Current per Amplifier	Vs=5V		720	870	uA
PM	Phase Margin	R_{load}=1kΩ, C_{load}=60pF		60		degrees
GM	Gain Margin	R_{load}=1kΩ, C_{load}=60pF		10		dB
GBWP	Gain-Bandwidth Product	f=1kHz		9		MHz
t_S	0.1% Settling Time	1.5 to 3.5V, Unity Gain		1.6		μs
SR	Slew Rate	A_V=1, R_{load}=2kΩ, C_{load}=100pF		5		V/μs
FPBW	Full Power Bandwidth	$2V_{P-P}$		320		kHz
THD+N	Total Harmonic Distortion and Noise	f=1kHz, AV=1, R_{load}=2kΩ, V_{OUT}=$1V_{PP}$		-100		dB
X_{talk}	Channel Separation	f = 1kHz, RL = 2kΩ		110		dB

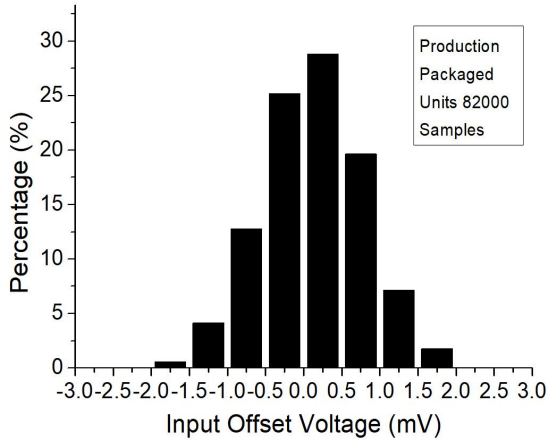
Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
2. A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.
3. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.
4. Full power bandwidth is calculated from the slew rate FPBW = SR/($\pi \bullet V_{P-P}$).

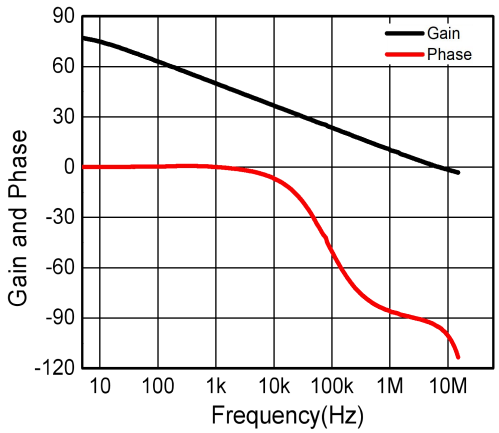
Typical Characteristics

T_A=25°C, V_S=±2.5V, V_{CM}=0V, unless otherwise noted.

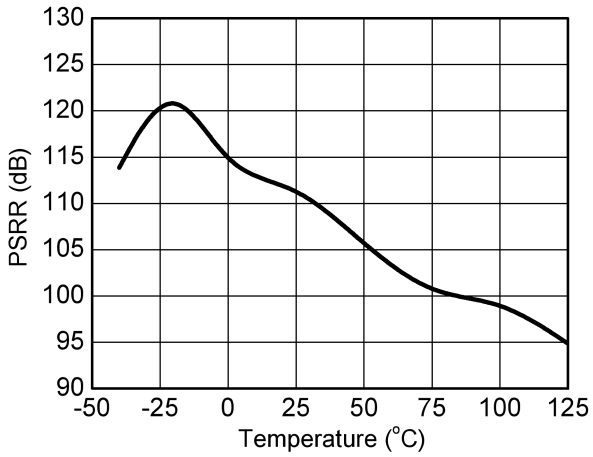
Offset Voltage Production Distribution



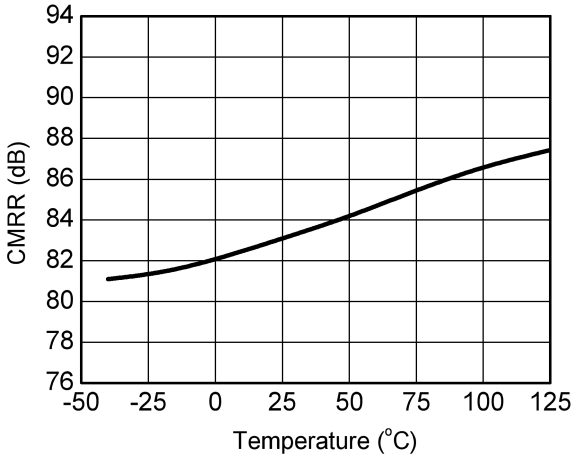
Open-Loop Gain and Phase



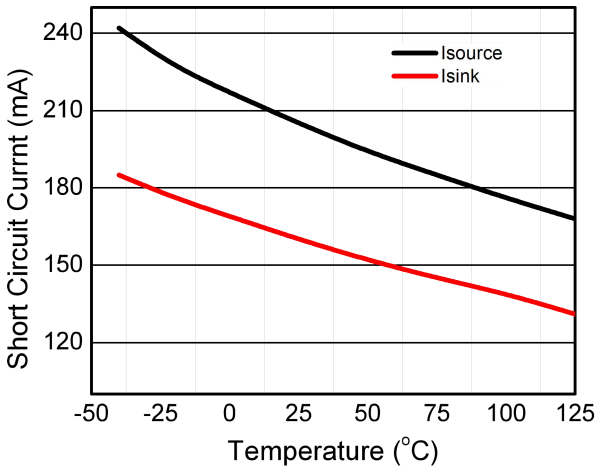
Power-Supply Rejection Ratio vs. Temperature



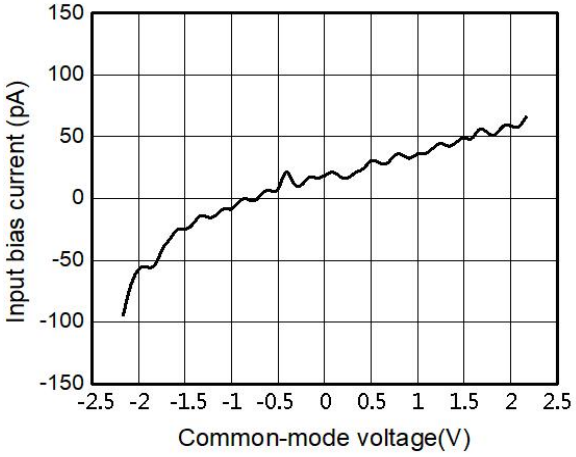
CMRR vs. Temperature



Short Circuit Current vs. Temperature



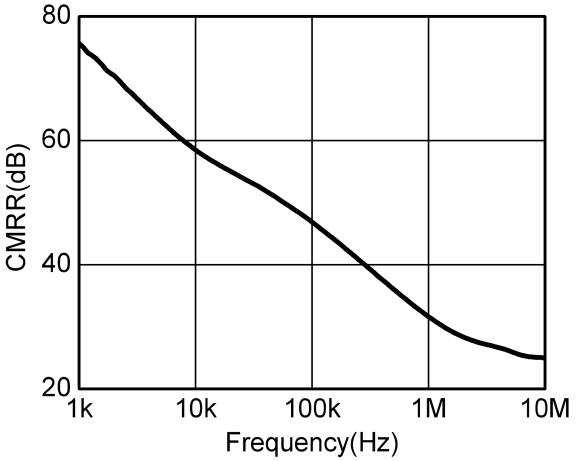
Input Bias Current vs. Input Common Mode Voltage



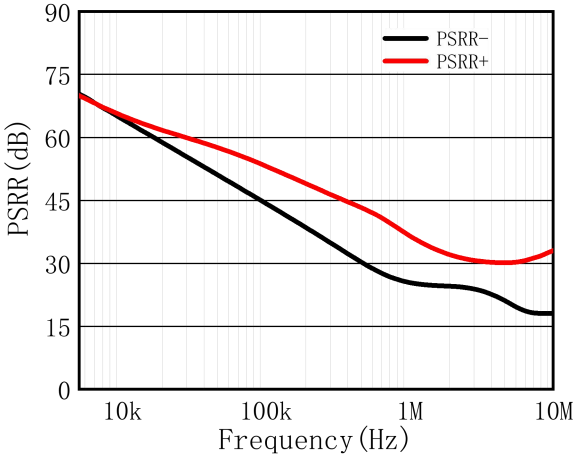
Typical Characteristics (continued)

T_A=25°C, V_S=±2.5V, V_{CM}=0V, unless otherwise noted

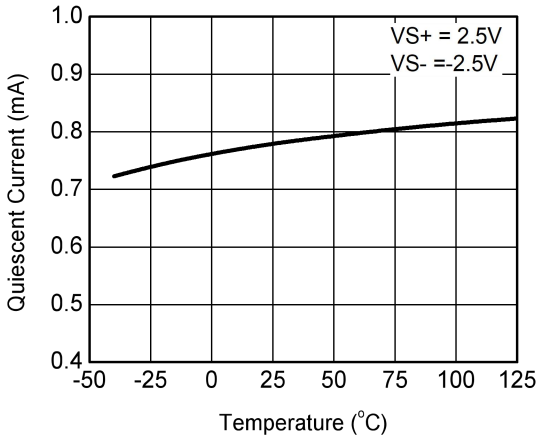
CMRR vs. Frequency



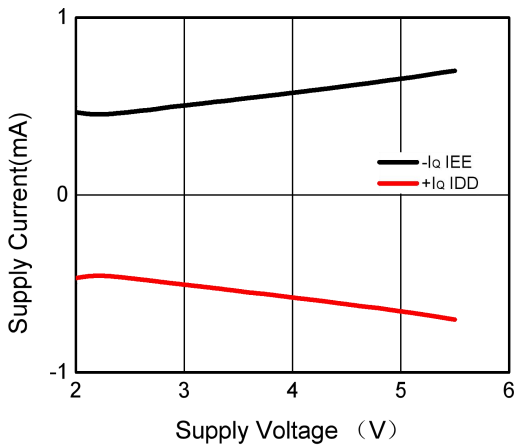
Power-Supply Rejection Ratio vs. Frequency



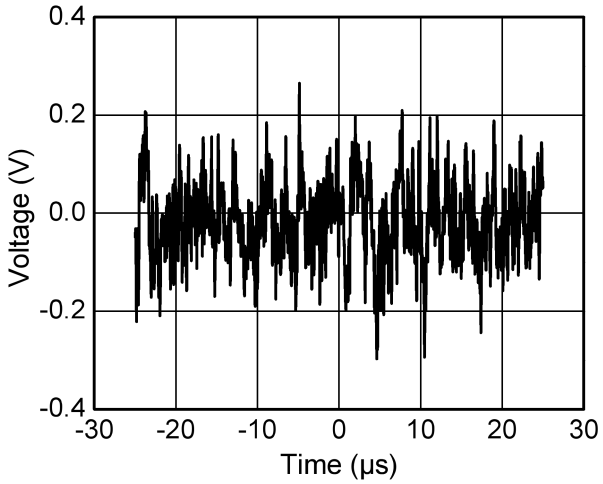
Quiescent Current vs. Temperature



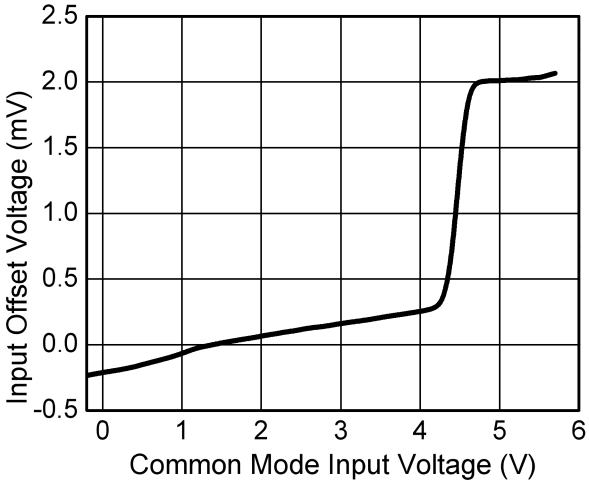
Quiescent Current vs. Supply Voltage



0.1 Hz TO 10 Hz Input Voltage Noise



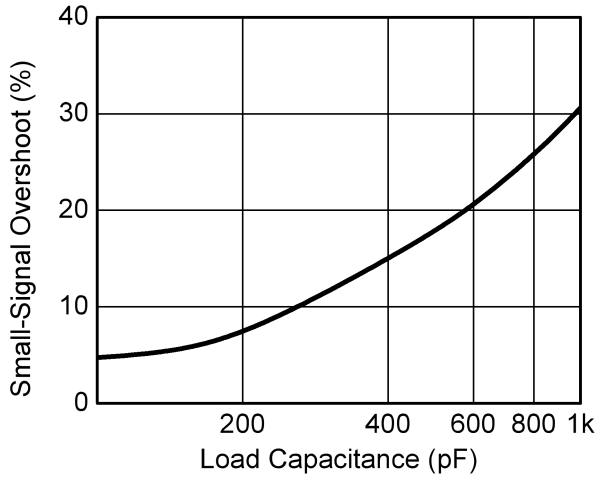
Offset Voltage vs Common-Mode Voltage



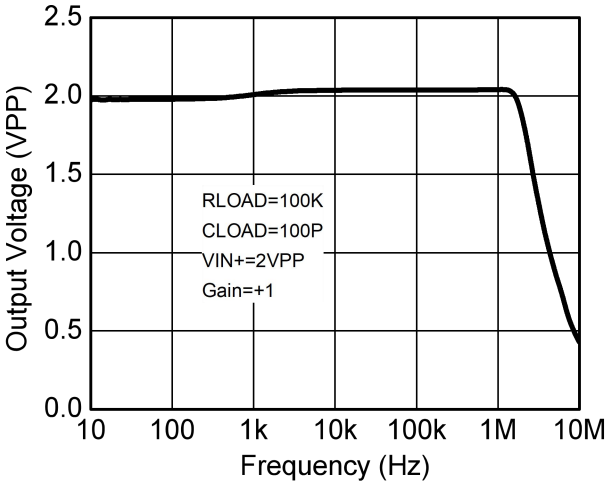
Typical Characteristics (continued)

T_A=25°C, V_S=±2.5V, V_{CM}=0V, unless otherwise noted

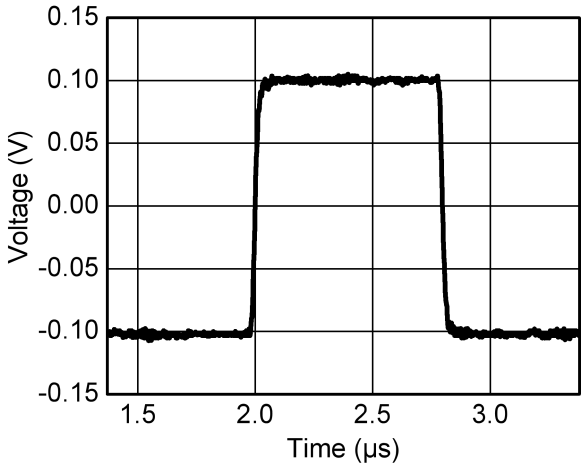
Small-Signal Overshoot vs. Load Capacitance



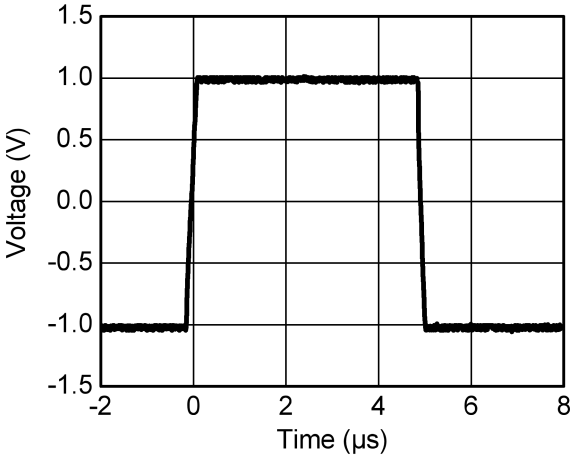
Closed-Loop Output Voltage Swing



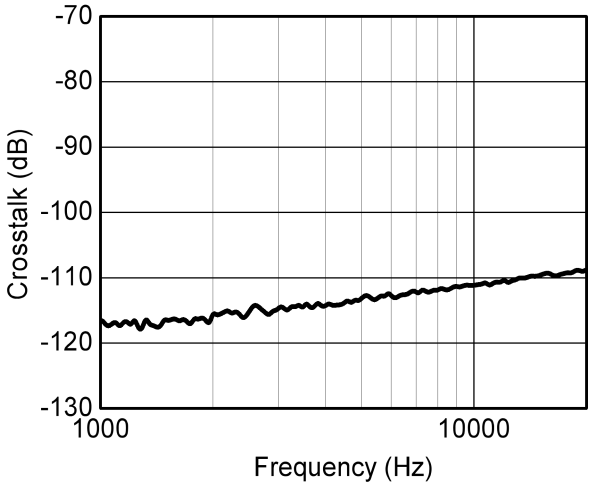
Small-Signal Step Response, 100mV Step



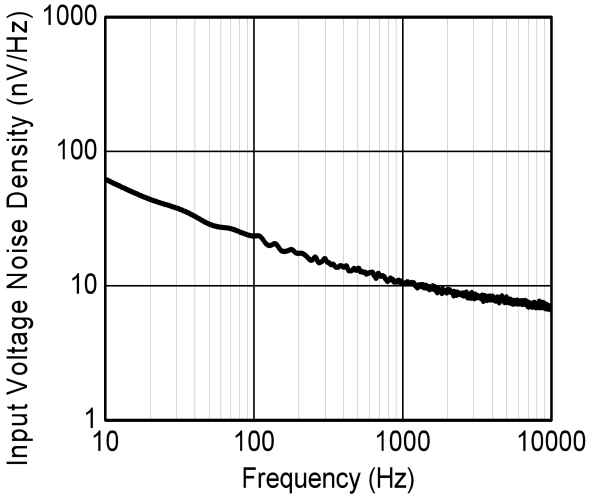
Large-Scale Step Response, 2V Step



Crosstalk



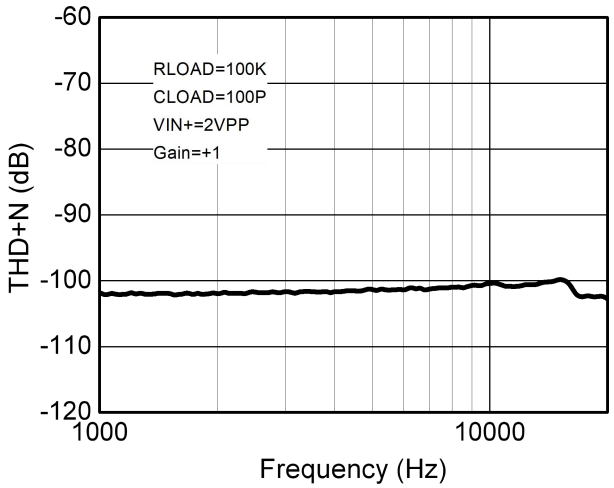
Noise Density



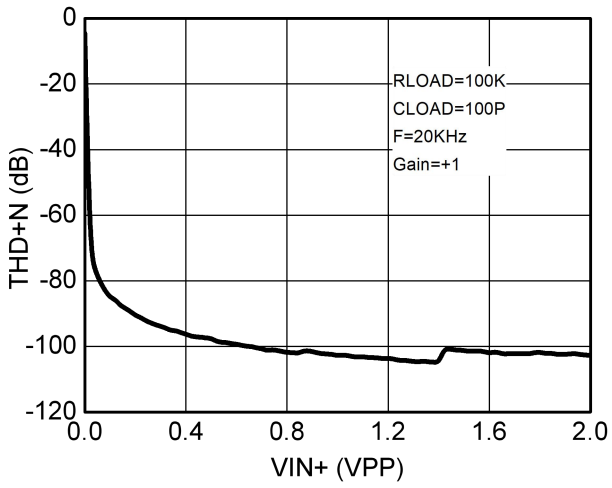
Typical Characteristics (continued)

T_A=25°C, V_S=±2.5V, V_{CM}=0V, unless otherwise noted

THD+N vs freq



THD+N vs Vin



Operation

The WS72631 series op amps can operate on a single-supply voltage (2.2 V to 5.5 V), or a split-supply voltage (±1.1 V to ±2.75 V), making them highly versatile and easy to use. The power-supply pins should have local bypass ceramic capacitors (typically 0.001 μF to 0.1 μF). These amplifiers are fully specified from +2.2 V to +5.5 V and over the extended temperature range of –40°C to +125°C. Parameters that can exhibit variance with regard to operating voltage or temperature are presented in the Typical Characteristics.

Input ESD Diode Protection

The WS72631 incorporates internal electrostatic discharge (ESD) protection circuits on all pins. In the case of input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes also provide in-circuit input overdrive protection, as long as the current is limited to 10 mA as stated in the Absolute Maximum Ratings table. Many input signals are inherently current-limited to less than 10 mA; therefore, a limiting resistor is not required. Figure 1 shows how a series input resistor (RS) may be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value should be kept to the minimum in noise-sensitive applications.

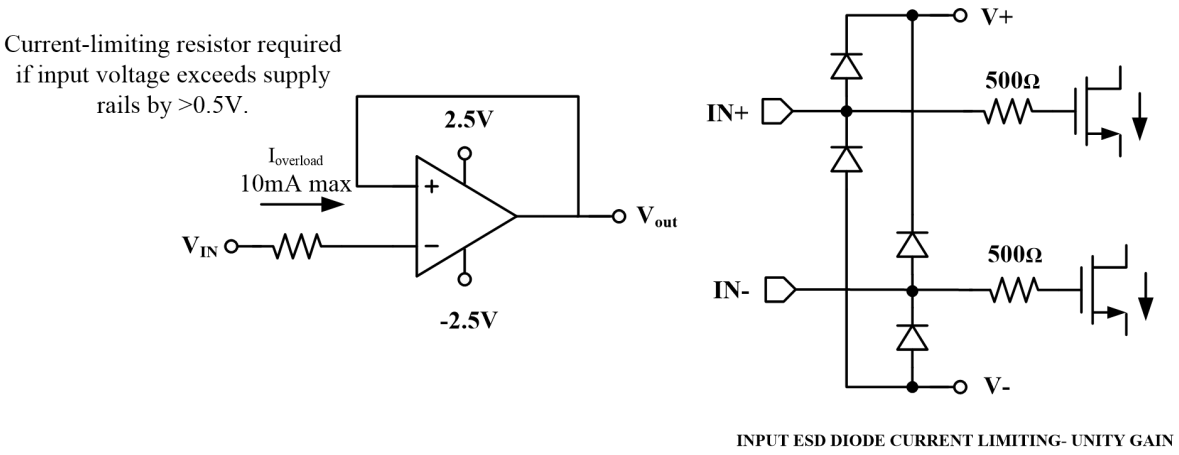


Figure1. Input ESD Diode

PCB Surface Leakage

In applications where low input bias current is critical, Printed Circuit Board (PCB) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is 1012Ω. A 5V difference would cause 5pA of current to flow, which is greater than the WS72631 OPA's input bias current at +27° C (±3pA, typical). It is recommended to use multi-layer PCB layout and route the OPA's -IN and +IN signal under the PCB surface.

The effective way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 1 for Inverting Gain application.

1. For Non-Inverting Gain and Unity-Gain Buffer:

a) Connect the non-inverting pin (VIN+) to the input with a wire that does not touch the PCB surface.

b) Connect the guard ring to the inverting input pin (VIN–). This biases the guard ring to the Common Mode input voltage.

2. For Inverting Gain and Trans-impedance Gain Amplifiers (convert current to voltage, such as photo detectors):

a) Connect the guard ring to the non-inverting input pin (VIN+). This biases the guard ring to the same reference voltage as the op-amp (e.g., VDD/2 or ground).

b) Connect the inverting pin (VIN–) to the input with a wire that does not touch the PCB surface.

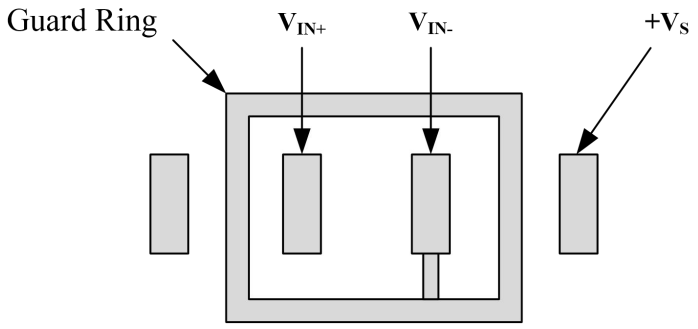


Figure 2 The Layout of Guard Ring

Power Supply Layout and Bypass

The WS72631 OPA's power supply pin (VDD for single-supply) should have a local bypass capacitor (i.e., 0.01μF to 0.1μF) within 2mm for good high frequency performance. It can also use a bulk capacitor (i.e., 1μF or larger) within 100mm to provide large, slow currents. This bulk capacitor can be shared with other analog parts.

Ground layout improves performance by decreasing the amount of stray capacitance and noise at the OPA's inputs and outputs. To decrease stray capacitance, minimize PC board lengths and resistor leads, and place external components as close to the op amps' pins as possible.

Proper Board Layout

To ensure optimum performance at the PCB level, care must be taken in the design of the board layout. To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at least 5mm from supply lines to minimize coupling.

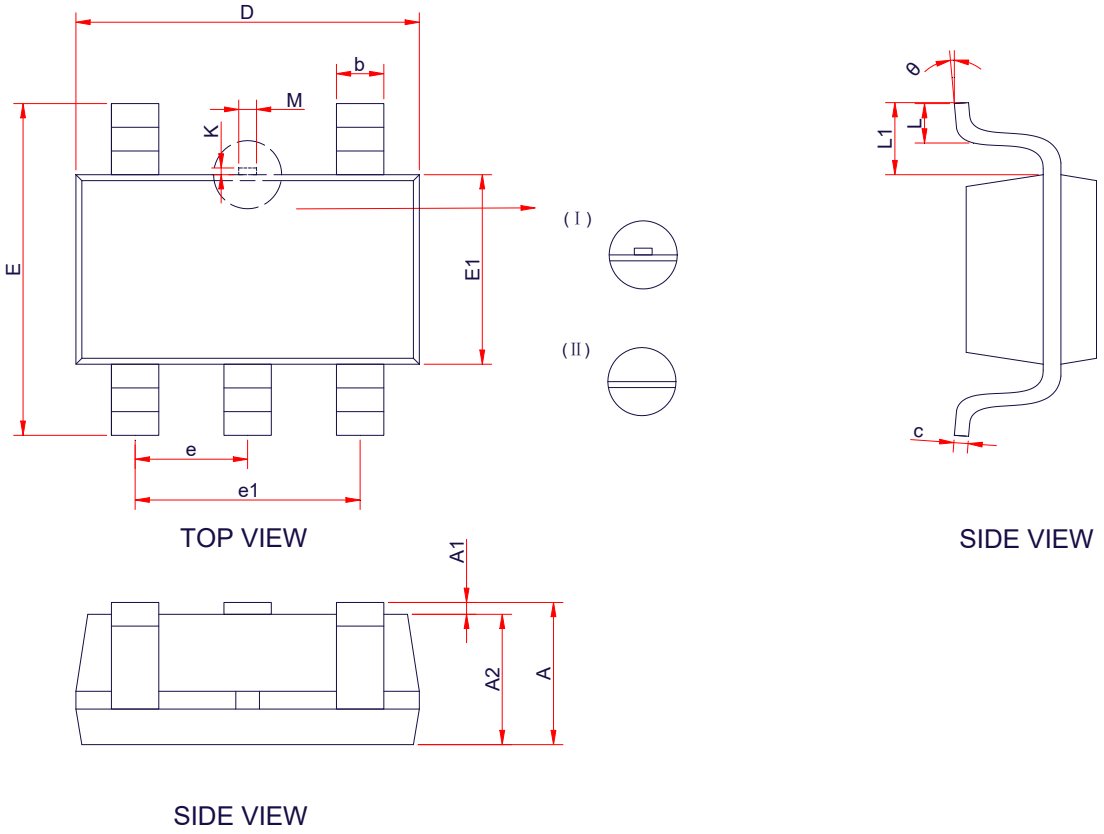
A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so heat sources warm both ends equally. Input signal paths should

contain matching numbers and types of components, where possible to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Ensure leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

PACKAGE OUTLINE DIMENSIONS

SOT-23-5L

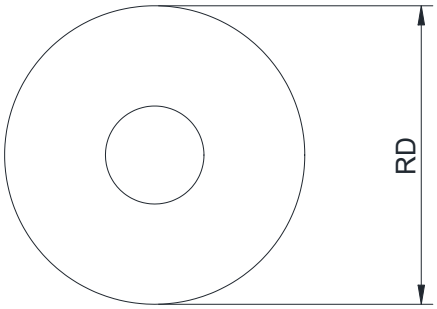


Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	-	-	1.45
A1	0.00	-	0.15
A2	0.90	1.10	1.30
b	0.30	0.40	0.50
c	0.10	-	0.21
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
M	0.10	0.15	0.25
K	0.00	-	0.25
θ	0°	-	8°

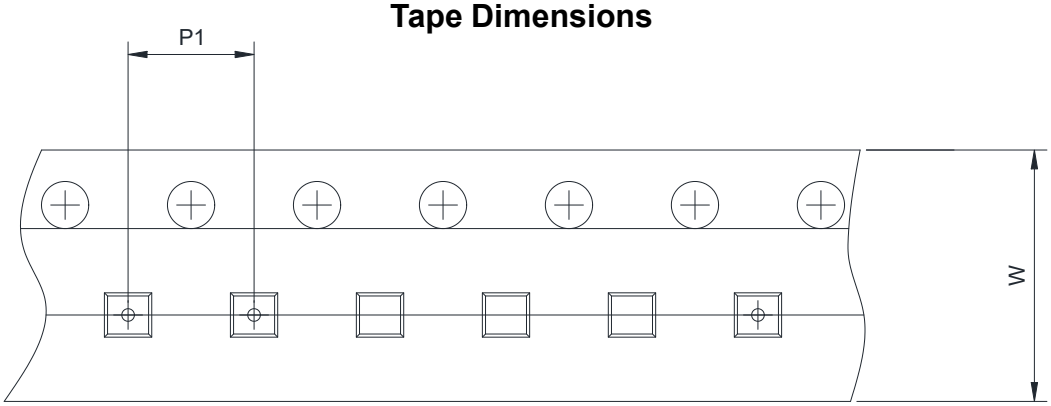
TAPE AND REEL INFORMATION

SOT-23-5L

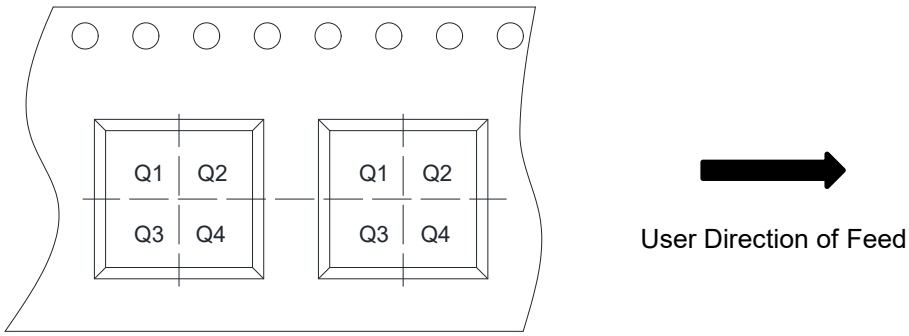
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch	☐ 13inch		
W	Overall width of the carrier tape	☑ 8mm	☐ 12mm	☐ 16mm	
P1	Pitch between successive cavity centers	☐ 2mm	☑ 4mm	☐ 8mm	
Pin1	Pin1 Quadrant	☐ Q1	☐ Q2	☑ Q3	☐ Q4

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