

## WS742128D

### Capless 2Vrms to 3Vrms Audio Driver with Adjustable Gain

#### Descriptions

The WS742128D is an integrated solution for Set-top box and high definition player, and designed to optimize the audio driver circuit performance while reducing the BOM cost by eliminating the peripheral discrete components for noise reduction. WS742128D features a 3Vrms stereo audio driver that designed to allow for the removal of output AC-coupling capacitors. Featuring single-ended input mode, gain range of  $\pm 1V/V$  to  $\pm 10V/V$  can be achieved via external gain resistor setting. The WS742128D is able to offer 3Vrms output at 600 $\Omega$  load with 5V supply. Meanwhile, the WS742128D offers built-in shut-down control circuitry for optimal pop-free performance. Under under-voltage condition, WS742128D is able to detect it and mutes the output. WS742128D satisfies MSL3 level requirements.

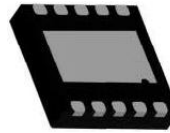
#### Applications

- Set-Top Boxes
- High Definition DVD Players
- Car Entertainment System
- Medical

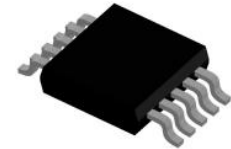
#### Features

- Single Supply Voltage : 3.0V~5.5V
- THD+N : >100dB
- SNR : >112dB
- -40°C to 85°C Operation Range
- Voltage Output at 600 $\Omega$  Load  
2Vrms with 3.3V supply voltage  
3Vrms with 5.0V supply voltage
- No Pop/Clicks Noise when Power ON/OFF
- No Need Output DC-Blocking Capacitors
- Optimized Frequency Response between 20Hz~20kHz
- Accepting Differential Input
- Featuring external under voltage mute
- Ultra Low noise and THD

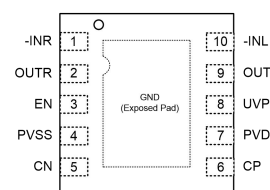
[Http://www.omnivision-group.com](http://www.omnivision-group.com)



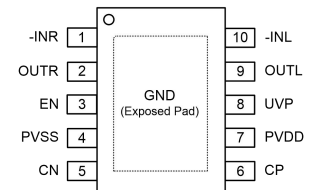
DFN2x2-10  
DFN3x3-10



EMSOP-10L

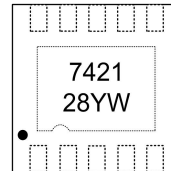


DFN2x2-10  
DFN3x3-10

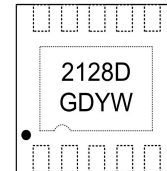


EMSOP-10L

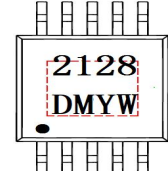
Pin configuration (Top view)



DFN2x2-10



DFN3x3-10



EMSOP-10L

#### Marking

742128, 2128, 2128D = Device code  
DM, GD = Special code  
Y = Year code  
W = Week code

#### Order Information

Device	Package	Shipping
WS742128DD-10/TR	DFN2x2-10	3000/Reel &Tape
WS742128DDA-10/TR	DFN3x3-10	3000/Reel &Tape
WS742128DM-10/TR	EMSOP-10L	4000/Reel &Tape

## Pin Descriptions

Pin Number	Symbol	Descriptions
1	-INR	Right-channel negative input
2	OUTR	Right-channel output
3	EN	Enable input, active-high
4	PVSS	Supply voltage
5	CN	Charge-pump flying capacitor negative
6	CP	Charge-pump flying capacitor positive
7	PVDD	Positive supply
8	UVP	Under voltage protection input
9	OUTL	Left-channel output
10	-INL	Left-channel negative input
EP	GND	Power ground

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	$V_{DD}^{(2)}$	6	V
Input Differential Voltage	$V_{IDR}^{(3)}$	$\pm 6$	V
Input Common Mode Voltage Range	$V_{ICR}$	$(V^-)-0.2$ to $(V^+)+0.2$	V
Output Short-Circuit Duration	$t_{SO}$	Unlimited	/
Operating Free-Air Temperature Range	$T_A$	-40 to 85	$^{\circ}C$
Storage Temperature Range	$T_{STG}$	-65 to 150	$^{\circ}C$
Junction Temperature Range	$T_J$	150	$^{\circ}C$
Lead Temperature Range	$T_L$	260	$^{\circ}C$
MSOP-10 $\theta_{JA}$		190	$^{\circ}C/W$

### Note:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are only stress ratings, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- All voltage values, except differential voltage are with respect to network terminal.
- Differential voltages are at IN+ with respect to IN-.

## ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum level	Unit
HBM	Human Body Model ESD	MIL-STD-883H Method 3015.8 JEDEC-EIA/JESD22-A114A	4	kV
MM	Machine Model ESD	JEDEC-EIA/JESD22-A115	200	V
CDM	Charged Device Model ESD	JEDEC-EIA/JESD22-C101E	2	kV

**Electronics Characteristics**

The \*denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = 5\text{V}$ ,  $R_L = 25\text{k}\Omega$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	
$V_{DD}$	Supply Voltage		*	3	5	5.5	V
$V_{IH}$	EN High level input voltage			1.1			V
$V_{IL}$	EN Low level input voltage				0.4		V
$T_A$	Operating Temperature Range		*	-40		85	$^\circ\text{C}$
$V_{OS}$	Output Offset Voltage	$V_{DD}=3\text{V}$ to $5\text{V}$ , input grounded, unity gain.	*	-3.5	0.6	3.5	mV
OVP	$V_{DD}$ Over Voltage Protection	$V_{DD}>5.5\text{V}$ then device shutdown.			5.75		V
PSRR	Power Supply Rejection Ratio			90			dB
$V_{OH}$	High Level Output Voltage	$V_{DD}=5\text{V}$ $R_L=2.5\text{k}\Omega$		4.92			V
		$V_{DD}=3.3\text{V}$ $R_L=2.5\text{k}\Omega$		3.15			V
$V_{OL}$	Low Level Output Voltage	$V_{DD}=5\text{V}$ $R_L=2.5\text{k}\Omega$		-4.65			V
		$V_{DD}=3.3\text{V}$ $R_L=2.5\text{k}\Omega$				-3	V
$I_{IH}$	EN High level input current	$V_{DD}=5\text{V}$ $V_i=V_{DD}$	*			1	$\mu\text{A}$
$I_{IL}$	EN Low level input current	$V_{DD}=5\text{V}$ $V_i=0$	*			1	$\mu\text{A}$
$I_{DD}$	Quiescent Current	$V_{DD}=3.3\text{V}$ $V_i=V_{DD}$		10.8			mA
		$V_{DD}=5\text{V}$ $V_i=V_{DD}$		12.8			
		Shut down mode $V_{DD} = 3-5\text{V}$				0.15	
$V_o$	Output Voltage	THD=1%, $V_{DD}=3.3\text{V}$ $f=1\text{kHz}$		2.05			$V_{rms}$
THD+N	Total Harmonic Distortion and Noise	$V_o=2V_{rms}$ $f=1\text{kHz}$ $R_L=600\Omega$ , $V_{DD}=3.3\text{V}$			0.001		%
$X_{TALK}$	Channel cross talk	$V_o=2V_{rms}$ $f=1\text{kHz}$ , $V_{DD}=3.3\text{V}$			100		dB
$I_o$	Maximum output current	$V_{DD}=3.3\text{V}$			40		mA
SNR	Signal noise ratio	$V_o=2V_{rms}$ BW=22kHz A-weighted and $V_{DD}=3.3\text{V}$			110		dB
SR	Slew Rate				17		$\text{V}/\mu\text{s}$
$V_N$	Noise output voltage	BW=20Hz to 22kHz, $V_{DD}=3.3\text{V}$			5.1		$\mu\text{V}_{rms}$
$G_{BW}$	Gain-Bandwidth Product	$V_{DD}=3.3\text{V}$			6.5		MHz
$A_{VO}$	Open Loop Large Signal Gain	$V_{DD}=3.3\text{V}$			100		dB
$V_{UVP}$	External under-voltage detection	$V_{DD}=3.3\text{V}$		1.14	1.21	1.31	V
$I_{HYS}$	External under-voltage detection hysteresis current	$V_{DD}=3.3\text{V}$			4.7		$\mu\text{A}$
$f_{CP}$	Charge pump frequency	$V_{DD}=3.3\text{V}$			490		kHz

## Electronics Characteristics (continued)

The \*denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = 5\text{V}$ ,  $R_L = 25\text{k}\Omega$

Attenuation@mute	Input-to-output attenuation in shutdown	EN=0V, $V_{DD}=3.3\text{V}$			90		dB
$V_o$	Output Voltage	THD=1%, $V_{DD}=5\text{V}$ f=1kHz		3.05			$V_{\text{rms}}$
THD+N	Total Harmonic Distortion and Noise	$V_o=2V_{\text{rms}}$ , f=1kHz $R_L=600\Omega$ , $V_{DD}=5\text{V}$			0.001		%
$X_{\text{TALK}}$	Channel cross talk	$V_o=2V_{\text{rms}}$ , f=1kHz, $V_{DD}=5\text{V}$			95		dB
$I_o$	Maximum output current	$V_{DD}=5\text{V}$			60		mA
SNR	Signal noise ratio	$V_o=2V_{\text{rms}}$ , BW=22kHz A-weighted $V_{DD}=5\text{V}$			112		dB
SR	Slew Rate				17		V/ $\mu\text{s}$
$V_N$	Noise output voltage	BW=20Hz to 22kHz, $V_{DD}=5\text{V}$			4.5		$\mu\text{V}_{\text{rms}}$
$G_{\text{BW}}$	Gain-Bandwidth Product	$V_{DD}=5\text{V}$			6.5		MHz
$A_{\text{VO}}$	Open Loop Large Signal Gain	$V_{DD}=5\text{V}$			110		dB
$V_{\text{UVP}}$	External under-voltage detection	$V_{DD}=5\text{V}$	1.14	1.21	1.31		V
$I_{\text{HYS}}$	External under-voltage detection hysteresis current	$V_{DD}=5\text{V}$			4.7		$\mu\text{A}$
$f_{\text{CP}}$	Charge pump frequency	$V_{DD}=5\text{V}$			490		kHz
Attenuation@mute	Input-to-output attenuation in shutdown	EN=0V, $V_{DD}=5\text{V}$			90		dB

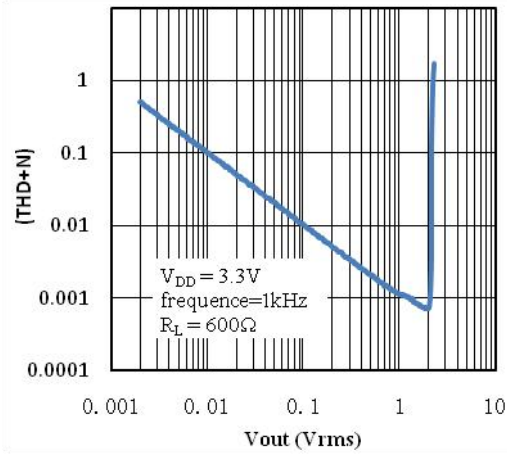
### Note:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.
2. A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.
3. Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

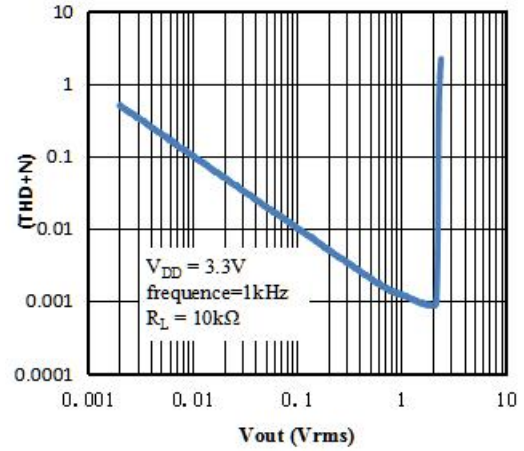
## Typical Characteristics

$T_A=25^\circ\text{C}$ ,  $V_{DD}=3.3\text{V}$ , unless otherwise noted

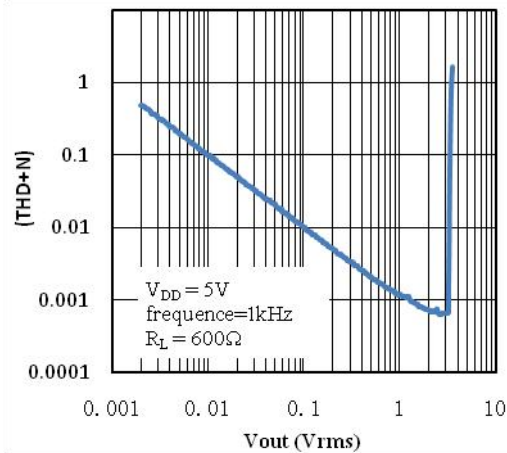
THD+N vs. Output Voltage



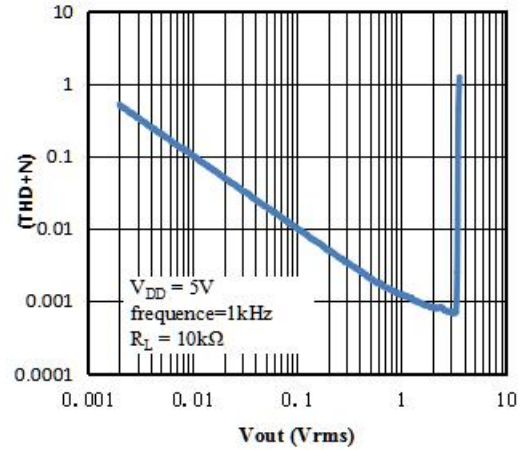
THD+N vs. Output Voltage



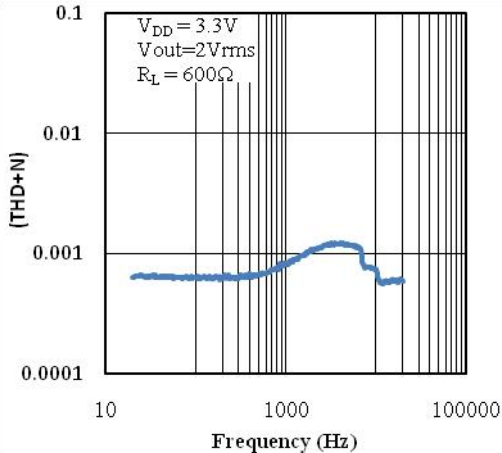
THD+N vs. Output Voltage



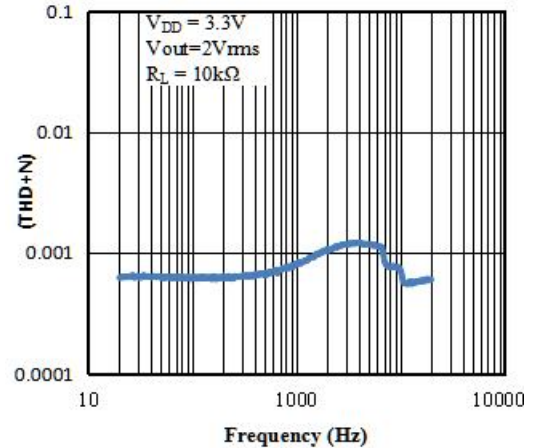
THD+N vs. Output Voltage



THD+N vs. Frequency

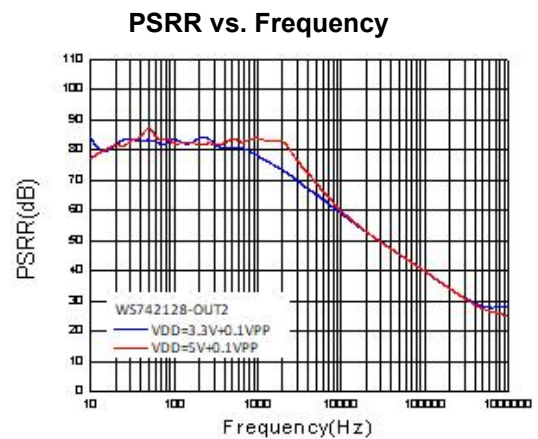
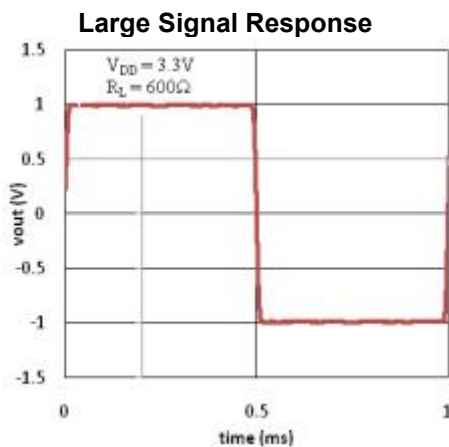
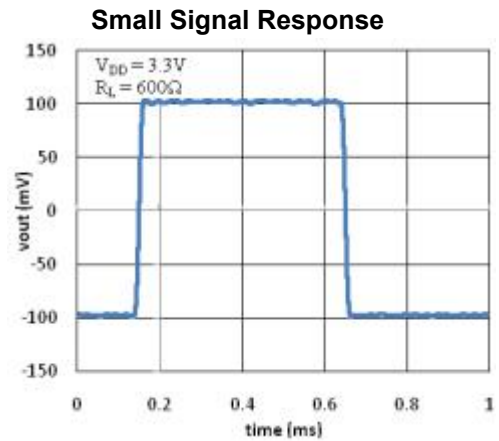
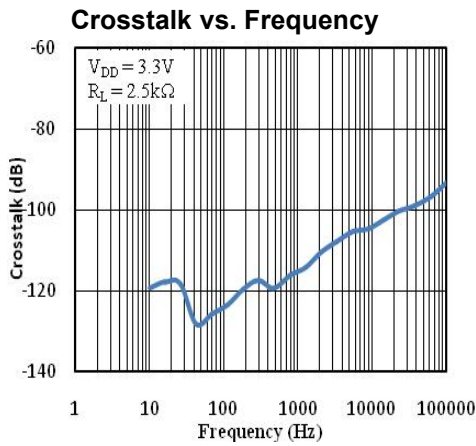
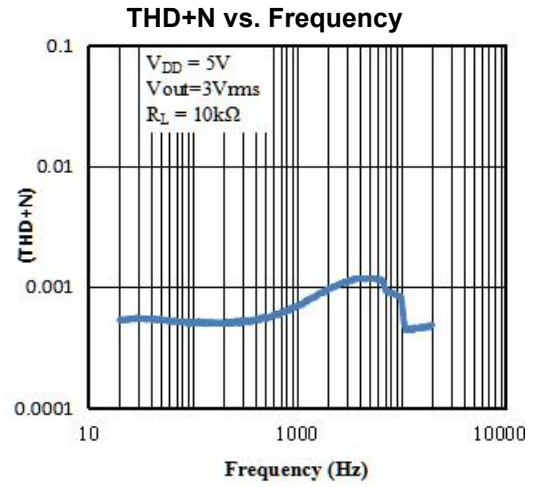
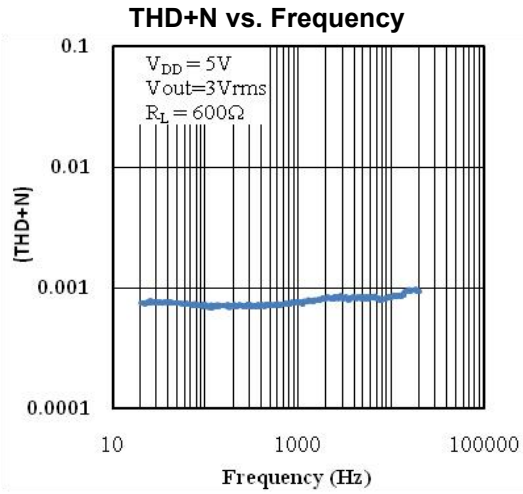


THD+N vs. Frequency

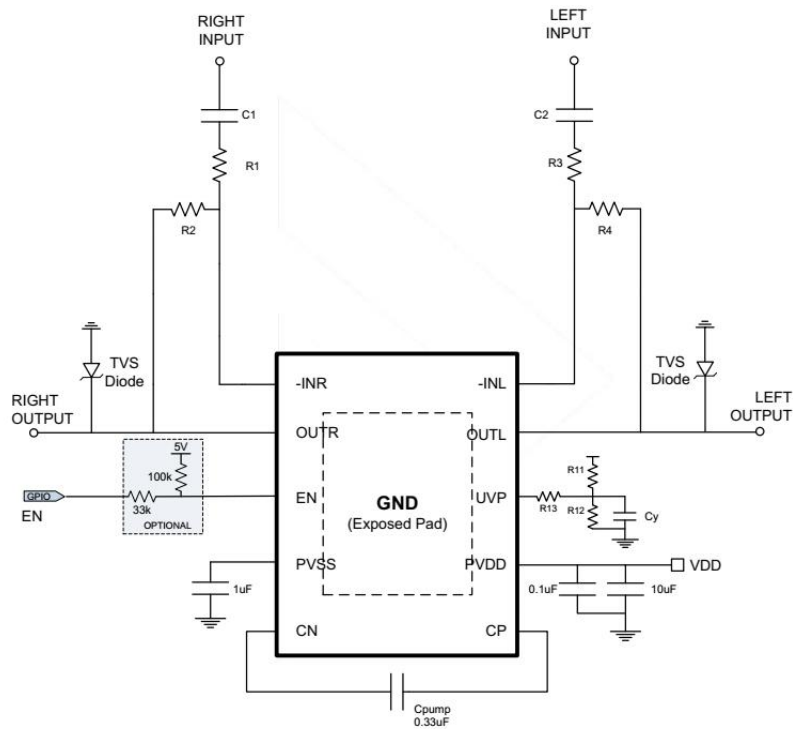


Typical Characteristics (continued)

$T_A=25^\circ\text{C}$ ,  $V_{DD}=3.3\text{V}$ , unless otherwise noted



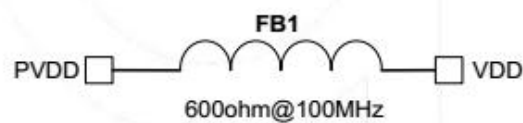
## Application Circuit



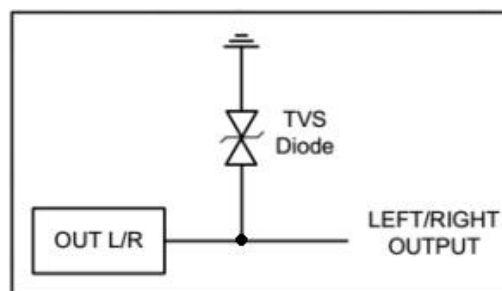
Differential-input, single-ended output, second-order filter  $R1=R3=15k\Omega$ ,  $R2=R4=30k\Omega$ ,  $C1=C2=33pF$ ,  $R11=5.6k\Omega$ ,  $R12=2.43k\Omega$ ,  $R13=15k\Omega$ ,  $Cpvss=0.33$  to  $1\mu F$ ,  $Cpump=0.33$  to  $1\mu F$ .

### Notes

1. In some applications, if the power supply noise needs to be filtered, the ferrite bead is recommended in a value of  $600\text{ohm}@100\text{MHz}$ , instead of RC network. RC network normally will lower the power supply resulting in the degraded the audio performance. If the resistor is not chosen properly, which can trigger the internal UVP detection circuit and shut down the output, as depicted below.



2. In order to protect the device against the power surge, transient voltage suppressor (TVS) devices are recommended at the output pins OUTL/OUTR.



## Application Notes

### Gain-Setting Resistors Ranges and Input-Blocking Capacitors

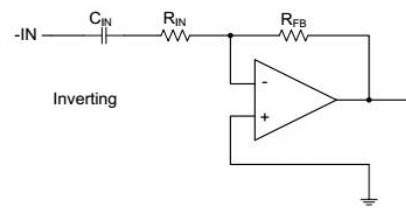
The gain-setting resistors,  $R_{IN}$  and  $R_{FB}$ , must be chosen so that noise, stability, and input capacitor size of the WS742128D are kept within acceptable limits. Voltage gain is defined as  $R_{FB}$  divided by  $R_{IN}$ . Table 1 lists the recommended resistor value for different gain settings. Selecting values that are too low demands a large input ac-coupling capacitor  $C_{IN}$ . Selecting values that are too high increases the noise of the amplifier. The gain-setting resistor must be placed close to the input pins to minimize capacitive loading on these input pins and to ensure maximum stability.

**Table 1. Input Capacitor with 2Hz cutoff and Resistor Values Recommended**

Input Res., $R_{IN}$	Feedback Res., $R_{fb}$	Inverting Gain
22 k $\Omega$	22 k $\Omega$	-1 V/V
15 k $\Omega$	30 k $\Omega$	-2 V/V
10 k $\Omega$	100 k $\Omega$	-10 V/V

$$f_{CIN} = \frac{1}{2\pi R_{IN} C_{IN}} \text{ or}$$

$$C_{IN} = \frac{1}{2\pi R_{IN} f_{CIN}}$$



**Equation 1. Cutoff decision Cutoff**

**Figure 2. Non-Inverting Gain Configuration**

### INPUT-BLOCKING CAPACITORS

DC input-blocking capacitors are required to be added in series with the audio signal into the input pins of WS742128D. These capacitors block the dc portion of the audio source and allow WS742128D inputs to be properly biased to provide maximum performance. These capacitors form a high-pass filter with the input resistor,  $R_{IN}$ . The cutoff frequency is calculated using the equation below. For this calculation, the capacitance used is the input-blocking capacitor, and the resistance is the input resistor chosen from Table 1; then the frequency and/or capacitance can be determined when one of the two values is given.



## 2nd Order Filter Typical Application

Several audio DACs used today require an external low-pass filter to remove out-of-band noise. This is possible with the WS742128D, as it can be used like an inverting OPAMP. Several filter topologies can be implemented, just like single-ended. In Figure 3, a multi-feedback (MFB) with single-ended input is shown. An ac-coupling capacitor to remove dc content from the source is shown; it serves to block any dc content from the source and lowers the dc-gain to 1, helping reduce the output dc-offset to minimum. The resistor values should have a low value for obtaining low noise, but should also have a high enough value to get a small size ac-coupling capacitor.

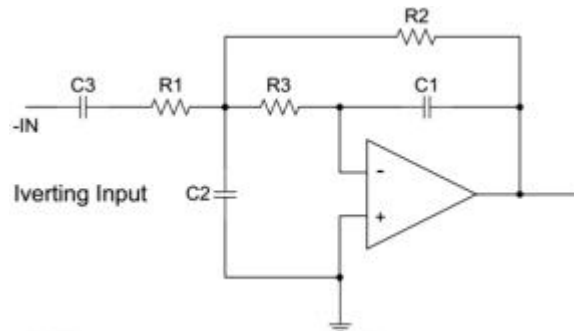


Figure 3. Second-Order Active Low-Pass Filter

## Charge Pump Flying Capacitor and PVSS Capacitor

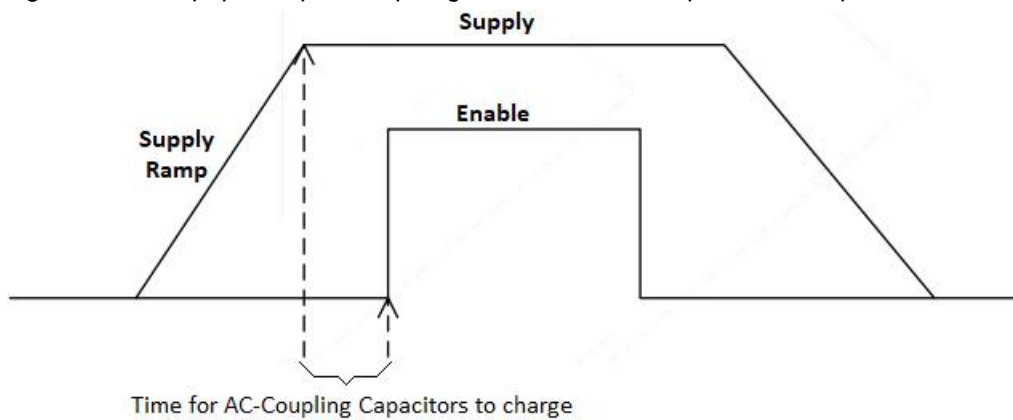
The charge pump flying capacitor serves to transfer charge during the generation of the negative supply voltage. The PVSS capacitor must be at least equal to the charge pump capacitor in order to allow maximum charge transfer. Low ESR X5R or X7R capacitors are recommended selection, a value of typical  $0.33\mu\text{F}$  is recommended for  $C_{\text{PUMP}}$ , and a value of typical  $1\mu\text{F}$  is recommended for PVSS. Capacitor values can be smaller than the value recommended, but the maximum output voltage may be reduced and the device may not operate to specifications.

## Decoupling Capacitors

The WS742128D requires adequate power supply decoupling to ensure that the noise and total harmonic distortion (THD) are low. A good low equivalent-series-resistance (ESR) X5R or X7R ceramic capacitor, typically a combine of paralleled  $0.1\mu\text{F}$  and  $10\mu\text{F}$ , placed as close as possible to the device VDD lead works best. Placing this decoupling capacitor close to the WS742128D is important for the performance of the amplifier. For filtering lower-frequency noise signals, a  $10\mu\text{F}$  or greater capacitor placed near the audio power amplifier would also help, but it is not required in most applications because of the high PSRR of this device.

## Pop-Free Power-Up

Pop-free power up is ensured by keeping the EN (shut down pin) low during power-supply ramp up and ramp down. The EN pin should be kept low until the input ac-coupling capacitors are fully charged before asserting the EN pin high to achieve pop-less power up. Figure6 illustrates the preferred sequence.

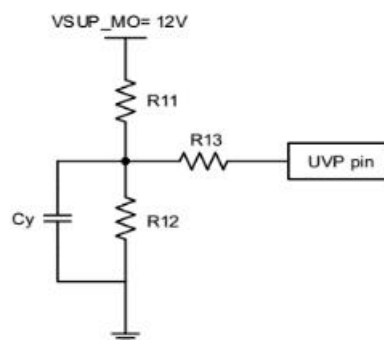


**Figure 4. Power-Up Sequences**

## External Under-voltage Detection

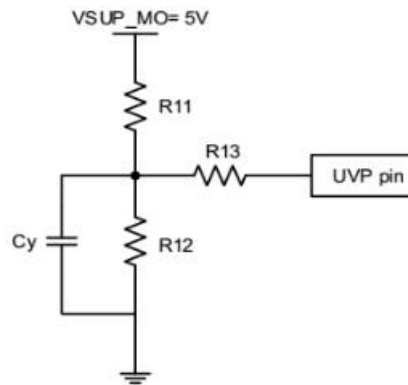
External under-voltage detection can be used to shut down the WS742128D before an input device can generate a pop noise. Although the shut down voltage is 1.21V, customers need to consider the accuracy of system passive components such as resistors and associated temperature variation. Users often select a resistor divider to obtain the power-on and shut down threshold for the specific application. The typical thresholds can be calculated as follows, respectively for VSUP\_MO at 5V and 12V. Usually for best power down noise performance, 12V supply is recommended for UVP circuitry as below. Typically this 12V is the power supply which generates the 5V supply for WS742128D PVDD pins.

### Case 1: VSUP\_MO=12V (Recommended)



$V_{UVP} = (1.21V - 4.7\mu A * R13) * (R11 + R12) / R12$ ;  $V_{hysteresis} = 4.7\mu A * R13 * (R11 + R12) / R12$ ; With the condition  $R13 \gg R11 // R12$ . For example, if  $R11 = 11k$ ,  $R12 = 1.4k$  and  $R13 = 47k$ , then  $V_{UVP} = 8.76V$ ;  $V_{hysteresis} = 1.957V$ . Here,  $V_{UVP}$  is the shut down threshold. In this case, the voltage at UVP pin 11 is greater than 1.431V under worst case of VSUP\_MO ripples.

Case 2: VSUP\_MO=5.0V



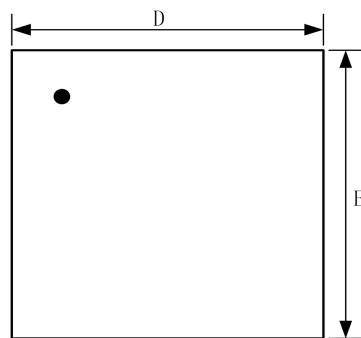
$V_{UVP} = (1.21V - 4.7\mu A * R13) * (R11 + R12) / R12$ ;  $V_{hysteresis} = 4.7\mu A * R13 * (R11 + R12) / R12$ ; With the condition  $R13 \gg R11 // R12$ . For example, if  $R11 = 5.6k$ ,  $R12 = 2.2k$  and  $R13 = 47k$ , then  $V_{UVP} = 3.506V$ ;  $V_{hysteresis} = 0.783V$ . Here,  $V_{UVP}$  is the shut down threshold. In this case, the voltage at UVP pin 11 is greater than 1.431V under worst case of VSUP\_MO ripples.

### Capacitive Load

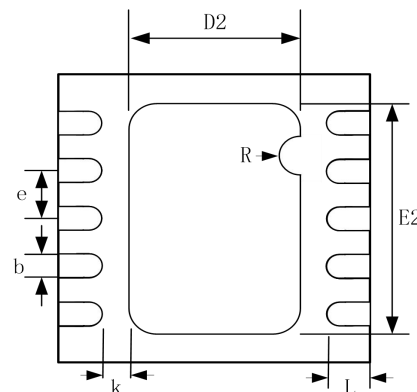
The WS742128D has the ability to drive a high capacitive load up to 220pF directly. Higher capacitive loads can be accepted by adding a series resistor of 47Ω or larger.

PACKAGE OUTLINE DIMENSIONS

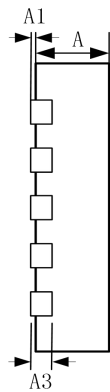
DFN2x2-10



TOP VIEW



BOTTOM VIEW



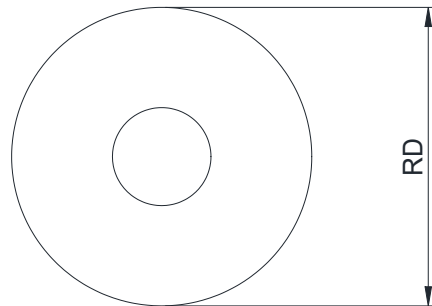
SIDE VIEW

Symbol	Dimensions In Millimeters (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 Ref.		
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.80	0.90	1.00
E2	1.30	1.40	1.50
e	0.30	0.40	0.50
L	0.22	0.30	0.35
k	0.15	0.25	0.35
R	0.10 Ref.		

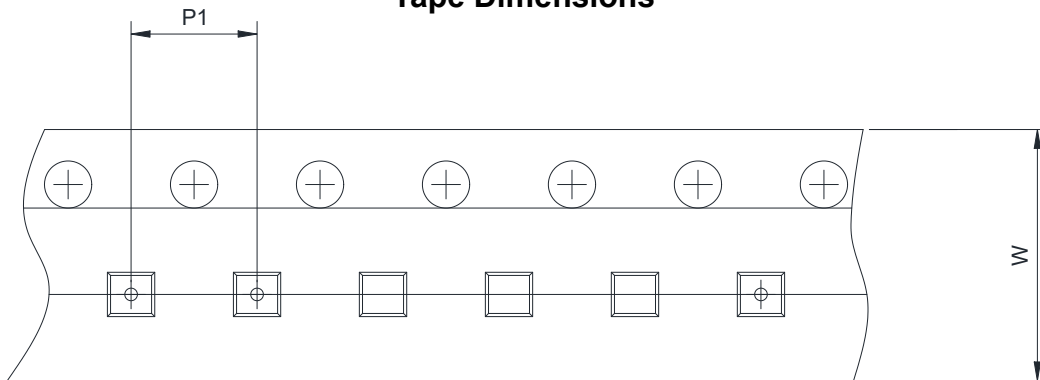
**TAPE AND REEL INFORMATION**

**DFN2x2-10**

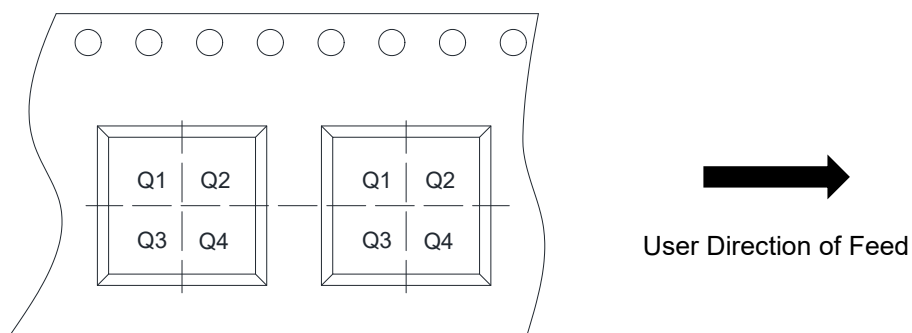
**Reel Dimensions**



**Tape Dimensions**



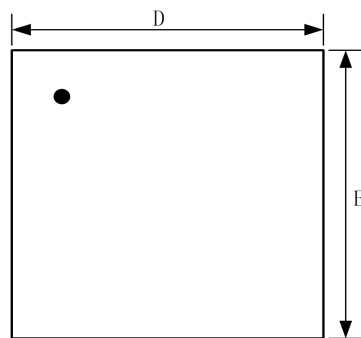
**Quadrant Assignments For PIN1 Orientation In Tape**



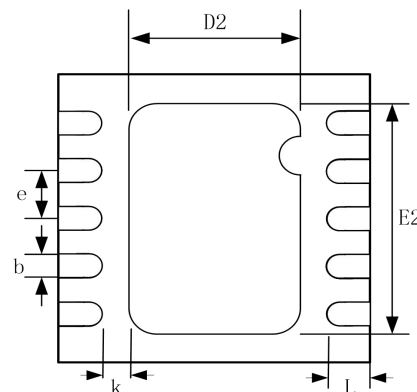
RD	Reel Dimension	<input checked="" type="checkbox"/> 7inch	<input type="checkbox"/> 13inch		
W	Overall width of the carrier tape	<input checked="" type="checkbox"/> 8mm	<input type="checkbox"/> 12mm		
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input checked="" type="checkbox"/> 4mm	<input type="checkbox"/> 8mm	
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2	<input type="checkbox"/> Q3	<input type="checkbox"/> Q4

PACKAGE OUTLINE DIMENSIONS

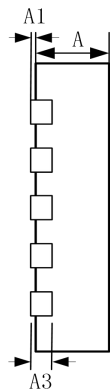
DFN3x3-10



TOP VIEW



BOTTOM VIEW



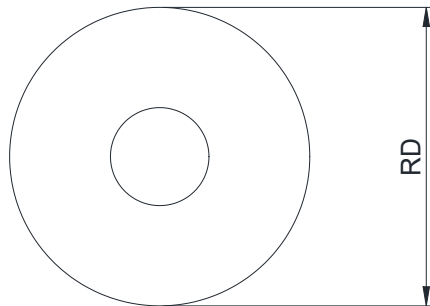
SIDE VIEW

Symbol	Dimensions In Millimeters (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	-	0.20 REF	-
b	0.20	0.25	0.30
D	3.00 BSC		
E	3.00 BSC		
D2	1.55	1.65	1.75
E2	2.30	2.40	2.50
e	0.50 BSC		
L	0.35	0.40	0.45
k	0.25	-	-

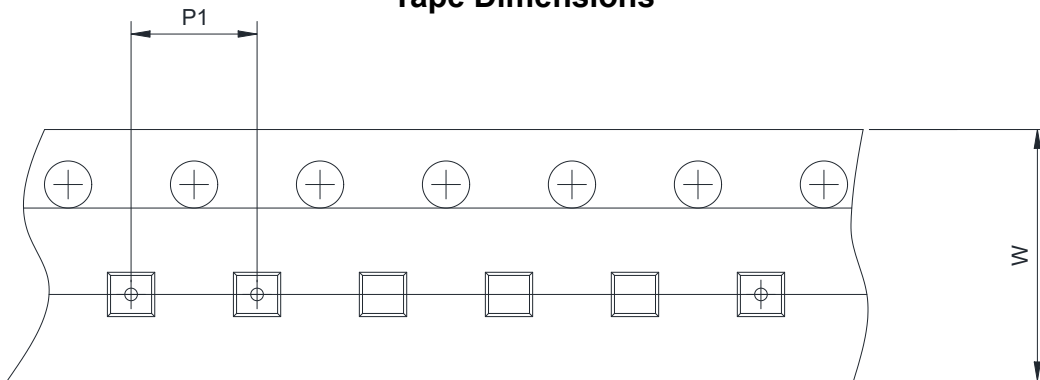
**TAPE AND REEL INFORMATION**

**DFN3x3-10**

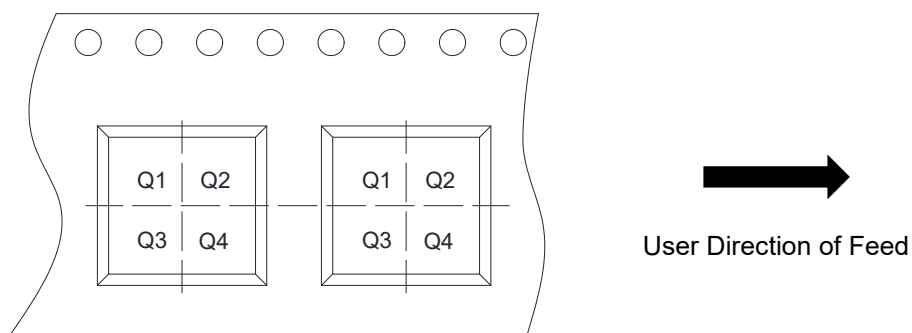
**Reel Dimensions**



**Tape Dimensions**



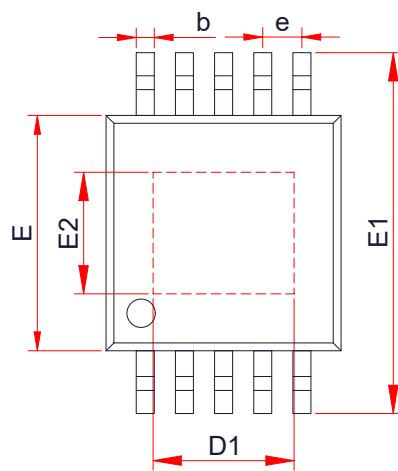
**Quadrant Assignments For PIN1 Orientation In Tape**



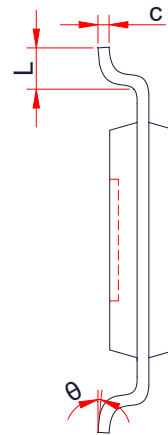
RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch		
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm		
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm	<input checked="" type="checkbox"/> 8mm	
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2	<input type="checkbox"/> Q3	<input type="checkbox"/> Q4

PACKAGE OUTLINE DIMENSIONS

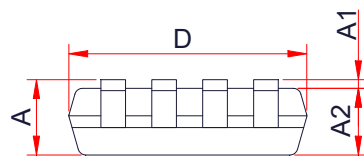
EMSOP-10L



TOP VIEW



SIDE VIEW



SIDE VIEW

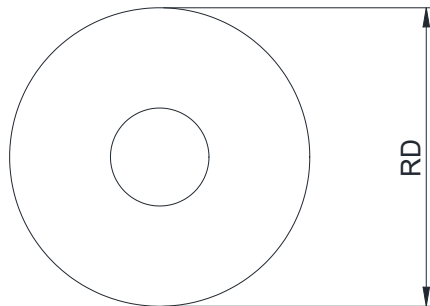
Symbol	Dimensions In Millimeters (mm)		
	Min.	Typ.	Max.
A	0.82	0.96-	1.10
A1	0.02	-	0.15
A2	0.75	0.85	0.95
b	0.18	-	0.28
c	0.09	-	0.23
D	2.90	3.00	3.10
D1	1.70	1.80	1.90
E1	4.75	4.90	5.05
E	2.90	3.00	3.10
E2	1.45	1.55	1.65
e	0.50 BSC		
L	0.40	-	0.80
$\theta$	0°	-	6°



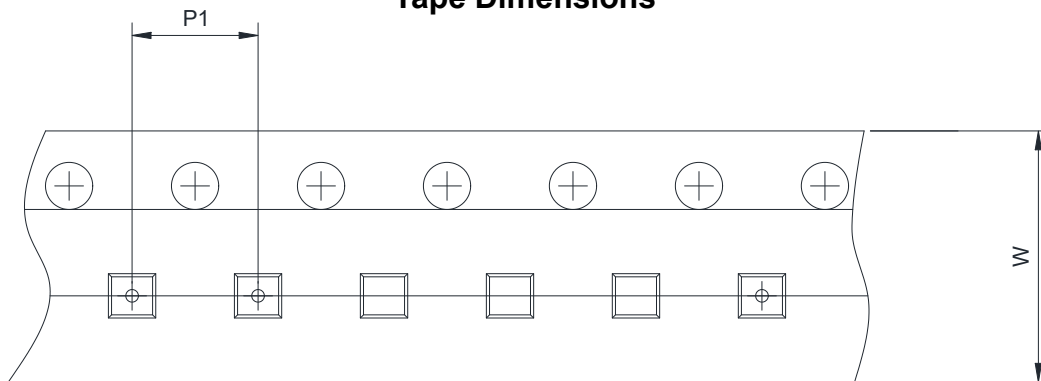
**TAPE AND REEL INFORMATION**

**EMSOP-10L**

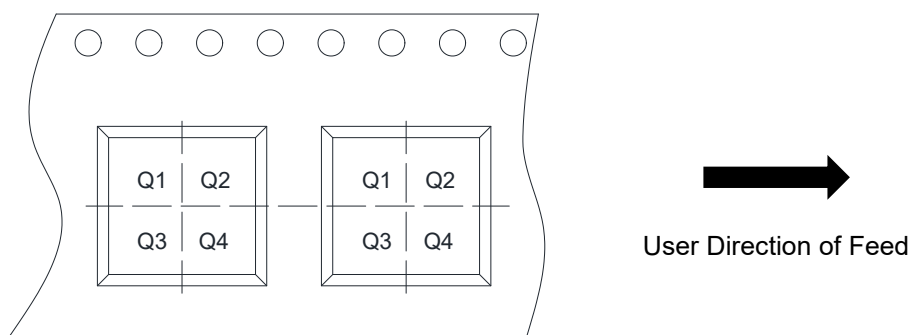
**Reel Dimensions**



**Tape Dimensions**



**Quadrant Assignments For PIN1 Orientation In Tape**



RD	Reel Dimension	<input type="checkbox"/> 7inch	<input checked="" type="checkbox"/> 13inch		
W	Overall width of the carrier tape	<input type="checkbox"/> 8mm	<input checked="" type="checkbox"/> 12mm		
P1	Pitch between successive cavity centers	<input type="checkbox"/> 2mm	<input type="checkbox"/> 4mm	<input checked="" type="checkbox"/> 8mm	
Pin1	Pin1 Quadrant	<input checked="" type="checkbox"/> Q1	<input type="checkbox"/> Q2	<input type="checkbox"/> Q3	<input type="checkbox"/> Q4

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