

# WSD100N06GDN56

#### **N-Ch MOSFET**

#### **General Description**

The WSD100N06GDN56 is the SGT MOSFET with extreme high cell density, which provide excellent R<sub>DSON</sub> and gate charge for most of the synchronous buck converter applications.

The WSD100N06GDN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

#### Features

Lead Fre e an d Green Devices Available

(RoH SCom plia nt)

100% UIS + Rg Tested

Reliable and Rugged

Moistu re Sensitivity Level MSL1

(per JED EC J-STD-020D)

#### **Product Summery**

Bvdss	Rdson	Id
60V	<b>3.0m</b> Ω	100A

#### Applications

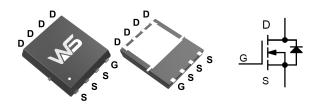
Secondary Side Synchronous Rectification

DC-DC Converter

Motor Control

Load Switching

#### DFN5x6A-8\_EP Pin Configuration



Symbol	Parameter			Rating	Units	
Vds	Drain-Source Voltage			60	V	
V <sub>GS</sub>	Gate-Source Voltage			$\pm 20$	V	
Ip <sup>1,6</sup>	Continuous Drain Current Tc=25°C Tc=100°C		C	100	A	
ID <sup>1,0</sup>			°C	65		
Idm <sup>2</sup>	Pulsed Drain Current To	Tc=25°C		240	А	
D		=25°0	C	83		
PD	Maximum Power Dissipation Tc=10		°C	50	W	
I <sub>AS</sub>	Avalanche Current, Single pulse			45	А	
Eas <sup>3</sup>	Single Pulse Avalanche Energy			101	mJ	
TJ	Maximum Junction Temperature			150	°C	
Tstg	Storage Temperature Range			-55 to 150	°C	
$\mathbf{R}_{\mathbf{ hetaJA}}^{1}$	Thermal Resistance Junction to ambient	ent Steady State		55	°C/W	
Rejc <sup>1</sup>	Thermal Resistance-Junction to Case		Steady State	1.5	°C/W	

#### Absolute Maximum Ratings @TA=25°C unless otherwise noted



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#### Electrical Characteristics @TA=25°C unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Static						
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250 \mu A$	60			V
IDSS	Zerr Cete Meltere Desin Connect	$V_{DS} = 48 \text{ V}, V_{GS} = 0 \text{ V}$			1	A
	Zero Gate Voltage Drain Current	T <sub>J</sub> =85°C	C		30	μA 30
Igss	Gate Leakage Current	$V_{GS} = \pm 20V, V_{DS} = 0V$			±100	nA
On Characte	ristics					
V <sub>GS(TH)</sub>	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_{DS} = 250 \mu A$	1.2	1.8	2.5	V
D 2	Drain-Source On-state Resistance	$V_{GS} = 10V, I_D = 20A$		3.0	3.6	mΩ
RDS(on) <sup>2</sup>		$V_{GS} = 4.5V, I_D = 15A$		4.4	5.4	mΩ
Switching						
Qg	Total Gate Charge	V <sub>DS</sub> =30V		58		nC
Qgs	Gate-Sour Charge	V <sub>GS</sub> =10V		16		nC
Qgd	Gate-Drain Charge	ID=20A		4.0		nC
td (on)	Turn-on Delay Time	V <sub>GEN</sub> =10V		18		ns
tr	Turn-on Rise Time	V <sub>DD</sub> =30V I <sub>D</sub> =20A		8		ns
td(off)	Turn-off Delay Time	$R_{G}=\Omega$		50		ns
tf	Turn-off Fall Time			11		ns
Rg	Gat resistance	V <sub>GS</sub> =0V, V <sub>DS</sub> =0V, f=1MHz		0.7		Ω
Dynamic						
Ciss	In Capacitance	V <sub>GS</sub> =0V		3458		pF
Coss	Out Capacitance	V <sub>DS</sub> =30V		1522		pF
Crss	Reverse Transfer Capacitance	f=1MHz		22		pF
Drain-Source	e Diode Characteristics and Maximum	Ratings				
Is <sup>1,5</sup>	Continuous Source Current	V <sub>G</sub> =V <sub>D</sub> =0V, Force Current			55	А
Іѕм	Pulsed Source Current3				240	А
Vsd <sup>2</sup>	Diode Forward Voltage	$I_{SD} = 1A$ , $V_{GS} = 0V$		0.8	1.3	V
trr	Reverse Recovery Time	I <sub>SD</sub> =20A, dl <sub>SD</sub> /dt=100A/µs		27		ns
Qrr	Reverse Recovery Charge	$1_{SD}$ -207, $u_{SD}$ / $u$ - 100A/ $\mu$ S		33		nC

Note :

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.

2.The data tested by pulsed , pulse width  $\leq$  300us , duty cycle  $\leq$  2%

3. The EAS data shows Max. rating . The test condition is  $V_{\text{DD}}\text{=}50V, V_{\text{GS}}\text{=}10V, L\text{=}0.1\text{mH}, I_{\text{AS}}\text{=}40\text{A}$ 

4. The power dissipation is limited by 150°C junction temperature

5. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

6. The maximum current rating is package limited.



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## **Typical Operating Characteristics**

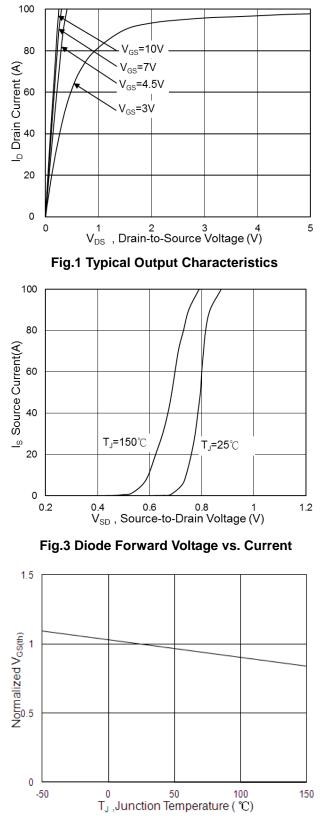


Fig.5 Normalized  $V_{GS(th)}$  vs T<sub>J</sub>

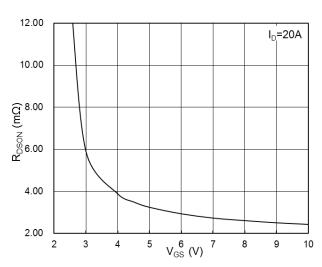


Fig.2 On-Resistance vs G-S Voltage

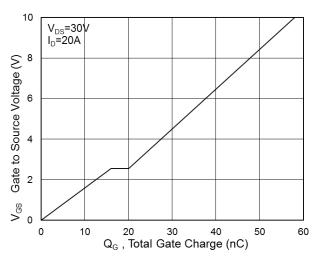
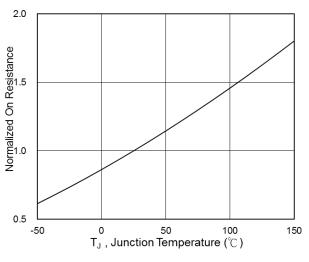
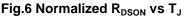


Fig.4 Gate-Charge Characteristics

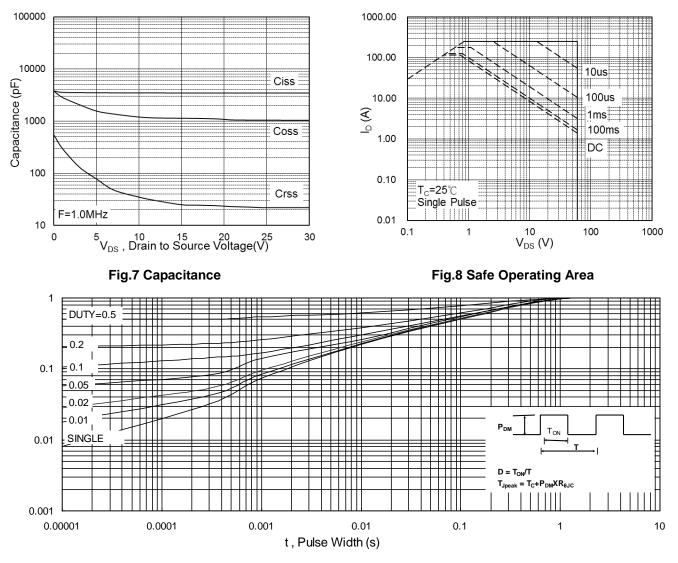




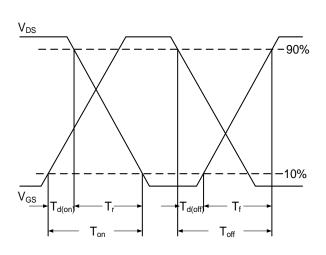


**N-Ch MOSFET** 

### **Typical Operating Characteristics (Cont.)**









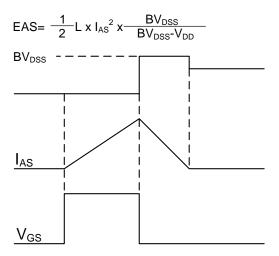


Fig.11 Unclamped Inductive Switching Waveform



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