

General Description

The WSD30150DN56 is the highest performance trench N-Ch MOSFET with extreme high celldensity ,which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSD30150DN56 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Product Summery

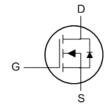
BVDSS	RDSON	ID
30V	1.8mΩ	150A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter
- Networking DC-DC Power System
- Power Tool Application

DFN5X6-8 Pin Configuration





Absolute Maximum Ratings

Symbol	Parameter Ratio		Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	±20	V
I _D @T _C =25℃	Continuous Drain Current, V _{GS} @ 10V ^{1,7}	150	Α
I _D @T _C =100℃	Continuous Drain Current, V _{GS} @ 10V ^{1,7}		А
I _{DM}	Pulsed Drain Current ² 200		А
EAS	Single Pulse Avalanche Energy ³	125	mJ
I _{AS}	Avalanche Current 50		Α
P _D @T _C =25°C	Total Power Dissipation ⁴ 62.5		W
T _{STG}	Storage Temperature Range -55 to 150		$^{\circ}$
TJ	Operating Junction Temperature Range -55 to 150		$^{\circ}$

Thermal Data

Symbol	Parameter	Тур.	Max.	Unit
$R_{ heta JA}$	Thermal Resistance Junction-Ambient ¹		30	°C/W
$R_{ heta JC}$	Thermal Resistance Junction-Case ¹		2	°C/W



N-Ch MOSFET

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V , I _D =250uA	30			V
$\triangle BV_{DSS}/\triangle T_{J}$	BV _{DSS} Temperature Coefficient	Reference to 25℃, I _D =1mA		0.02		V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V , I _D =20A		1.8	2.4	0
		V _{GS} =4.5V , I _D =15A		2.4	3.2	mΩ
V _{GS(th)}	Gate Threshold Voltage	\/ -\/ -250\	1.4	1.7	2.5	V
$\triangle V_{GS(th)}$	V _{GS(th)} Temperature Coefficient	$V_{GS}=V_{DS}$, $I_D=250uA$		-6.1		mV/℃
	V _{DS} =24V , V _{GS} =0V , T _J =25°C			1		
I _{DSS}	Drain-Source Leakage Current	V _{DS} =24V , V _{GS} =0V , T _J =55℃			5	- uA
I _{GSS}	Gate-Source Leakage Current	V_{GS} = $\pm 20 V$, V_{DS} = $0 V$			±100	nA
gfs	Forward Transconductance	V _{DS} =5V , I _D =10A		27		S
Rg	Gate Resistance	V _{DS} =0V , V _{GS} =0V , f=1MHz		0.8	1.5	Ω
Q_g	Total Gate Charge (4.5V)	V _{DS} =15V , V _{GS} =4.5V , I _D =30A		26		
Q_gs	Gate-Source Charge			9.5		nC
Q _{gd}	Gate-Drain Charge			11.4		
T _{d(on)}	Turn-On Delay Time			20		
Tr	Rise Time	V_{DD} =15V , V_{GEN} =10V , R_{G} =6 Ω , I_{D} =1A, RL =15 Ω .		12		
T _{d(off)}	Turn-Off Delay Time			69		ns
T _f	Fall Time			29		
C _{iss}	Input Capacitance	V _{DS} =15V , V _{GS} =0V , f=1MHz		3200		
C _{oss}	Output Capacitance			680		pF
C _{rss}	Reverse Transfer Capacitance			320		

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =25V , L=0.1mH , I _{AS} =30A	98			mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	-V _G =V _D =0V , Force Current			30	Α
I _{SM}	Pulsed Source Current ^{2,6}				200	Α
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V , I _S =A , T _J =25℃			1.2	V

Note:

- 1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, t<10 sec.
- 2.The data tested by pulsed , pulse width \leq 300us , duty cycle \leq 2%
- 3. The EAS data shows Max. rating . The test condition is V_{DD} =25V, V_{GS} =10V, L=0.1mH, I_{AS} =30A
- 4.The power dissipation is limited by 150 $^{\circ}\mathrm{C}$ junction temperature
- 5.The Min. value is 100% EAS tested guarantee.
- 6. The data is theoretically the same as I_D and I_{DM} , in real applications, should be limited by total power dissipation.
- 7.Package limitation current is 100A.



Typical Characteristics

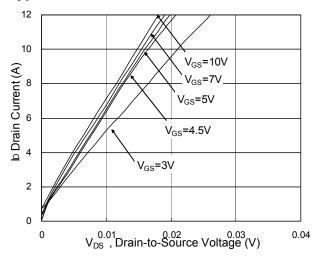


Fig.1 Typical Output Characteristics

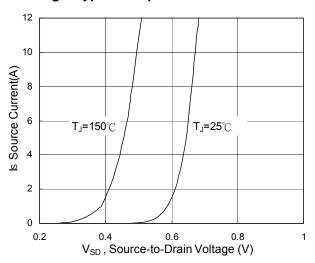


Fig.3 Forward Characteristics of Reverse

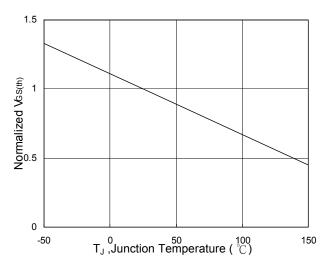


Fig.5 Normalized V_{GS(th)} v.s T_J

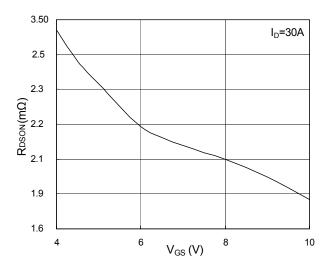


Fig.2 On-Resistance v.s Gate-Source

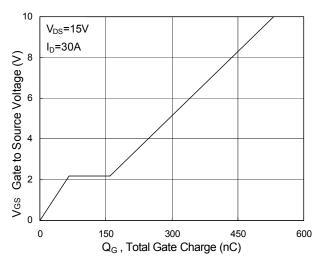


Fig.4 Gate-Charge Characteristics

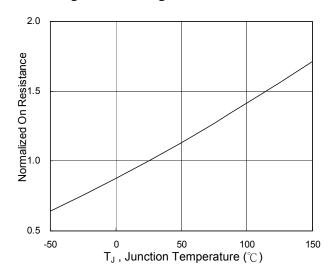
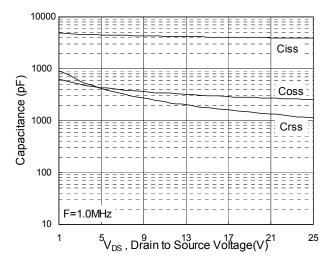


Fig.6 Normalized R_{DSON} v.s T_J





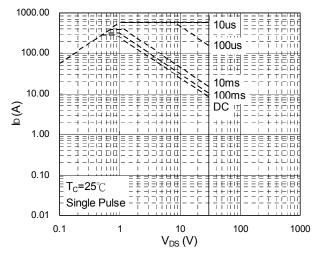


Fig.7 Capacitance

Fig.8 Safe Operating Area

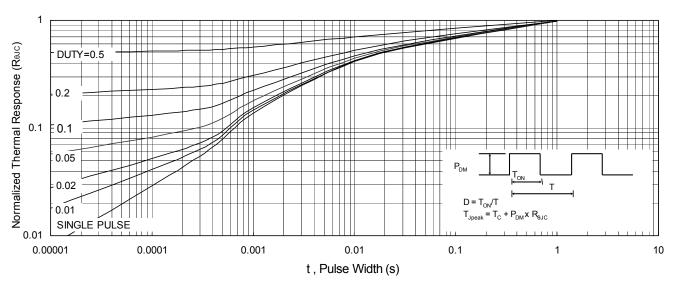


Fig.9 Normalized Maximum Transient Thermal Impedance

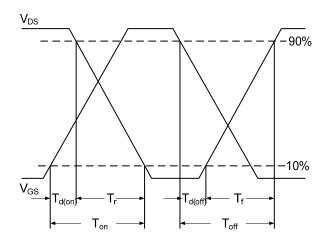


Fig.10 Switching Time Waveform

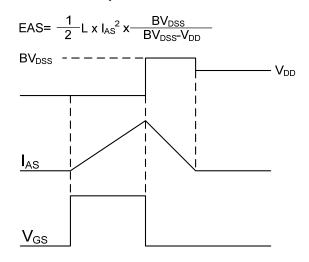


Fig.11 Unclamped Inductive Waveform



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