## General Description

The WSD3069DN56 is the highest performance trench N-ch and P-ch MOSFET with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSD3069DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

## Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

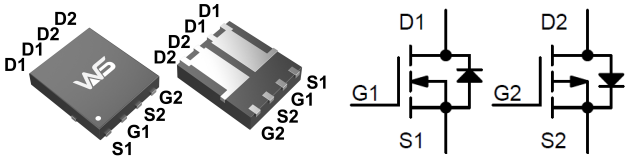
## Product Summery

| BVDSS | RDSON | ID |
|---|---|---|
| 30V | 15mΩ | 16A |
| -30V | 15mΩ | -16A |

## Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- CCFL Back-light Inverter

## DFN5X6C-8 Pin Configuration




## Absolute Maximum Ratings ($T_A$= 25°C unless otherwise noted)

| Symbol | Parameter | | N Channl | P Channl | Unit |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain-Source Voltage | | 30 | -30 | V |
| $V_{GSS}$ | Gate-Source Voltage | | ±20 | ±20 | |
| $I_D$ | Continuous Drain Current G | Tc=25°C | 16 | -16 | A |
| | | Tc=100°C | 10.5 | -12.5 | |
| $I_{DM}$ | Pulsed Drain Current C | | 35 | -65 | A |
| $I_{DSM}$ | Continuous Drain Current | $T_A$=25°C | 9.5 | -11 | A |
| | | $T_A$=70°C | 7.5 | -8.5 | |
| $P_D$ | Maximum Power Dissipation B | Tc=25°C | 10 | 20 | W |
| | | Tc=100°C | 4 | 8 | |
| $P_{DSM}$ | Maximum Power Dissipation A | Tc=25°C | 3.1 | 4.1 | W |
| | | Tc=100°C | 2 | 2.6 | |
| $I_S$ | Diode Continuous Forward Current | Tc=25°C | 10 | -16 | A |
| $E_{AS}$ | Single pulsed avalanlce energy C | L=0.5mH | 7 | -36 | mJ |
| $I_{AS}$ | Single pulsed avalanlce Current | L=0.5mH | 12 | -27 | A |
| $T_j$ | Maximum Junction Temperature | | 150 | 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -55 to 150 | -55 to 150 | |
| $R_{\theta JA}$ | Thermal Resistance-Junction to Ambient AD | t≤10S | 40 | 30 | °C/W |
| | | Steady StateC | 70 | 65 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance-Junction to Case | | 21 | 6 | °C/W |

## N-Channl Electrical Characteristics ($T_J$= 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_{DS}$=250μA | 30 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ =24V, $V_{GS}$=0V | - | - | 1 | μA |
| | | $T_j$=55°C | - | - | 5 | μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ =$V_{GS}$, $I_{DS}$=250μA | 1 | 1.5 | 2 | V |
| $I_{GSS}$ | Gate Leakage Current | $V_{GS}$=±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| $R_{DS(ON)}$ | Drain-Source On-state Resistance | $V_{GS}$=10V, $I_{DS}$=10A | - | 15 | 19.5 | mΩ |
| | | $V_{GS}$=4.5V, $I_{DS}$=5A | - | 18 | 24 | |
| $R_G$ | Gate Resistance | F=1MHz, $V_{GS}$=0V, $V_{DS}$=0V | - | - | 2.8 | Ω |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$ =15V, Frequency=1.0MHz | - | 373 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 67 | - | |
| $C_{rss}$ | Reverse transfer capacitance | | - | 41 | - | |
| $t_{d(ON)}$ | Turn-on delay Time | $V_{GEN}$=10V ,$V_{DD}$=15V $R_G$=3Ω, RL=1.5Ω | - | 4.3 | - | nS |
| $t_r$ | Turn-on rise Time | | - | 2.8 | - | |
| $t_{d(OFF)}$ | Turn-off delay Time | | - | 15.8 | - | |
| $t_f$ | Turn-off rise Time | | - | 3 | - | |
| $Q_g$ | Total Gate Charge (10V) | $V_{DS}$ =15V, $V_{GS}$=10V, $I_{DS}$=10A | - | 7.1 | - | nC |
| $Q_g$ | Total Gate Charge (4.5V) | | - | 3.5 | - | |
| $Q_{gs}$ | Gate-Source Charge | | - | 1.2 | - | |
| $Q_{gd}$ | Gate-Drain Charge | | - | 1.6 | - | |
| $V_{SD}$ | Diode Forward Voltage | $I_{SD}$=1A, $V_{GS}$=0V | - | 0.75 | 1 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{DS}$=10A, $dI_{SD}/dt$=500A/μs | - | 6 | - | ns |
| Qrr | Reverse Recovery Charge | | - | 6.6 | - | nC |

A. The value of $R_{\theta JA}$ is measured with the device mounted on 1in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$ =25° C. The Power dissipation $P_{DSM}$ is based on $R_{\theta JA}$ t≤ 10s and the maximum allowed junction temperature of 150° C. The value in any given application depends on the user's specific board design.

B. The power dissipation $P_D$ is based on $T_{J(MAX)}$=150° C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Single pulse width limited by junction temperature $T_{J(MAX)}$=150° C.

D. The $R_{\theta JA}$ is the sum of the thermal impedance from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink,rating. assuming a maximum junction temperature of TJ(MAX)=150°C. The SOA curve provides a single pulse

G. The maximum current rating is package limited.

H. These tests are performed with the device mounted on 1 in$^2$ FR-4 board with 2oz. Copper, in a still air environment with $T_A$=25° C.

## P-Channl Electrical Characteristics ($T_J$= 25°C unless otherwise noted)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$=0V, $I_{DS}$=-250A | -30 | - | - | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ =-24V, $V_{GS}$=0V | - | - | -1 | μA |
| | | $T_j$=55°C | - | - | -5 | μA |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ =$V_{GS}$, $I_{DS}$=-250A | 1 | 1.5 | 2 | V |
| $I_{GSS}$ | Gate Leakage Current | $V_{GS}$=±20V, $V_{DS}$=0V | - | - | ±100 | nA |
| $R_{DS(ON)}$ | Drain-Source On-state Resistance | $V_{GS}$=-10V, $I_{DS}$=-9.7A | - | 15 | 20 | mΩ |
| | | $V_{GS}$=-4.5V, $I_{DS}$=-7A | - | 20 | 27 | |
| $R_G$ | Gate Resistance | F=1MHz, $V_{GS}$=0V,$V_{DS}$=0V | - | 4 | - | Ω |
| $C_{iss}$ | Input Capacitance | $V_{GS}$=0V, $V_{DS}$=-15V, Frequency=1.0MHz | - | 1040 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 180 | - | |
| $C_{rss}$ | Reverse transfer capacitance | | - | 125 | - | |
| $t_{d(ON)}$ | Turn-on delay Time | $V_{GEN}$=-10V ,$V_{DD}$=-15V $R_G$=3Ω, RL=1.5Ω | - | 10 | - | nS |
| $t_r$ | Turn-on rise Time | | - | 5.5 | - | |
| $t_{d(OFF)}$ | Turn-off delay Time | | - | 26 | - | |
| $t_f$ | Turn-off rise Time | | - | 9 | - | |
| $Q_g$ | Total Gate Charge | $V_{DS}$=-15V, $V_{GS}$=-10V, $I_{DS}$=-9.7A | - | 19 | - | nC |
| $Q_g$ | Total Gate Charge | | - | 9.6 | - | |
| $Q_{gs}$ | Gate-Source Charge | | - | 3.6 | - | |
| $Q_{gd}$ | Gate-Drain Charge | | - | 4.6 | - | |
| $V_{SD}$ | Diode Forward Voltage | $I_{SD}$=-1A, $V_{GS}$=0V | - | -0.75 | -1.1 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_{DS}$=-9.7A, $dI_{SD}$/dt=500A/μs | - | 11.5 | - | ns |
| Qrr | Reverse Recovery Charge | | - | 25 | - | nC |

## N-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

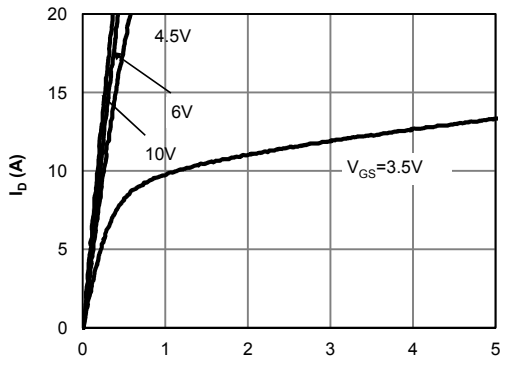



Figure 1: On-Region Characteristics (Note E)

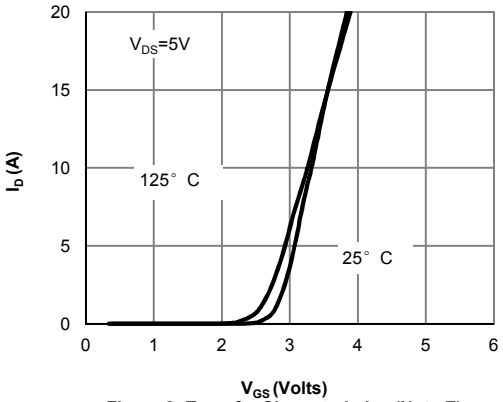



Figure 2: Transfer Characteristics (Note E)

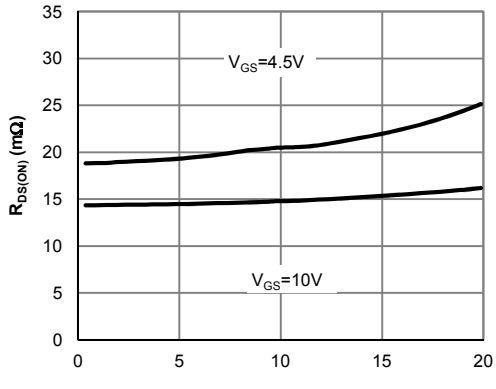



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

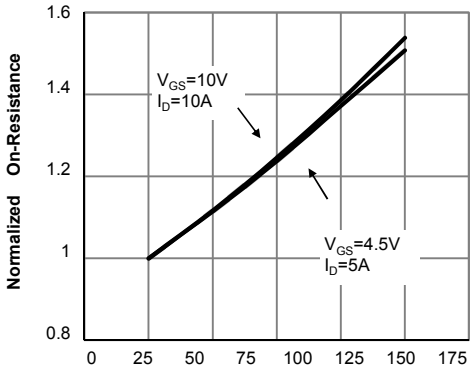



Figure 4: On-Resistance vs. Junction Temperature (Note E)

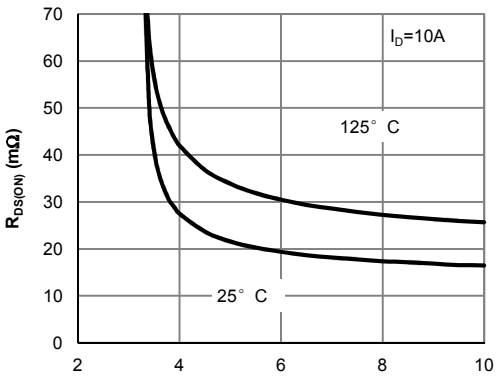



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

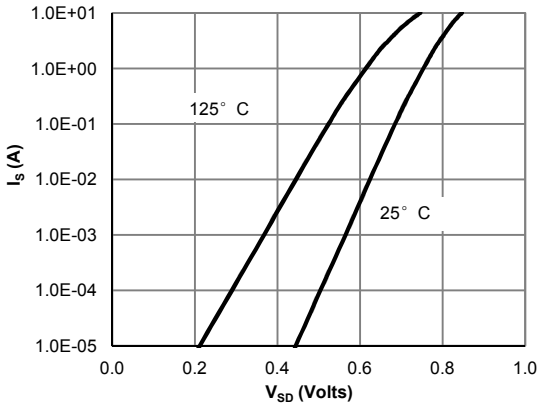



Figure 6: Body-Diode Characteristics (Note E)

**N-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

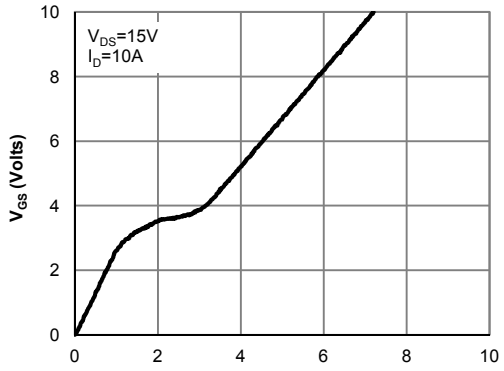



**Figure 7: Gate-Charge Characteristics**

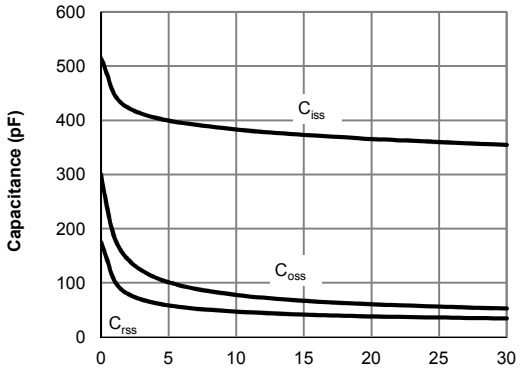



**Figure 8: Capacitance Characteristics**

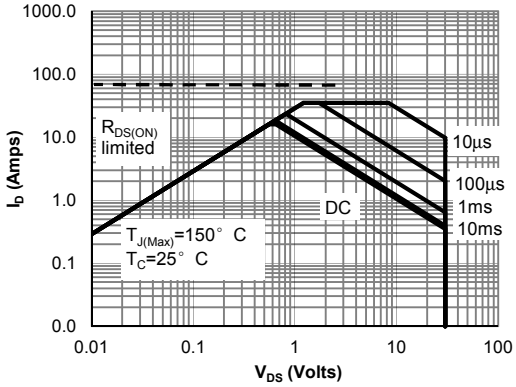



**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

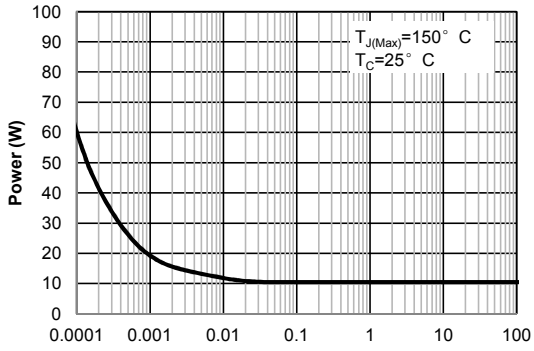



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

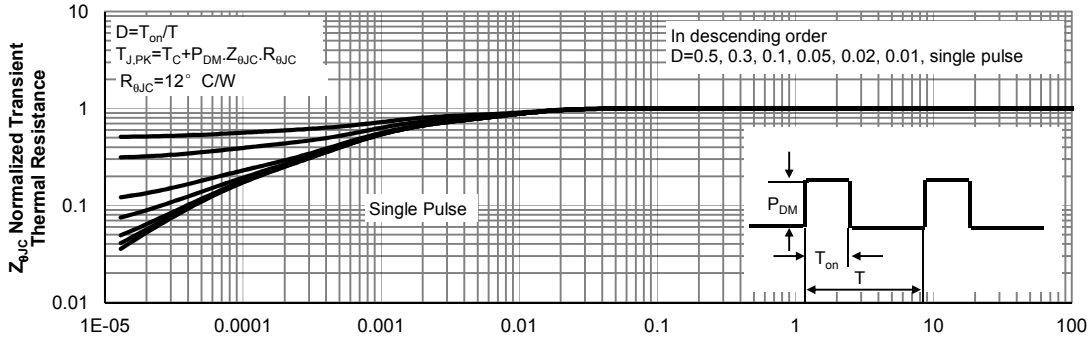



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**N-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

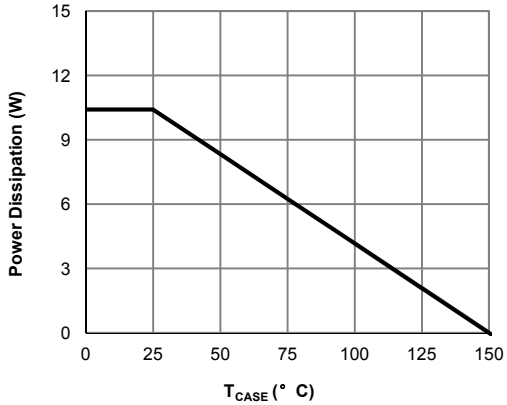



**Figure 12: Power De-rating (Note F)**

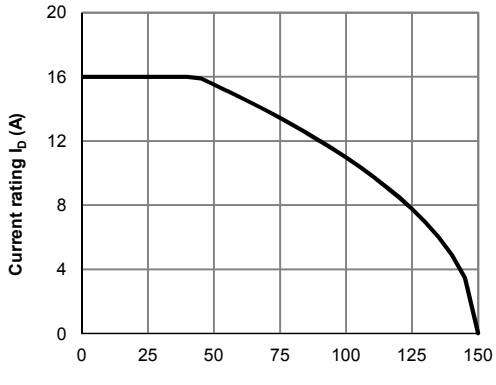



**Figure 13: Current De-rating (Note F)**

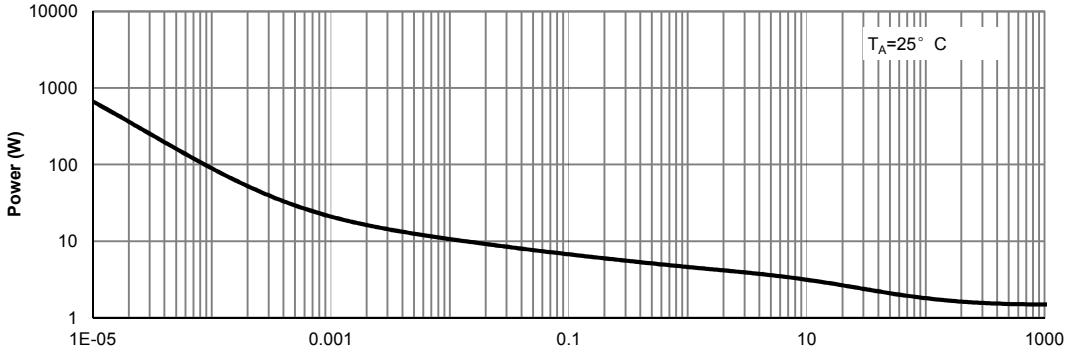



**Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)**

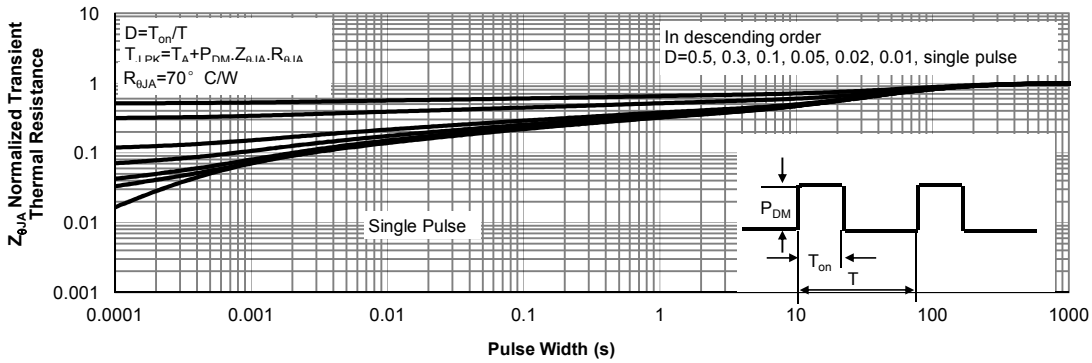



**Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)**

## P-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

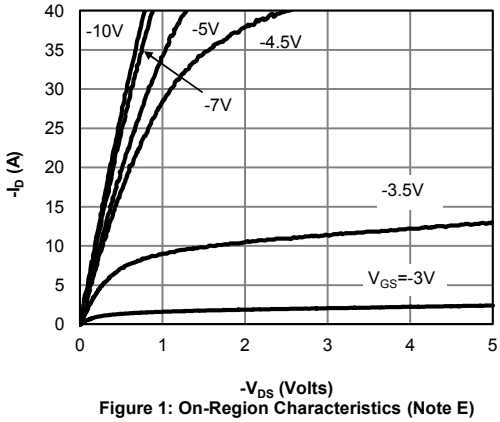



Figure 1: On-Region Characteristics (Note E)

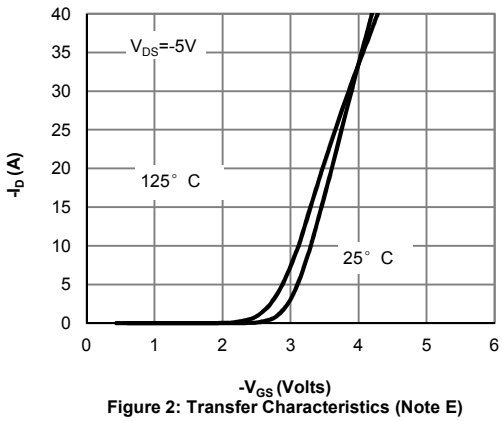



Figure 2: Transfer Characteristics (Note E)

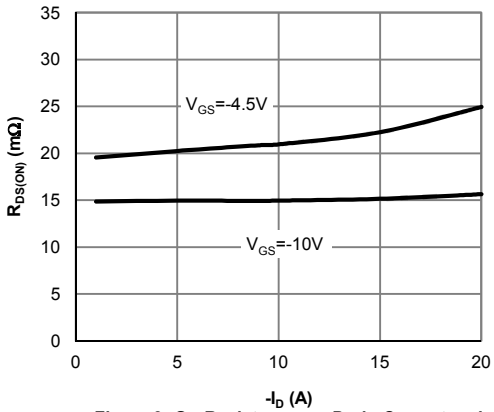



Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

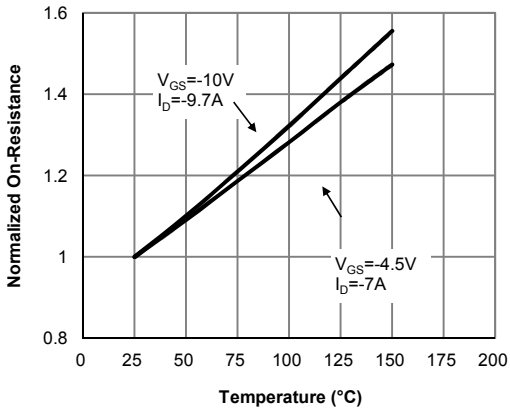



Figure 4: On-Resistance vs. Junction Temperature (Note E)

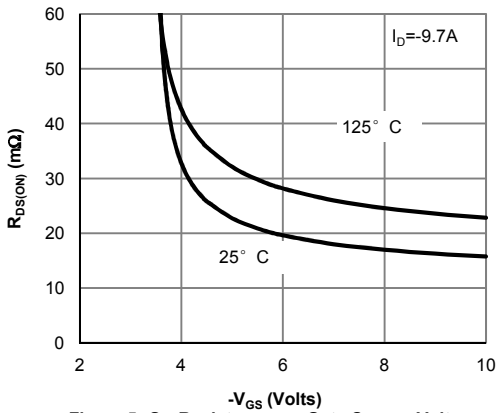



Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

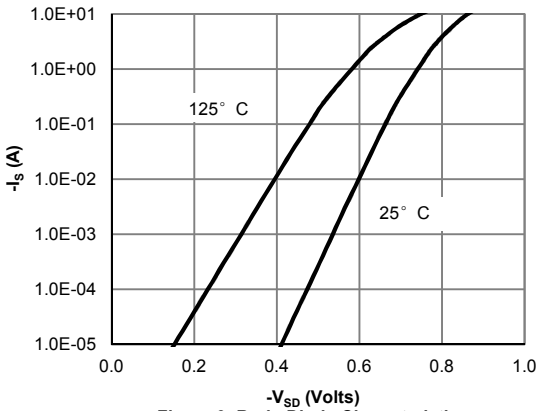



Figure 6: Body-Diode Characteristics (Note E)

**P-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

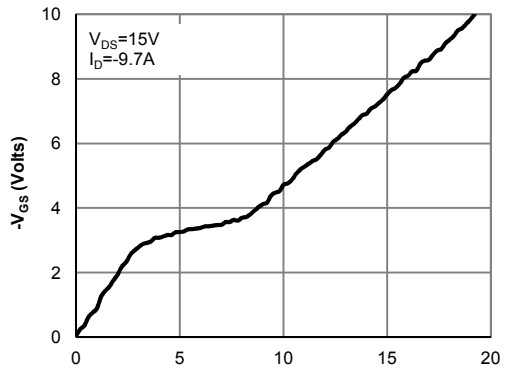



**Figure 7: Gate-Charge Characteristics**

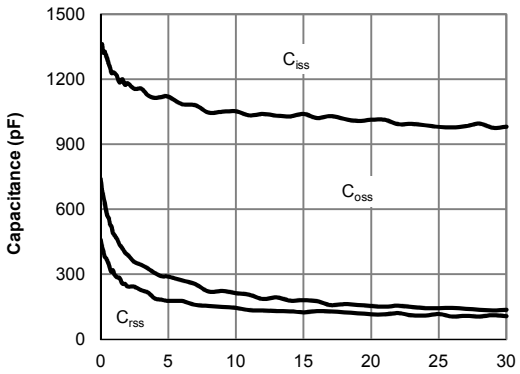
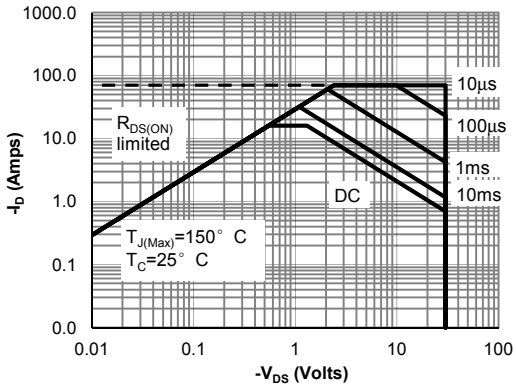



**Figure 8: Capacitance Characteristics**




**$V_{GS}$> or equal to 4.5V**
**Figure 9: Maximum Forward Biased Safe Operating Area (Note F)**

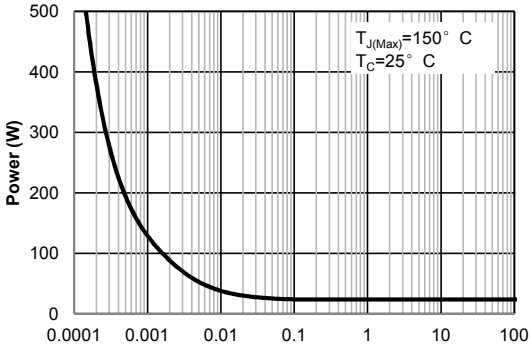



**Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)**

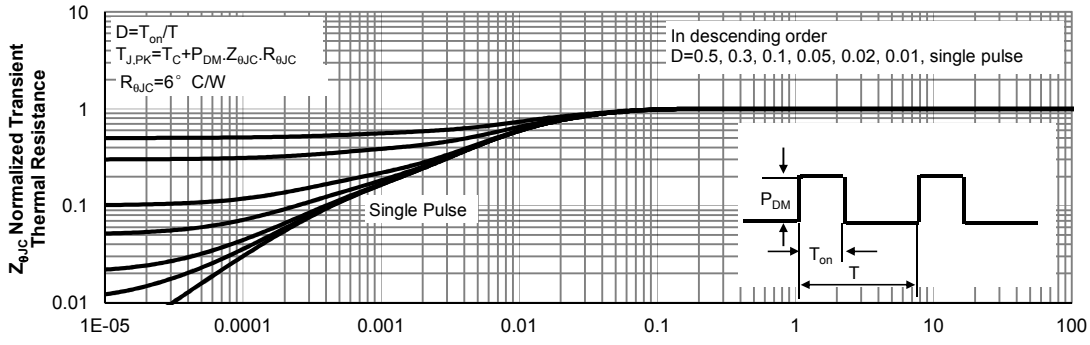



**Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)**

**P-Channl TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS**

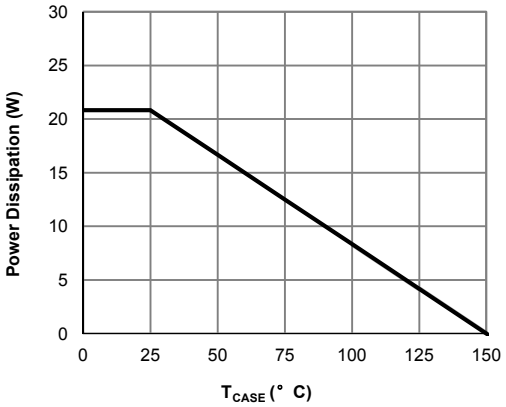



**Figure 12: Power De-rating (Note F)**

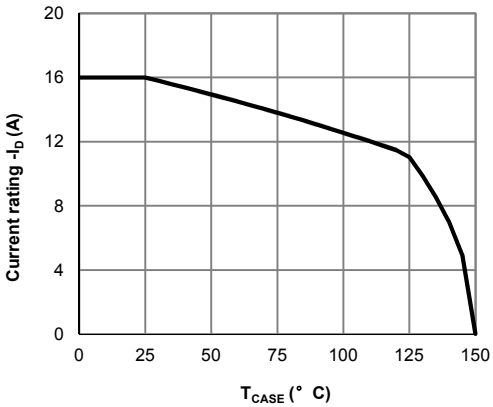



**Figure 13: Current De-rating (Note F)**

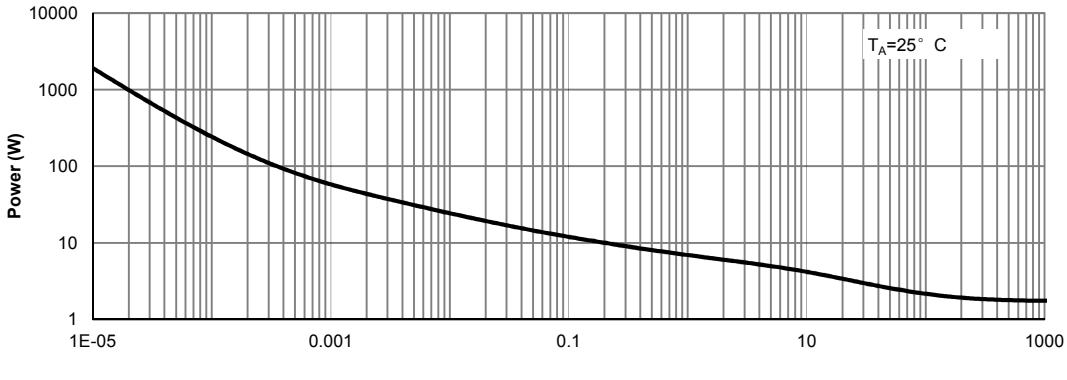



**Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note H)**

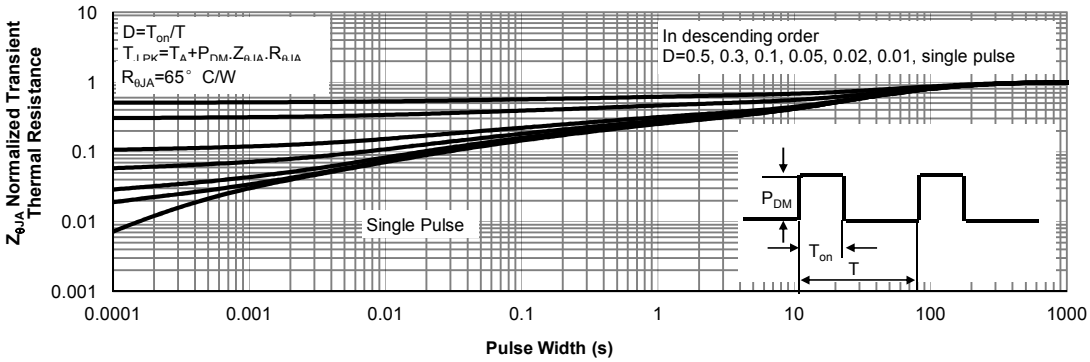



**Figure 15: Normalized Maximum Transient Thermal Impedance (Note H)**

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