

## General Description

The WSD4090DN56 advanced trench technology to provide excellent RDS(ON), low gate charge and operation with gate voltages as low as 4.5V. This device is suitable for use as a Battery protection or in other Switching application.

## Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

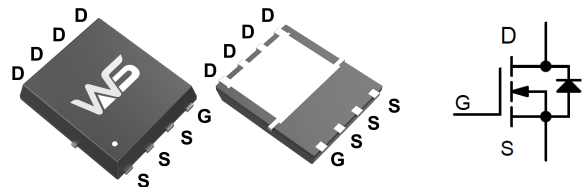
## Product Summary

BVDSS	RDSON	ID
40V	4.0mΩ	90A

## Applications

- Battery protection
- Load switch
- Uninterruptible power supply

## DFN5X6-8L Pin Configuration



## Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	90	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	62	A
$I_{DM}$	Pulsed Drain Current <sup>2</sup>	190	A
EAS	Single Pulse Avalanche Energy <sup>3</sup>	56	mJ
$I_{AS}$	Avalanche Current	34	A
$P_D@T_C=25^\circ C$	Total Power Dissipation <sup>4</sup>	52.1	W
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ C$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ C$

## Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>	---	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case <sup>1</sup>	---	2.4	$^\circ C/W$

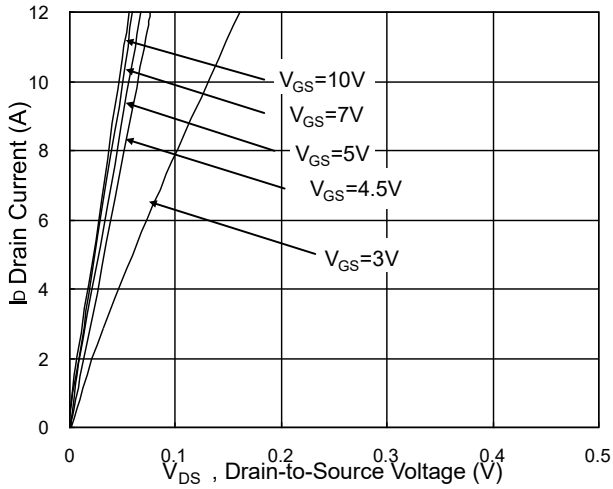
**Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V , I <sub>D</sub> =250uA	40	---	---	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	BV <sub>DSS</sub> Temperature Coefficient	Reference to 25 °C , I <sub>D</sub> =1mA	---	0.043	---	V/°C
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =10V , I <sub>D</sub> =20A	---	4.0	5.5	mΩ
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =4.5V , I <sub>D</sub> =15A	---	5.9	---	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =250uA	1.6	2.9	4.0	V
ΔV <sub>GS(th)</sub>	V <sub>GS(th)</sub> Temperature Coefficient		---	-6.94	---	mV/°C
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =25 °C	---	---	2	uA
		V <sub>DS</sub> =32V , V <sub>GS</sub> =0V , T <sub>J</sub> =55 °C	---	---	10	
I <sub>GSS</sub>	Gate-Source Leakage Current	V <sub>GS</sub> =±20V , V <sub>DS</sub> =0V	---	---	±100	nA
g <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =5A	---	24	---	S
Q <sub>g</sub>	Total Gate Charge (10V)	V <sub>DS</sub> =20V , V <sub>GS</sub> =10V , I <sub>D</sub> =40A	---	20	---	nC
Q <sub>gs</sub>	Gate-Source Charge		---	5.7	---	
Q <sub>gd</sub>	Gate-Drain Charge		---	9.4	---	
T <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> =30V , V <sub>GEN</sub> =10V , R <sub>G</sub> =1Ω, I <sub>D</sub> =1A ,RL=15Ω.	---	10.9	---	ns
T <sub>r</sub>	Rise Time		---	16.4	---	
T <sub>d(off)</sub>	Turn-Off Delay Time		---	18	---	
T <sub>f</sub>	Fall Time		---	29	---	
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =20V , V <sub>GS</sub> =0V , f=1MHz	---	1492	1940	pF
C <sub>oss</sub>	Output Capacitance		---	391	---	
C <sub>rss</sub>	Reverse Transfer Capacitance		---	59	---	
I <sub>S</sub>	Continuous Source Current <sup>1,5</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current	---	---	70	A
V <sub>SD</sub>	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =20A , T <sub>J</sub> =25 °C	---	---	1.3	V

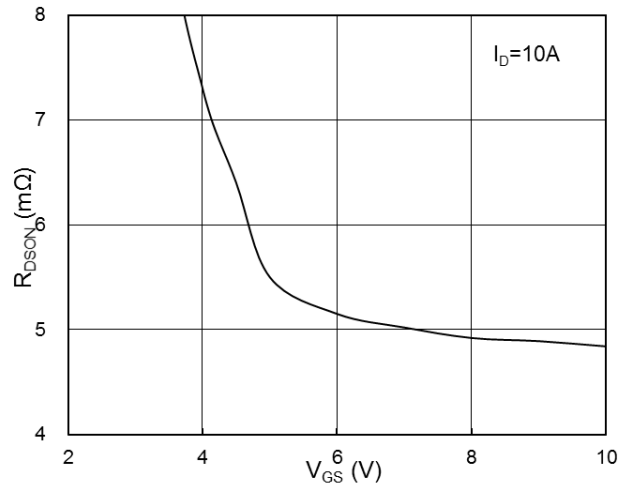
**Note :**

- 1.The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%
- 3.The EAS data shows Max. rating . The test condition is V<sub>DD</sub>=20V,V<sub>GS</sub>=10V,L=0.1mH,I<sub>AS</sub>=34A
- 4.The power dissipation is limited by 150°C junction temperature
- 5.The data is theoretically the same as I<sub>D</sub> and I<sub>DM</sub> , in real applications , should be limited by total power dissipation.

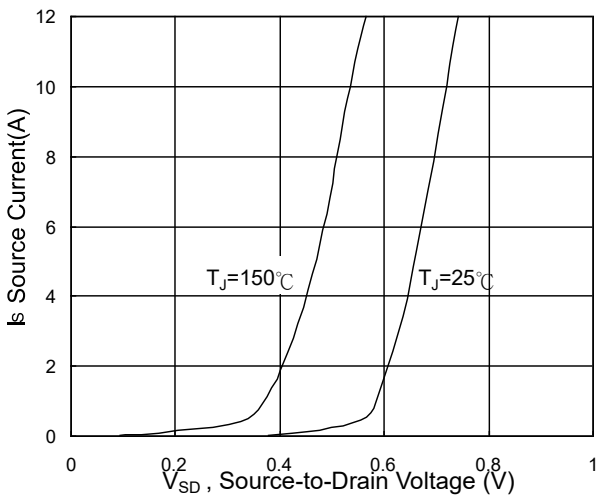
**Typical Characteristics**



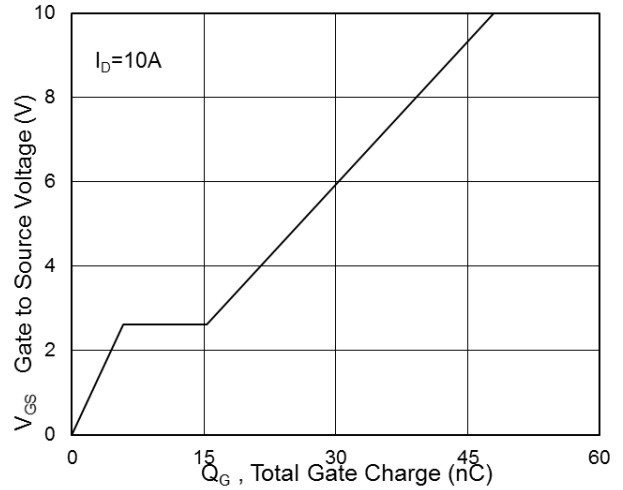
**Fig.1 Typical Output Characteristics**



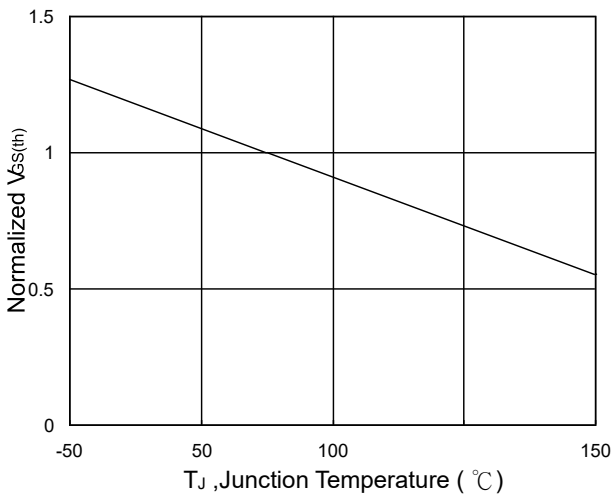
**Fig.2 On-Resistance vs. G-S Voltage**



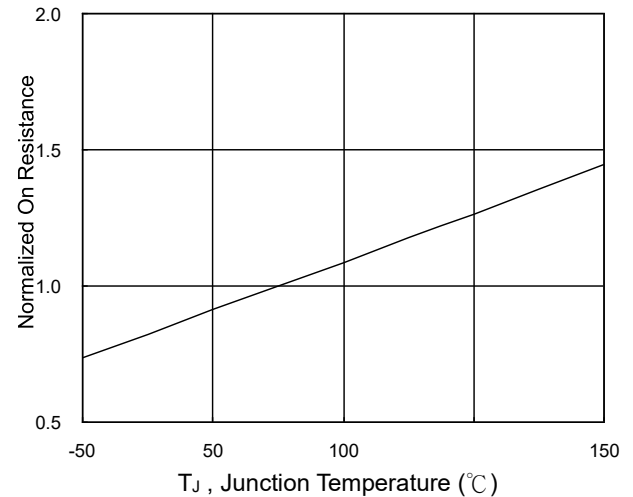
**Fig.3 Forward Characteristics of Reverse**



**Fig.4 Gate-Charge Characteristics**



**Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$**



**Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$**

Typical Characteristics

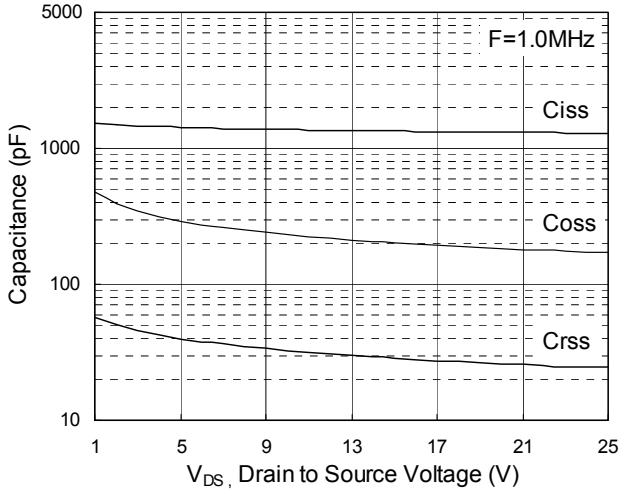


Fig.7 Capacitance

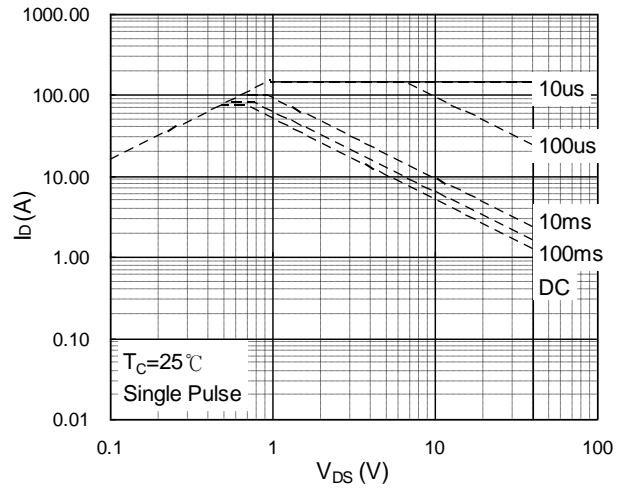


Fig.8 Safe Operating Area

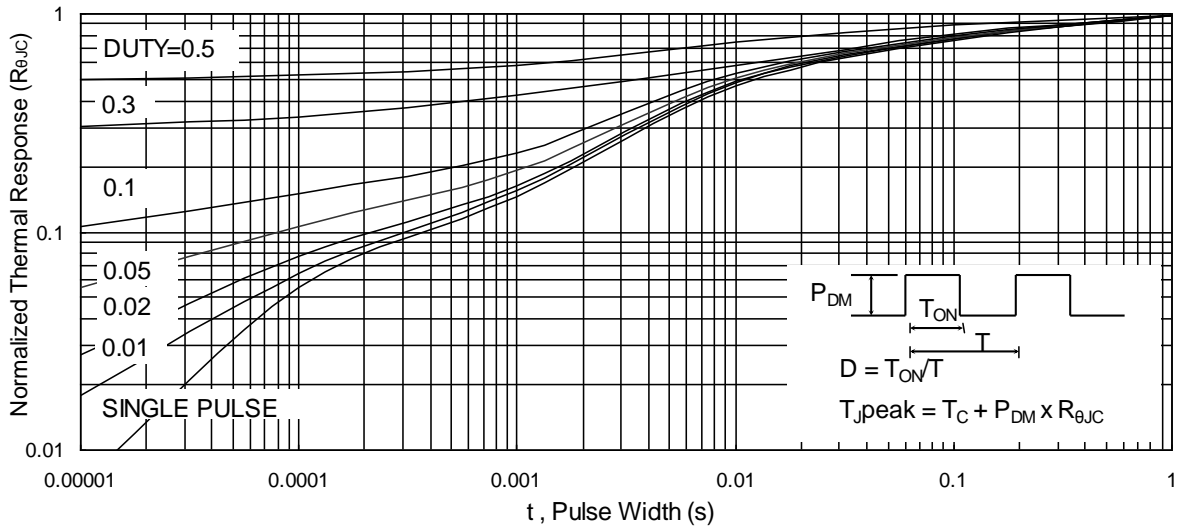


Fig.9 Normalized Maximum Transient Thermal Impedance



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