

**P-Ch MOSFET** 

# **General Description**

The WSD40L60DN56 is the highest performance trench P-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The WSD40L60DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

#### **Features**

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

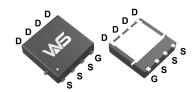
# **Product Summery**

BVDSS	RDSON	ID
-40V	10mΩ	-60A

# **Applications**

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

# **DFN5x6-8 Pin Configuration**





# **Absolute Maximum Ratings**

Symbol	Parameter	Rating	Units
V <sub>DS</sub>	Drain-Source Voltage	-40	V
$V_{GS}$	Gate-Source Voltage	±20	V
I <sub>D</sub> @T <sub>C</sub> =25℃	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-60	Α
I <sub>D</sub> @T <sub>C</sub> =100°C	Continuous Drain Current, V <sub>GS</sub> @ -10V <sup>1</sup>	-35	А
I <sub>DM</sub>	Pulsed Drain Current <sup>2</sup>	-150	Α
EAS	Single Pulse Avalanche Energy <sup>3</sup>	150	mJ
I <sub>AS</sub>	Avalanche Current	-30	Α
P <sub>D</sub> @T <sub>C</sub> =25°C	Total Power Dissipation <sup>4</sup>	50	W
T <sub>STG</sub>	Storage Temperature Range	-55 to 150	$^{\circ}$
$T_J$	Operating Junction Temperature Range	-55 to 150	℃

# **Thermal Data**

Symbol	Parameter	Тур.	Max.	Unit
$R_{ heta JA}$	Thermal Resistance Junction-Ambient <sup>1</sup>		62.5	°C/W
R <sub>θJA</sub>	Thermal Resistance Junction-Ambient <sup>1</sup> (t ≤10s)		40	°C/W
$R_{ heta JC}$	Thermal Resistance Junction-Case <sup>1</sup>		2.5	°C/W



**P-Ch MOSFET** 

# Electrical Characteristics (T<sub>J</sub>=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS}$ =0V , $I_D$ =-250uA	-40			V
$\triangle BV_{DSS}/\triangle T_{J}$	BVDSS Temperature Coefficient	Reference to 25℃, I <sub>D</sub> =-1mA		-0.030		V/°C
D		V <sub>GS</sub> =-10V , I <sub>D</sub> =-15A		10	14	0
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-10A		14	21	mΩ
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> =V <sub>DS</sub> . I <sub>D</sub> =-250uA	-1.2	-1.7	-2.5	V
$\triangle V_{GS(th)}$	V <sub>GS(th)</sub> Temperature Coefficient	V <sub>GS</sub> =V <sub>DS</sub> , I <sub>D</sub> =-250uA		4.8		mV/℃
	Drain Source Leakage Current	V <sub>DS</sub> =-32V , V <sub>GS</sub> =0V , T <sub>J</sub> =25℃			-1	uA
I <sub>DSS</sub>	Drain-Source Leakage Current	V <sub>DS</sub> =-32V , V <sub>GS</sub> =0V , T <sub>J</sub> =55℃			-5	
I <sub>GSS</sub>	Gate-Source Leakage Current	$V_{GS}$ = $\pm 20 V$ , $V_{DS}$ = $0 V$			±100	nA
gfs	Forward Transconductance	V <sub>DS</sub> =-5V , I <sub>D</sub> =-15A		25		S
Rg	Gate Resistance	V <sub>DS</sub> =0V , V <sub>GS</sub> =0V , f=1MHz		6.5		Ω
$Q_g$	Total Gate Charge (-4.5V)	V <sub>DS</sub> =-15V , V <sub>GS</sub> =-4.5V , I <sub>D</sub> =-15A		35		
$Q_{gs}$	Gate-Source Charge			3.5		nC
$Q_{gd}$	Gate-Drain Charge			13		
T <sub>d(on)</sub>	Turn-On Delay Time			45		
Tr	Rise Time	$V_{DD}$ =-15V , $V_{GS}$ =-10V , $R_G$ =6 $\Omega$		18		no
T <sub>d(off)</sub>	Turn-Off Delay Time	I <sub>D</sub> =-1A ,Rι=15Ω		180		ns
T <sub>f</sub>	Fall Time			65		
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> =-15V , V <sub>GS</sub> =0V , f=1MHz		3410		
C <sub>oss</sub>	Output Capacitance			450		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			228		

# **Guaranteed Avalanche Characteristics**

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
EAS	Single Pulse Avalanche Energy <sup>5</sup>	V <sub>DD</sub> =-20V , L=0.5mH , I <sub>AS</sub> =-24A	100			mJ

# **Diode Characteristics**

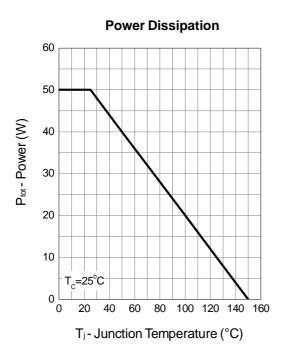
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
I <sub>S</sub>	Continuous Source Current <sup>1,6</sup>	V <sub>G</sub> =V <sub>D</sub> =0V , Force Current			-50	Α
I <sub>SM</sub>	Pulsed Source Current <sup>2,6</sup>				-150	Α
$V_{SD}$	Diode Forward Voltage <sup>2</sup>	V <sub>GS</sub> =0V , I <sub>S</sub> =-1A , T <sub>J</sub> =25℃			-1	V
t <sub>rr</sub>	Reverse Recovery Time	lF=-15A,dI/dt=100A/μs, T <sub>J</sub> =25℃		32		nS
Qrr	Reverse Recovery Charge			24		nC

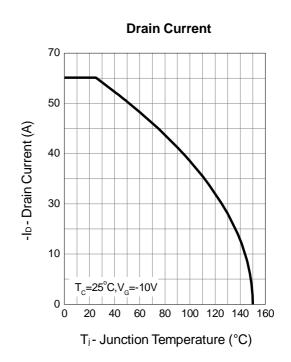
#### Note:

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper,t≦10sec.
- 2.The data tested by pulsed , pulse width  $\leqq 300 \text{us}$  , duty cycle  $\leqq 2\%$
- 3. The EAS data shows Max. rating . The test condition is  $V_{DD}$ =-20V,  $V_{GS}$ =-10V, L=0.5mH,  $I_{AS}$ =-24A
- 4.The power dissipation is limited by 150°C junction temperature
- 5. The Min. value is 100% EAS tested guarantee.
- 6. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

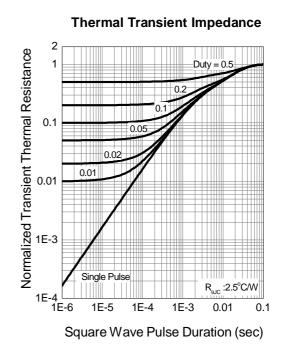


# **Typical Characteristics**



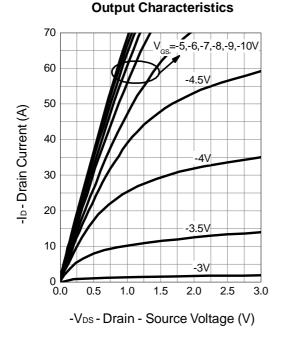


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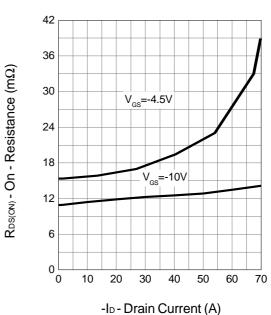




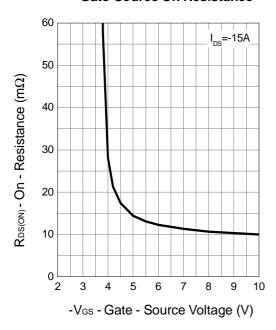
# **Typical Characteristics**



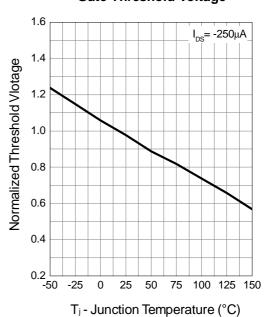
## **Drain-Source On Resistance**



## **Gate-Source On Resistance**



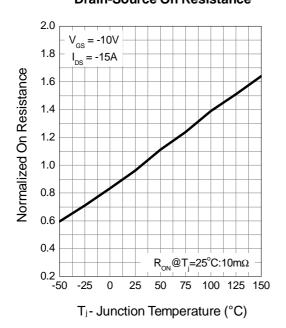
# **Gate Threshold Voltage**



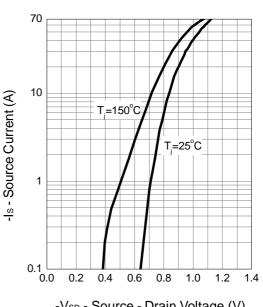


# **Typical Characteristics**

# **Drain-Source On Resistance**

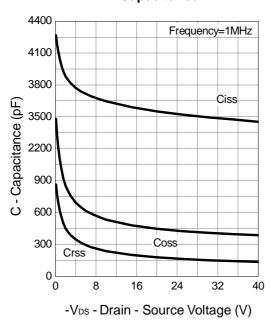


## **Source-Drain Diode Forward**

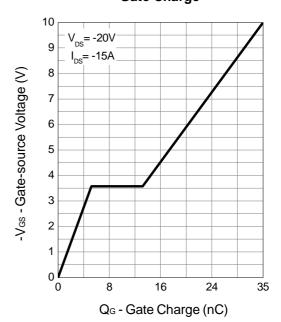


-V<sub>SD</sub> - Source - Drain Voltage (V)

# Capacitance



# **Gate Charge**





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PJMF280N60E1 T0 00201 PJMF600N65E1 T0 00201 PJMF900N65E1 T0 00201