

### Description

The WSD45P10DN56 uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.

### Features

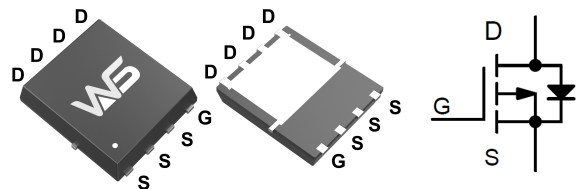
- Super high dense cell design
- Advanced trench process technology
- Reliable and rugged
- High density cell design for ultra low On-Resistance

BVDSS	RDS(ON)	ID
-100V	62 mΩ	-27.5A

### Application

- Portable equipment and battery powered systems

### DFN5X6-8 Pin Configuration



### Absolute Maximum Ratings @TA=25°C unless otherwise noted

Symbol	Parameter	Ratings	Unit
V <sub>DSS</sub>	Drain-Source Voltage	-100	V
V <sub>GSS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current (Continuous) *C	T <sub>C</sub> =25°C	-27.5
		T <sub>C</sub> =100°C	-17.4
I <sub>DM</sub>	Drain Current (Pulse) *B	-110	A
P <sub>D</sub>	Power Dissipation	T <sub>C</sub> =25°C	104
T <sub>J</sub> /T <sub>STG</sub>	Operating Temperature/ Storage Temperature	-55~150	°C

### Thermal Resistance Ratings

Symbol	Parameter	Maximum	Unit
R <sub>thJC</sub>	Maximum Junction-to-Case (Drain) *A	Steady State	1.2

**Electrical Characteristics @ $T_A=25^{\circ}\text{C}$  unless otherwise noted**

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = -250\mu A$	-100	--	--	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -80V, V_{GS} = 0V$	--	--	-1	$\mu A$
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{DS} = -250\mu A$	-1	--	-2.5	V
$I_{GSS}$	Gate Leakage Current	$V_{GS} = 20V, V_{DS} = 0V$	--	--	100	nA
$R_{DS(on)}$	Drain-Source On-state Resistance	$V_{GS} = -10V, I_D = -20A$	--	62	81	m $\Omega$
$R_{DS(on)}$		$V_{GS} = -6V, I_D = -15A$	--	65	84.5	m $\Omega$
$R_{DS(on)}$		$V_{GS} = -4.5V, I_D = -15A$	--	70	91	m $\Omega$
$V_{SD}$	Diode Forward Voltage	$I_{SD} = -1A, V_{GS} = 0V$	--	--	-1.2	V
$I_S$	Diode Forward Current *C	$T_C = 25^{\circ}\text{C}$	--	--	-27.5	A
$Q_g$	Total Gate Charge	$V_{GS} = -10V,$ $V_{DS} = -80V,$ $I_D = -18A$	--	75	--	nC
$Q_{gs}$	Gate-Source Charge		--	9	--	nC
$Q_{gd}$	Gate-Drain Charge		--	18	--	nC
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = -10V,$ $V_{DS} = -50V,$ $I_D = -18A,$ $R_G = 3.3R$	--	17	--	ns
$t_r$	Turn-on Rise Time		--	6	--	ns
$t_{d(off)}$	Turn-off Delay Time		--	75	--	ns
$t_f$	Turn-Off Fall Time		--	10	--	ns
$C_{iss}$	Input Capacitance	$V_{DS} = -50V,$ $V_{GS} = 0V,$ $f = 1.0\text{MHz}$	--	2590	--	pF
$C_{oss}$	Output Capacitance		--	320	--	pF
$C_{rss}$	Reverse Transfer Capacitance		--	45	--	pF

**Note:**

- A: The value of  $R_{\theta JA}$  is measured with the device mounted on 1in2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A=25^{\circ}\text{C}$ . The value in any given application depends on the user's specific board design.
- B: Repetitive rating, pulse width limited by junction temperature.
- C: The current rating is based on the  $t_s \leq 10\text{s}$  junction to ambient thermal resistance rating.
- D: Pulse Test: Pulse Width  $\leq 300\mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

Typical Performance Characteristics ((T<sub>J</sub> = 25 °C, unless otherwise noted))

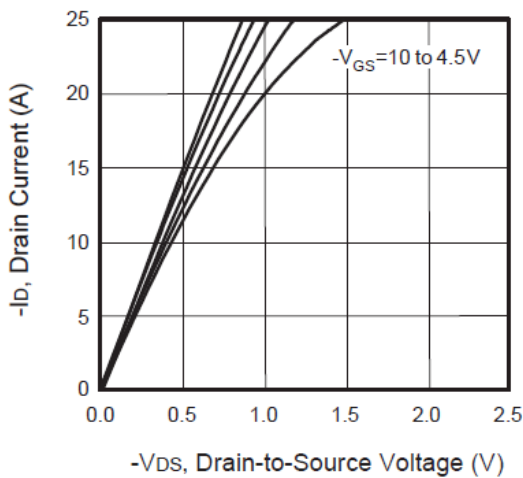


Figure 1. Output Characteristics

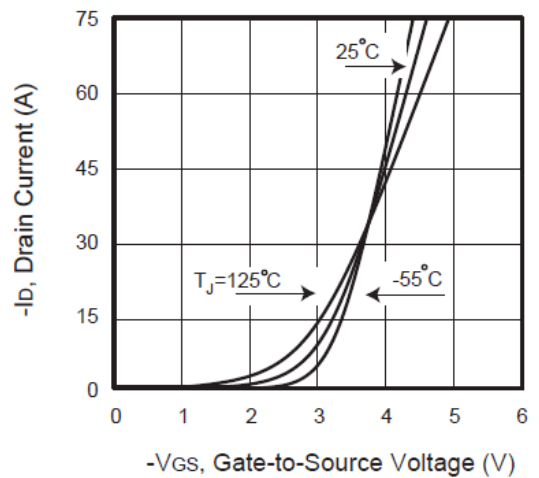


Figure 2. Transfer Characteristics

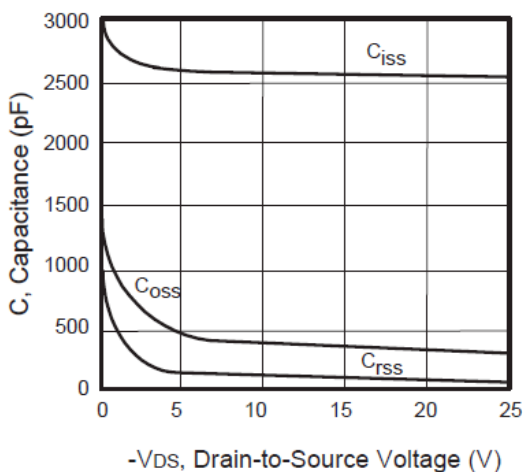


Figure 3. Capacitance

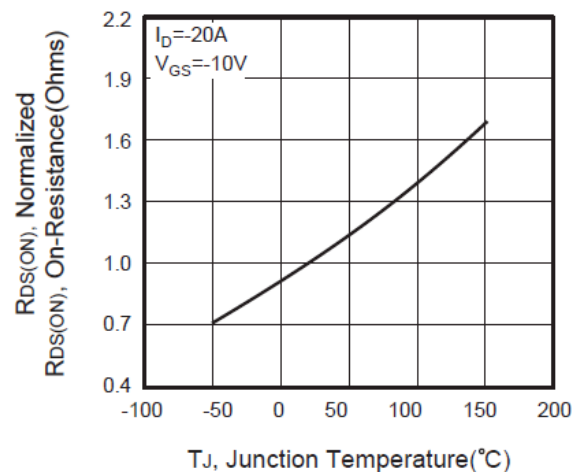


Figure 4. On-Resistance Variation with Temperature

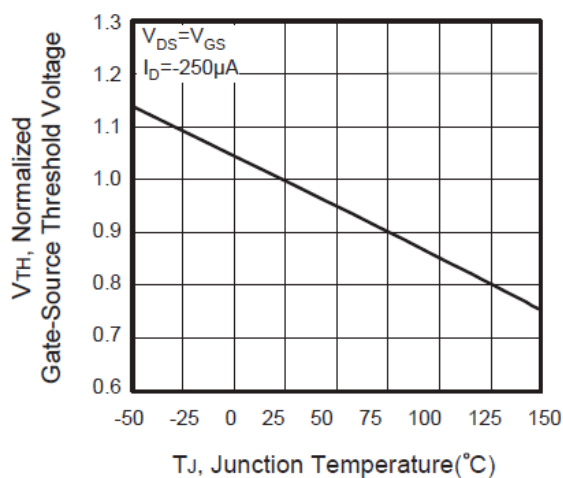


Figure 5. Gate Threshold Variation with Temperature

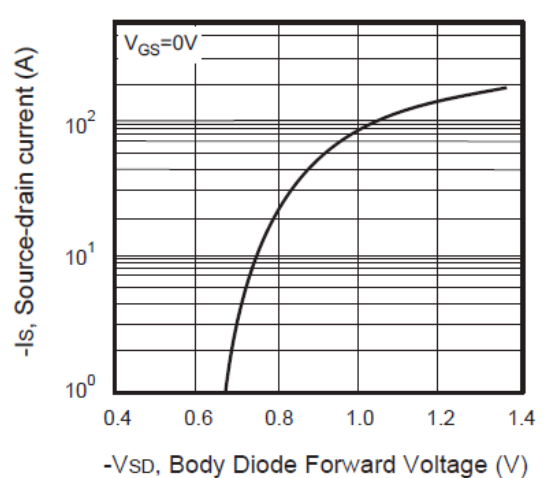


Figure 6. Body Diode Forward Voltage Variation with Source Current

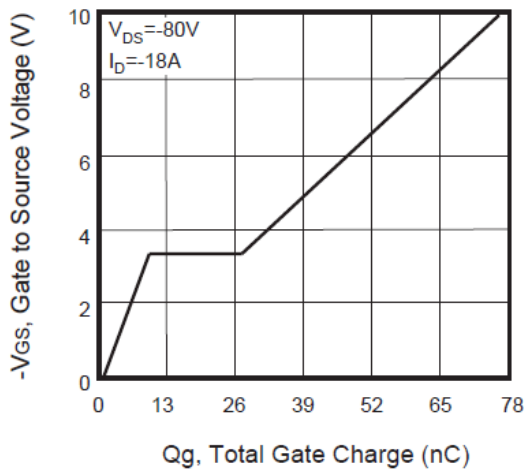


Figure 7. Gate Charge

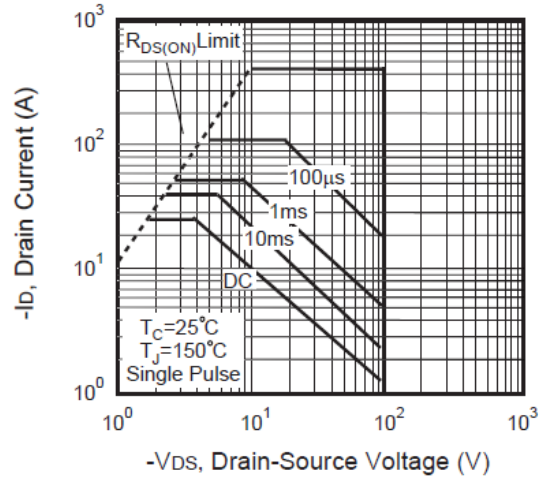


Figure 8. Maximum Safe Operating Area

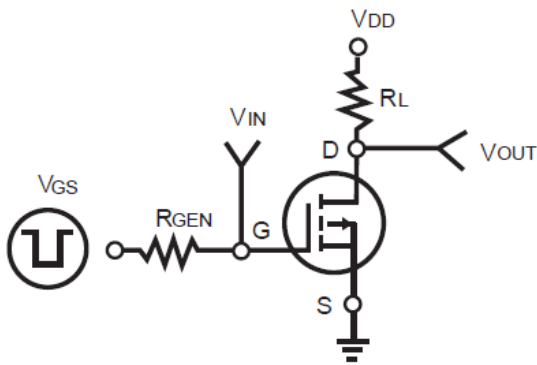


Figure 9. Switching Test Circuit

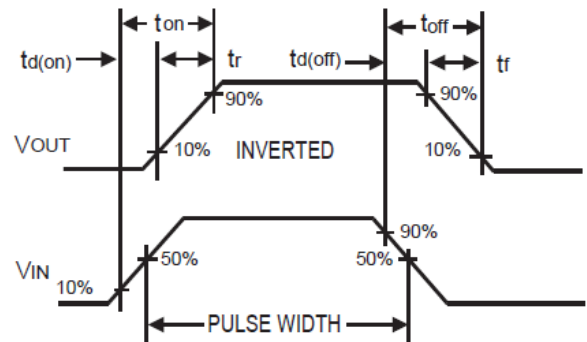


Figure 10. Switching Waveforms

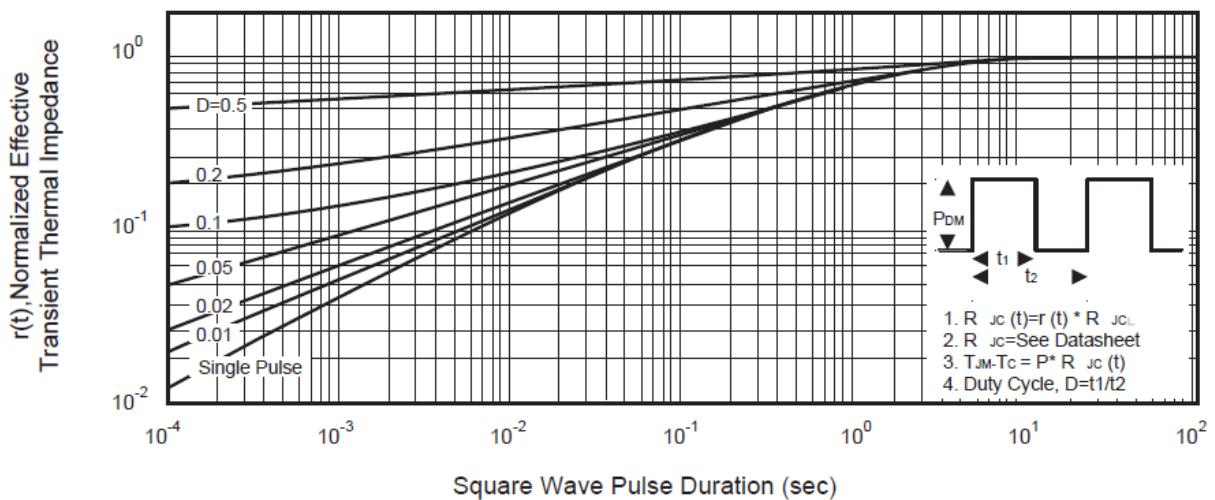


Figure 11. Normalized Thermal Transient Impedance Curve



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