General Description

The WSD6056DN56 is the highest performance trench Dual N-Ch MOSFET with extreme high cell density,which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The WSD6056DN56 meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

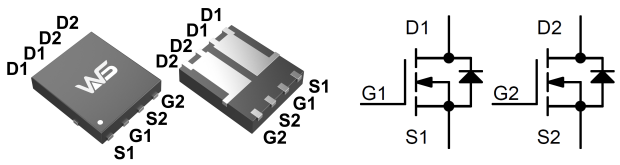
Product Summery

BVDSS	RDSON	ID
60V	16mΩ	45A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Fast switching
- Load Switch

DFN5X6C-8-EP2 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
Common Ratings				
V_{DSS}	Drain-Source Voltage		60	V
V_{GSS}	Gate-Source Voltage		±20	V
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature Range		-55 to 150	°C
I_S	Diode Continuous Forward Current	T_c=25°C	45	A
I_D	Continuous Drain Current	T_c=25°C	45	A
		T_c=70°C	28.5	
I_{DM} [b]	Pulse Drain Current Tested	T_c=25°C	180	A
P_D	Maximum Power Dissipation	T_c=25°C	67	W
		T_C=70°C	45	
$R_{\theta JL}$	Thermal Resistance-Junction to Lead	Steady State	5	°C/W
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	t ≤ 10s	45	°C/W
		Steady State [b]	90	
I_{AS} [d]	Avalanche Current, Single pulse	L=0.5mH	20	A
E_{AS} [d]	Avalanche Energy, Single pulse	L=0.5mH	20	mJ

Note a：Max. continuous current is limited by bonding wire.
Note b：Pulse width limited by max. junction temperature.
Note c：Surface mounted on 1in^2 pad area, steady state t = 999s.
Note d：UIS tested and pulse width limited by maximum junction temperature 150°C (initial temperature T_j=25°C).

Electrical Characteristics (T_J=25 ℃, unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Static Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_{DS}=250μA	60	-	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=60V, V_{GS}=0V	-	-	1	μA
		T_J=85°C	-	-	30	
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_{DS}=250μA	1.2	1.5	2.5	V
I_{GSS}	Gate Leakage Current	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
$R_{DS(ON)}$ [3]	Drain-Source On-state Resistance	V_{GS}=10V, I_{DS}=20A	-	16	20	mΩ
		V_{GS}=4.5V, I_{DS}=15A	-	20	25	
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{SD}=1A, V_{GS}=0V	-	0.75	1.2	V
t_{rr}	Reverse Recovery Time	I_{SD}=20A, dI_{SD}/dt=100A/μs	-	26	-	ns
Q_{rr}	Reverse Recovery Charge		-	30	-	nC
Dynamic Characteristics [3,4]						
R_G	Gate Resistance	V_{GS}=0V,V_{DS}=0V,F=1MHz	-	0.9	-	Ω
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=30V, F=1.0MHz Ω	-	945	-	pF
C_{oss}	Output Capacitance		-	275	-	
C_{rss}	Reverse Transfer Capacitance		-	26	-	
$t_{d(ON)}$	Turn-on Delay Time	VDD=30V, I_{DS}=1A, V_{GEN}=10V, R_G=3.3Ω.	-	10	-	ns
t_r	Turn-on Rise Time		-	13.5	-	
$t_{d(OFF)}$	Turn-off Delay Time		-	28	-	
t_f	Turn-off Fall Time		-	20	-	
Gate Charge Characteristics [3,4]						
Q_g	Total Gate Charge	V_{DS}=30V, V_{GS}=10V, I_{DS}=20A	-	28	-	nC
Q_g	Total Gate Charge	V_{DS}=30V, V_{GS}=10V, I_{DS}=20A	-	17.6	-	
Q_{gth}	Threshold Gate Charge		-	3.5	-	
Q_{gs}	Gate-Source Charge		-	2.7	-	
Q_{gd}	Gate-Drain Charge		-	6.3	-	

Note :
1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. V_{DD}=48V,V_{GS}=10V,L=0.1mH,I_{AS}=20A.,R_G=25Ω Starting T_J=25
3. The data tested by pulsed , pulse width<=300us , duty cycle<=2%.
4. Essentially independent of operating temperature.

Typical Operating Characteristics

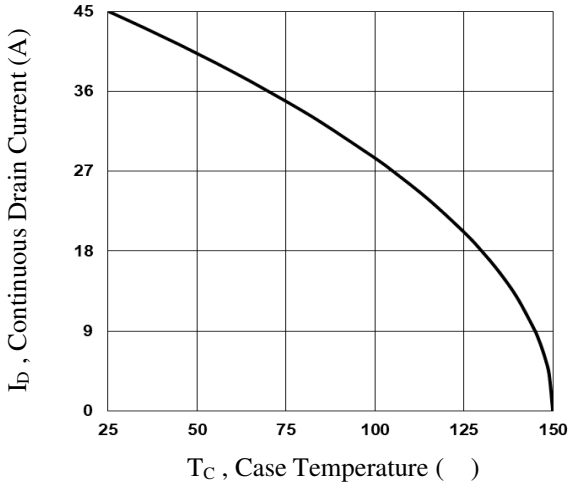


Fig.1 Continuous Drain Current vs. T_C

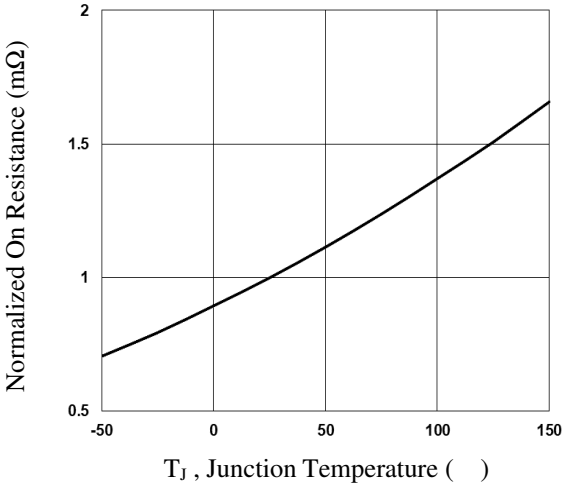


Fig.2 Normalized RDSON vs. T_J

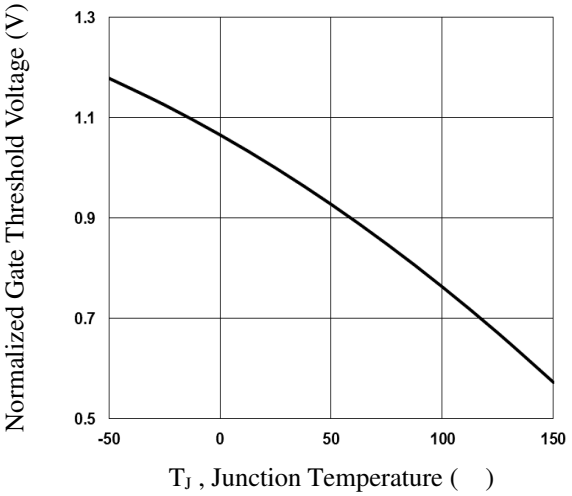


Fig.3 Normalized V_{th} vs. T_J

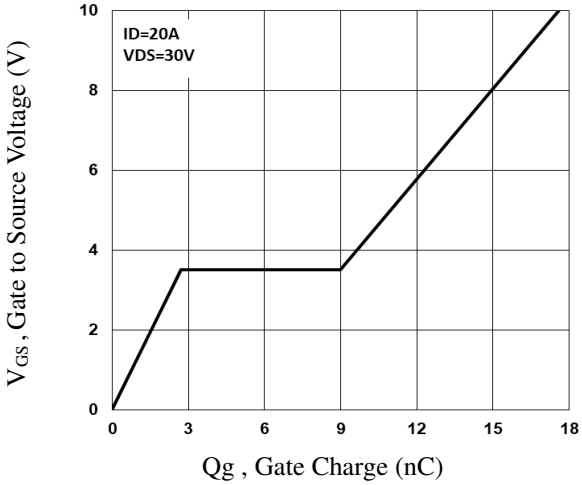


Fig.4 Gate Charge Waveform

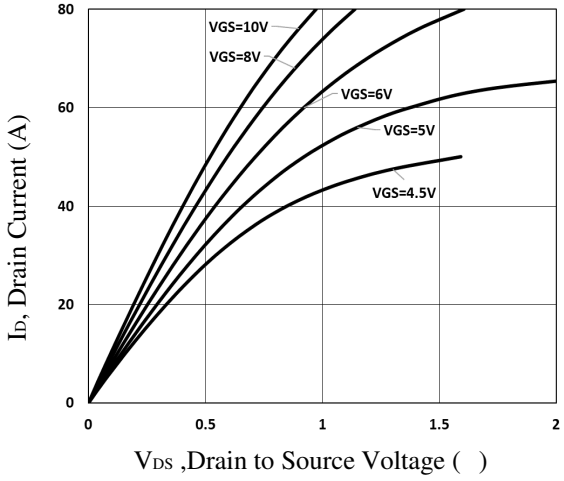


Fig.5 Typical Output Characteristics

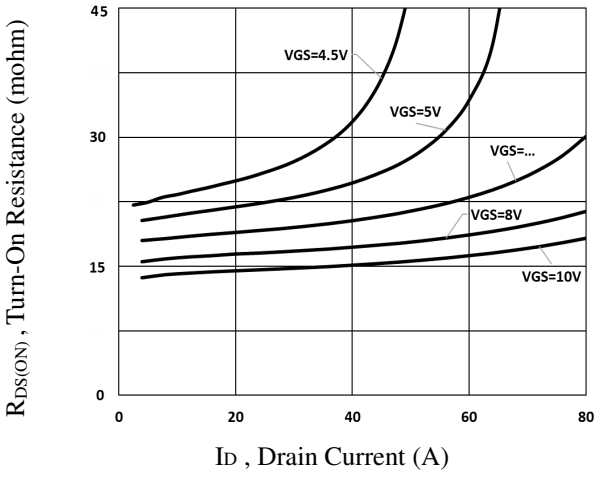


Fig.6 Turn-On Resistance vs. I_D

Typical Operating Characteristics(Cont.)

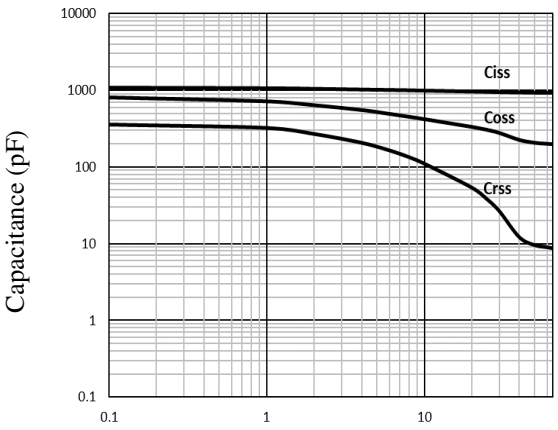


Fig.7 Capacitance Characteristics

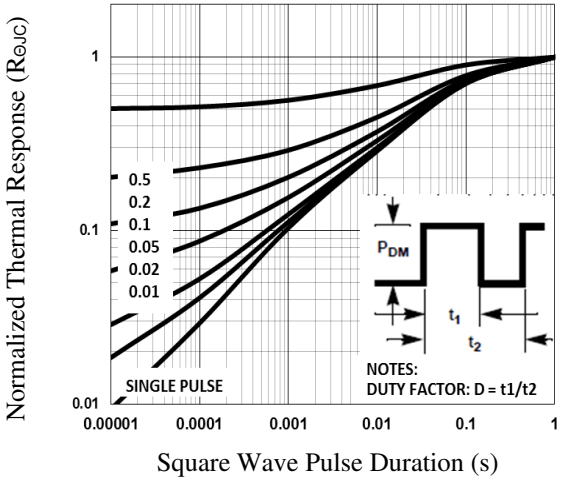


Fig.8 Normalized Transient Response

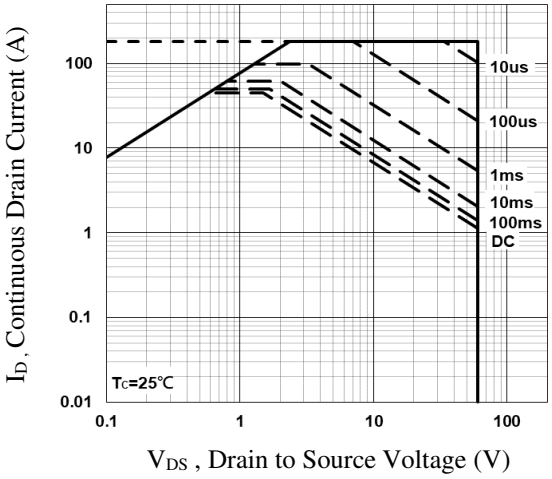


Fig.9 Maximum Safe Operation Area

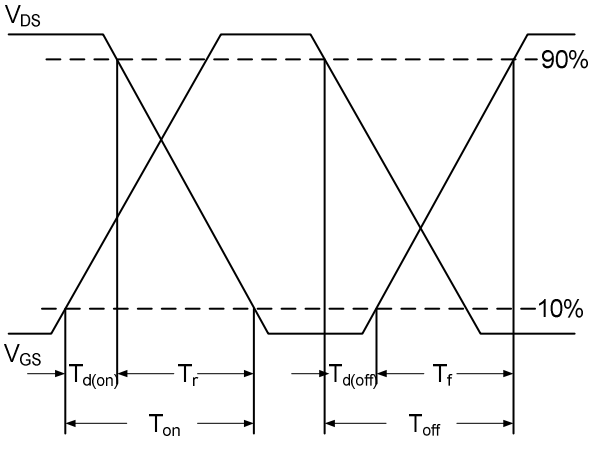


Fig.10 Switching Time Waveform

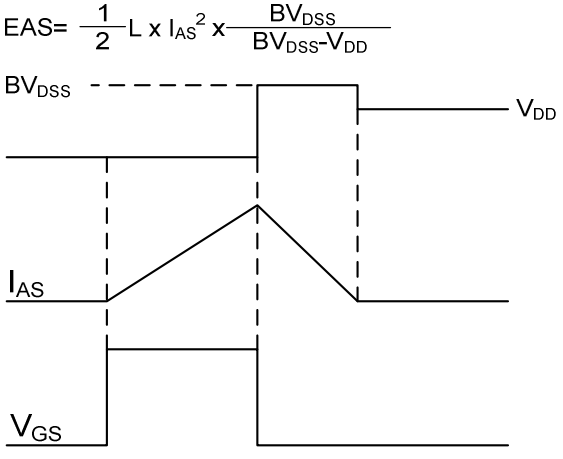


Fig.11 EAS Waveform

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