

General Description

The WSF7N40 is N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching .

performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency..

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent Cdv/dt effect decline
- Green Device Available

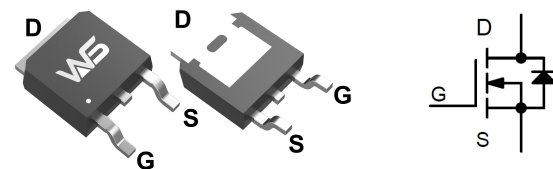
Product Summary

BVDSS	RDSON	ID
400V	0.8Ω	7A

Applications

- Uninterruptible Power Supply(UPS)
- Power Factor Correction (PFC)

TO-252 Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	400	V
V_{GS}	Gate-Source Voltage	±30	V
$I_D@T_C=25^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	7	A
$I_D@T_C=100^{\circ}C$	Continuous Drain Current, $V_{GS} @ 10V^1$	4.0	A
I_{DM}	Pulsed Drain Current ²	28	A
EAS	Single Pulse Avalanche Energy ³	176	mJ
I_{AR}	Avalanche Current	7	A
$P_D@T_C=25^{\circ}C$	Total Power Dissipation ³	33	W
T_{STG}	Storage Temperature Range	-55 to 150	°C
T_J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	60	°C/W
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	3.8	°C/W

Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	400	---	---	V
ΔBV _{DSS} /ΔT _J	BVDSS Temperature Coefficient	Reference to 25°C, I _D =1mA	---	0.25	---	V/°C
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =4A	---	0.8	1.1	Ω
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	2.0	3.5	4.0	V
ΔV _{GS(th)}	V _{GS(th)} Temperature Coefficient		---	-4.63	---	mV/°C
I _{DSS}	Drain-Source Leakage Current	V _{DS} =400V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =400V, V _{GS} =0V, T _J =125°C	---	---	10	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±30V, V _{DS} =0V	---	---	±100	nA
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	1.6	---	Ω
Q _g	Total Gate Charge (10V)	V _{DS} =400V, V _{GS} =10V, I _D =7A	---	19	---	nC
Q _{gs}	Gate-Source Charge		---	3.7	---	
Q _{gd}	Gate-Drain Charge		---	11	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =250V, V _{GS} =10V, R _G =25Ω, I _D =7A	---	13	---	ns
T _r	Rise Time		---	20	---	
T _{d(off)}	Turn-Off Delay Time		---	76	---	
T _f	Fall Time		---	40	---	
C _{iss}	Input Capacitance	V _{DS} =25V, V _{GS} =0V, f=1MHz	---	700	---	pF
C _{oss}	Output Capacitance		---	94	---	
C _{rss}	Reverse Transfer Capacitance		---	12	---	

Guaranteed Avalanche Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
EAS	Single Pulse Avalanche Energy ⁵	V _{DD} =50V, L=0.1mH, I _{AS} =4.5A	90	---	---	mJ

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current ^{1,6}	V _G =V _D =0V, Force Current	---	---	7	A
I _{SM}	Pulsed Source Current ^{2,6}		---	---	28	A
V _{SD}	Diode Forward Voltage ²	V _{GS} =0V, I _S =7A, T _J =25°C	---	---	1.4	V
t _{rr}	Reverse Recovery Time	I _F =7A, di/dt=100A/μs, T _J =25°C	---	260	---	ns
Q _{rr}	Reverse Recovery Charge		---	3.8	---	uC

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper, t<10sec.
- The data tested by pulsed, pulse width ≤ 300us, duty cycle ≤ 2%
- The EAS data shows Max. rating. The test condition is V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=2.5A
- The power dissipation is limited by 150°C junction temperature
- The Min. value is 100% EAS tested guarantee.
- The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

Typical Characteristics

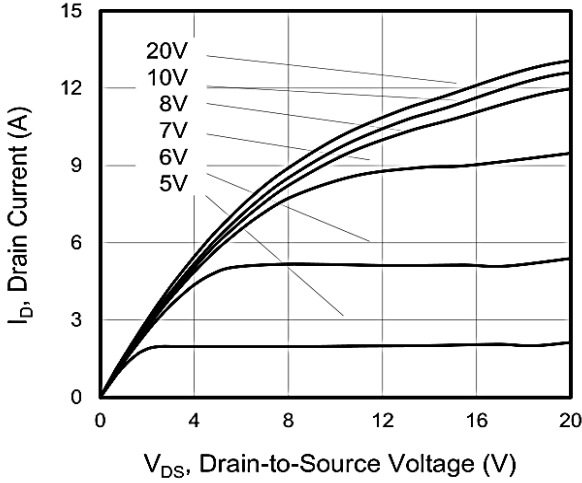


Figure 1. Output Characteristics ($T_J = 25^\circ\text{C}$)

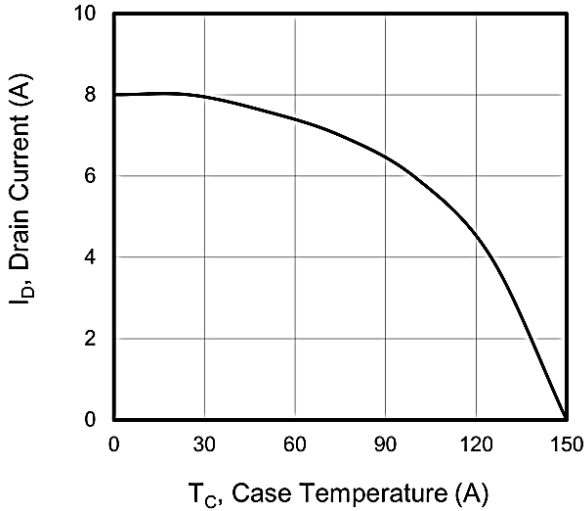


Figure 3. Drain Current vs. Temperature

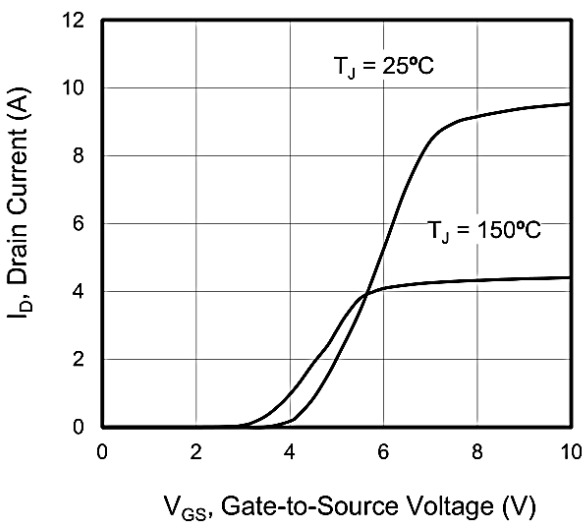


Figure 5. Transfer Characteristics

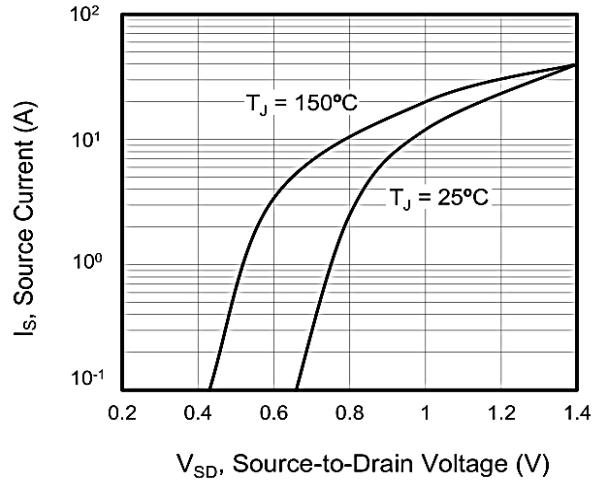


Figure 2. Body Diode Forward Voltage

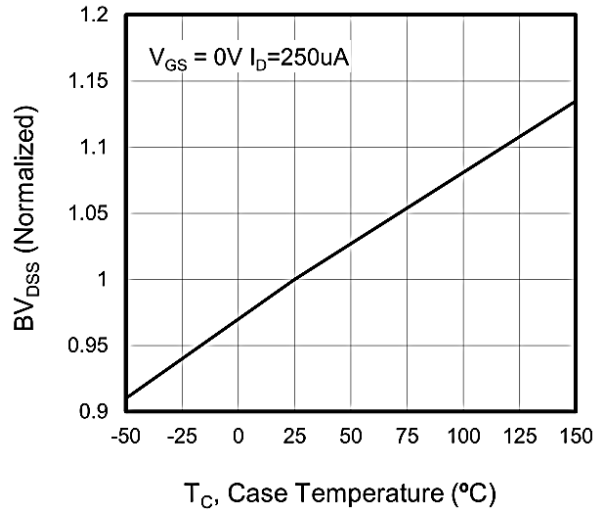


Figure 4. BV_{DSS} Variation vs. Temperature

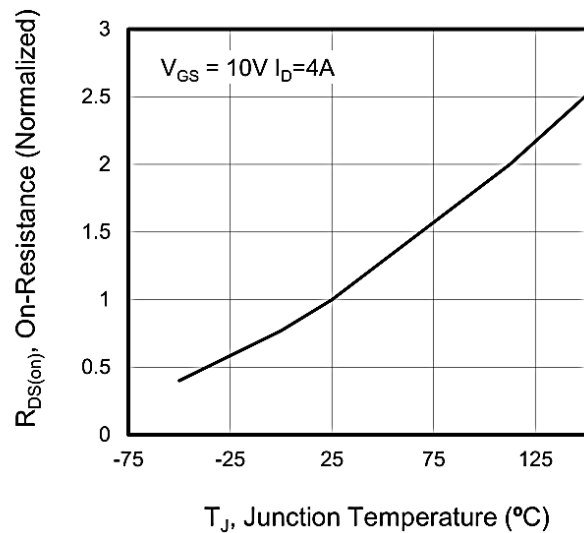


Figure 6. On-Resistance vs. Temperature

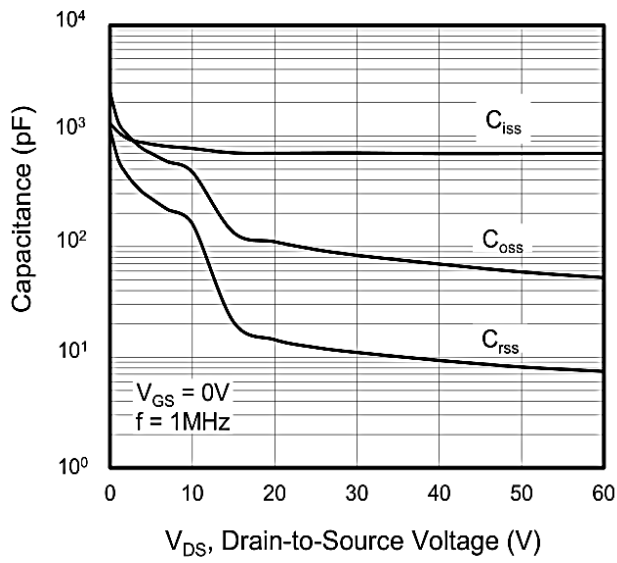


Figure 7. Capacitance

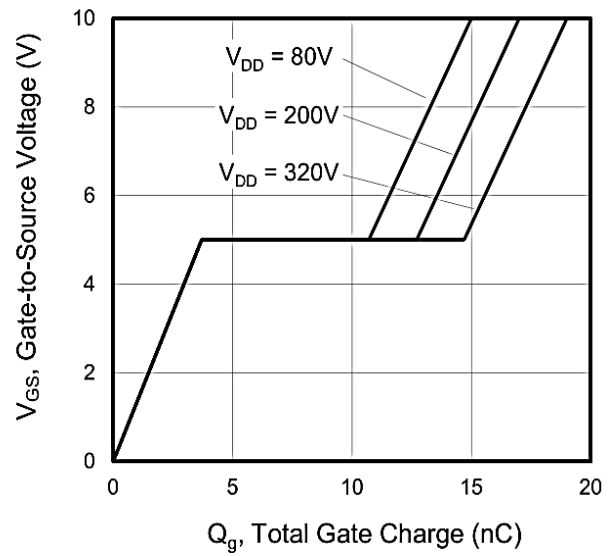


Figure 8. Gate Charge

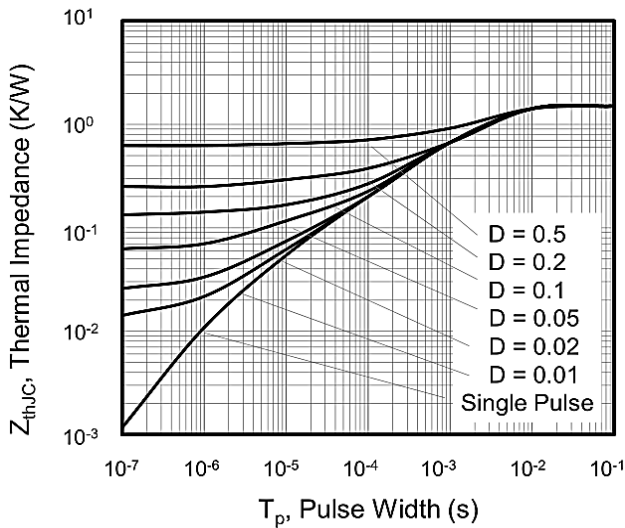


Figure 9. Transient Thermal Impedance



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