

General Description

The WSP4016 is the highest performance trench N-ch MOSFET with extreme high cell density, which provide excellent RDSON and gate chargens for most of the synchronous buck converter applications .

The WSP4016 meet the RoHS and Green Product requirement, 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	40	V
V_{GS}	Gate-Source Voltage	± 20	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	15.5	A
$I_D@T_C=70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	8.4	A
I_{DM}	Pulsed Drain Current ²	30	A
$P_D@T_A=25^\circ C$	Total Power Dissipation $T_A=25^\circ C$	2.08	W
$P_D@T_A=70^\circ C$	Total Power Dissipation $T_A=70^\circ C$	1.3	W
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
$R_{\theta JA}$	Thermal Resistance Junction-ambient ¹	---	60	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	---	20	$^\circ C/W$

Notes

- Surface Mounted on 1" x 1" FR4 Board.
- Pulse width limited by maximum junction temperature

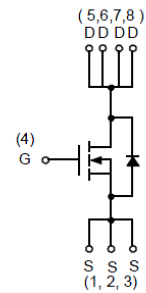
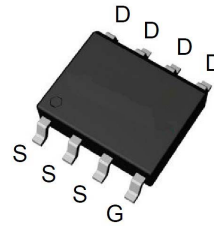
Product Summery

BVDSS	RDSON	ID
40V	11.5m Ω	15.5A

Applicatio

- White LED boost converters
- Automotive Systems
- Industrial DC/DC Conversion Circuits

SOP-8 Pin Configuration



Electrical Characteristics (T_J=25 °C, unless otherwise noted)

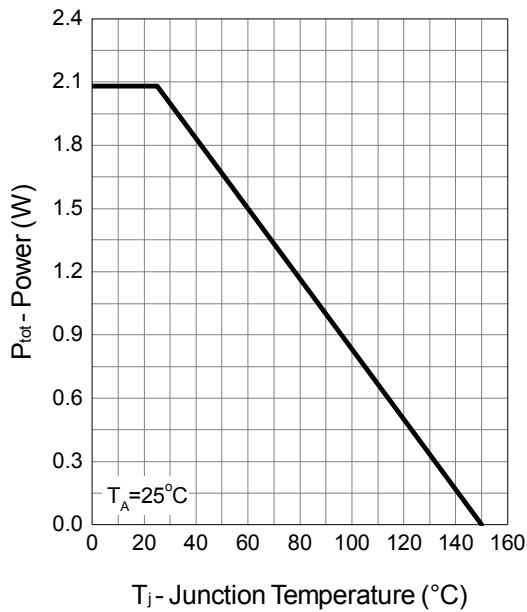
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	40	---	---	V
R _{DS(ON)}	Static Drain-Source On-Resistance ²	V _{GS} =10V, I _D =7A	---	8.5	11.5	mΩ
		V _{GS} =4.5V, I _D =5A	---	11	14.5	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	1.8	2.5	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =32V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =32V, V _{GS} =0V, T _J =55°C	---	---	25	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
g _{fs}	Forward Transconductance	V _{DS} =5V, I _D =15A	---	31	---	S
Q _g	Total Gate Charge (4.5V)	V _{DS} =20V, V _{GS} =10V, I _D =7A	---	20	30	nC
Q _{gs}	Gate-Source Charge		---	3.9	---	
Q _{gd}	Gate-Drain Charge		---	3	---	
T _{d(on)}	Turn-On Delay Time	V _{DD} =20V, V _{GEN} =10V, R _G =1Ω, I _D =1A, R _L =20Ω.	---	12.6	---	ns
T _r	Rise Time		---	10	---	
T _{d(off)}	Turn-Off Delay Time		---	23.6	---	
T _f	Fall Time		---	6	---	
C _{iss}	Input Capacitance	V _{DS} =20V, V _{GS} =0V, f=1MHz	---	1125	---	pF
C _{oss}	Output Capacitance		---	132	---	
C _{rss}	Reverse Transfer Capacitance		---	70	---	

Note :

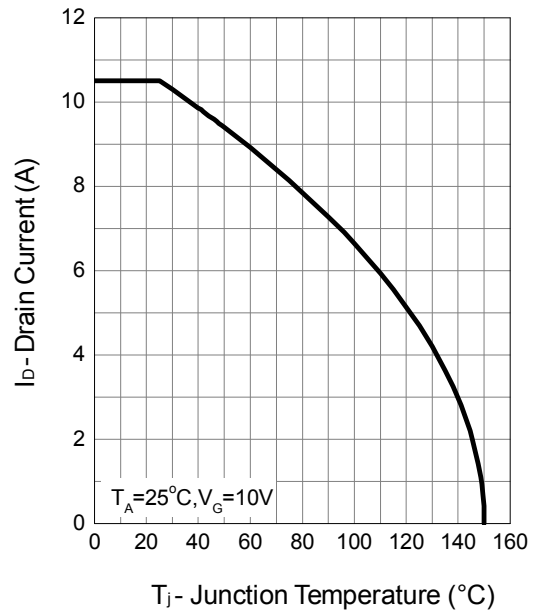
1. Pulse test: PW ≤ 300us duty cycle ≤ 2%.
2. Guaranteed by design, not subject to production testing.

Typical Characteristics

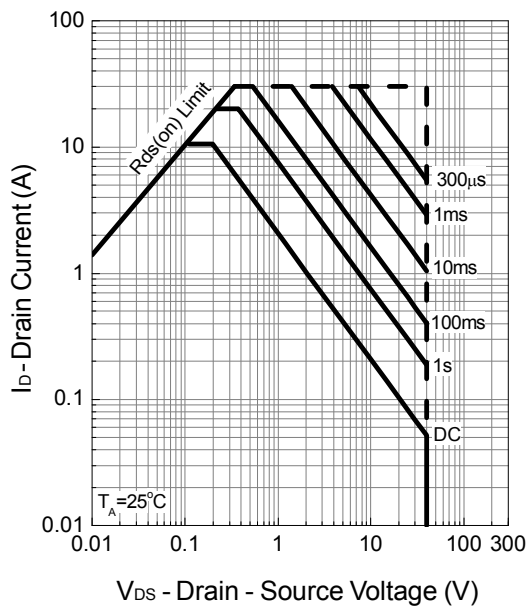
Power Dissipation



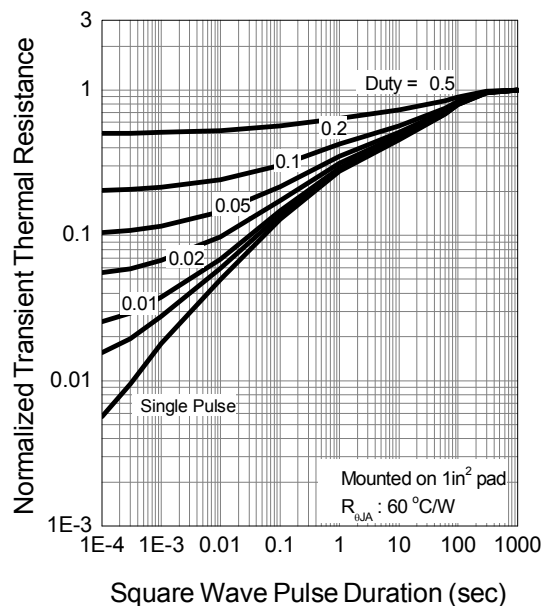
Drain Current



Safe Operation Area

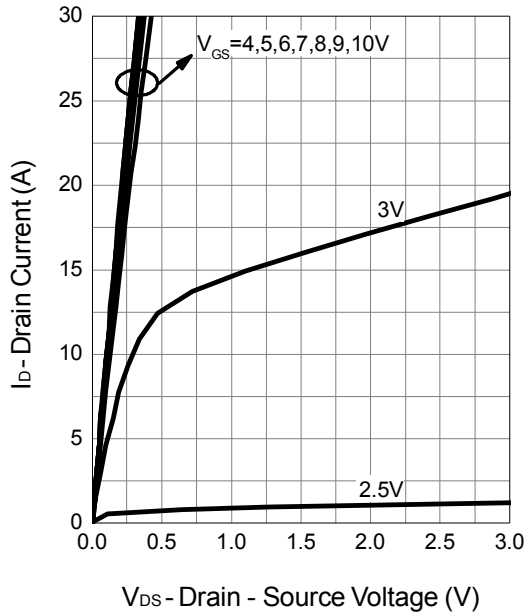


Thermal Transient Impedance

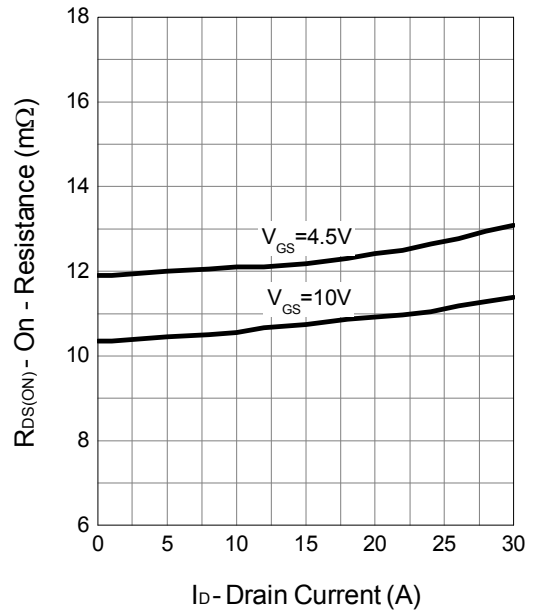


Typical Characteristics

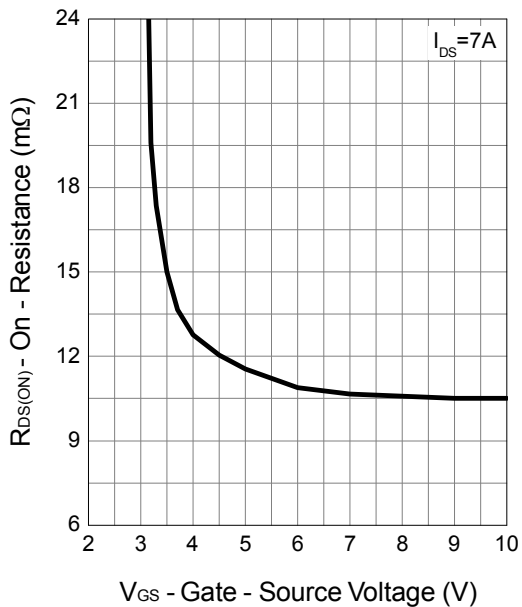
Output Characteristics



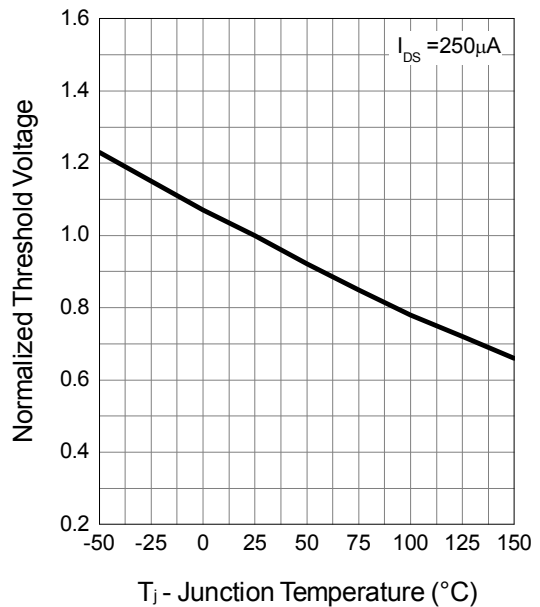
Drain-Source On Resistance



Gate-Source On Resistance

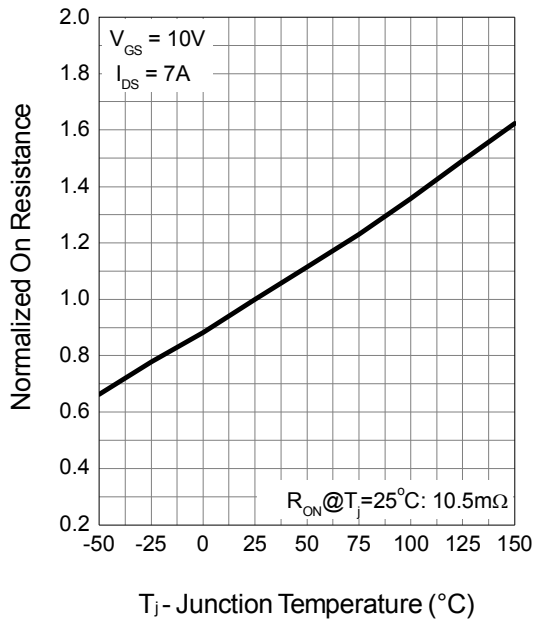


Gate Threshold Voltage

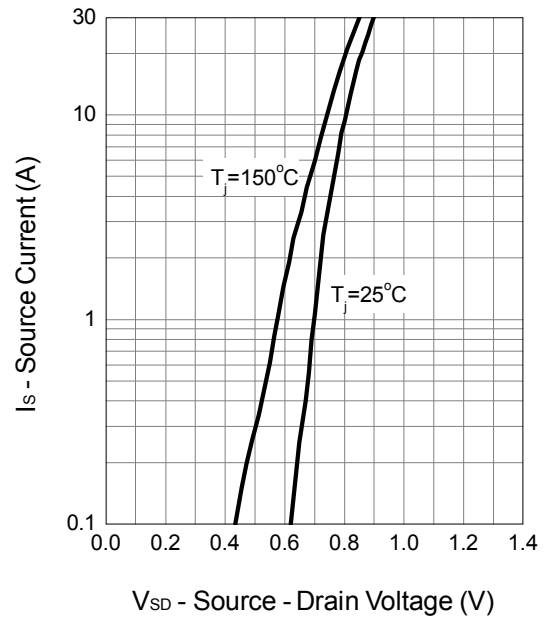


Typical Characteristics

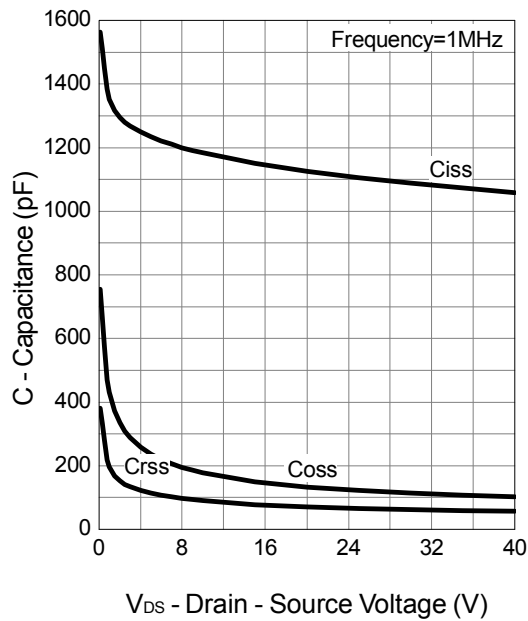
Drain-Source On Resistance



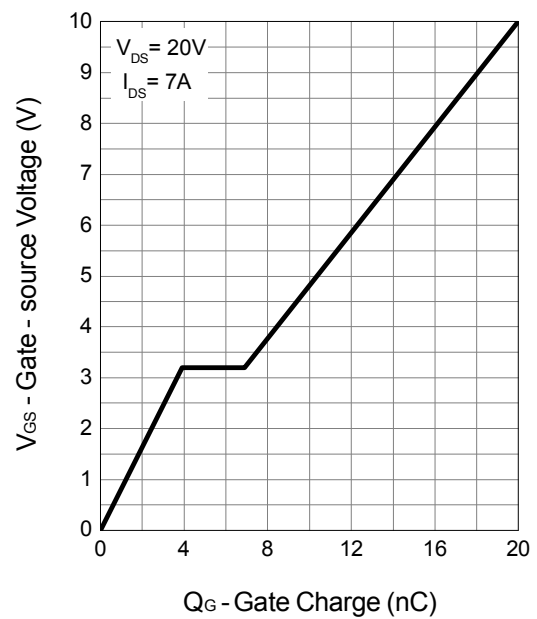
Source-Drain Diode Forward



Capacitance

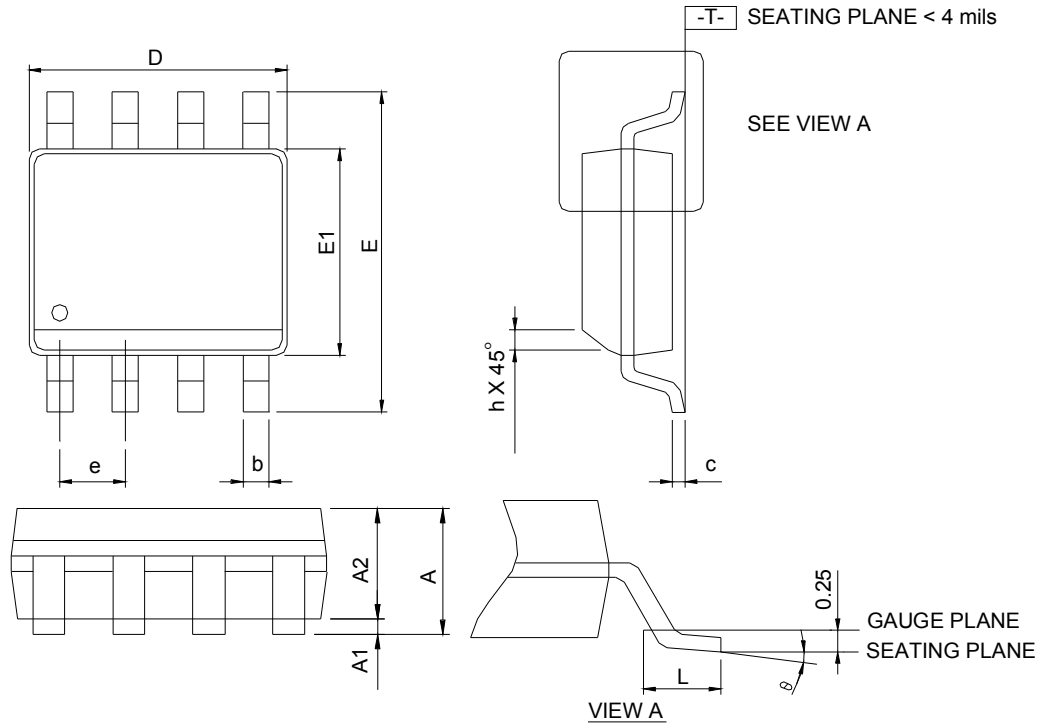


Gate Charge



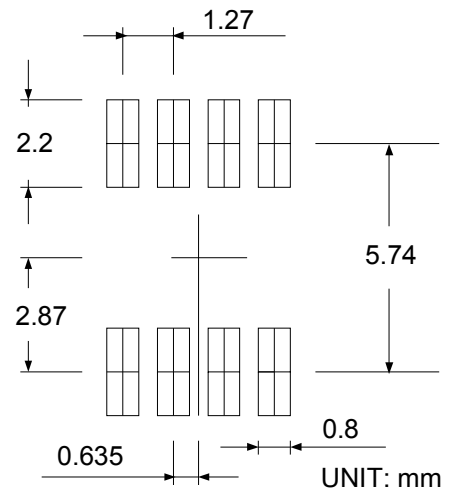
Package Information

SOP-8



S OP-8	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	-	1.75	-	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	-	0.049	-
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN



Note: 1. Follow JEDEC MS-012 AA.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.



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